International Journal of Physical Research, 12 (2) (2024) 24-28

International Journal of Physical Research

Website: www.sciencepubco.com/index.php/IJPR

Research paper

Effect of electron mobility variation on short channel effects in nanoscale double gate FinFETs: A comparative study

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Abstract

This work investigates the impact of electron mobility variations on short channel effects (SCEs) in different semiconductor materials using FinFETs. Using PADRE simulator, the work examines Gallium Arsenide (GaAs), Gallium Antimonide (GaSb), Gallium Nitride (GaN), and Silicon (Si) FinFETs, analyzing performance metrics such as Drain Induced Barrier Lowering (DIBL), Subthreshold Swing (SS) and Threshold Voltage roll-off. The result shows that GaN-FinFET exhibits lowest subthreshold swing of 63 mV/dec at electron mobility of 10000 cm^2/Vs, and threshold voltage of 0.44V at electron mobility of 10000 cm^2/Vs, while Si-FinFET exhibits lowest DIBL of 3 mV/V at (4000-10000) cm^2/Vs. This finding contributes to advancing the understanding of short channel effects in nanoscale FinFETs and provides valuable insights for optimizing device performance in future semiconductor technologies.

Keywords: *DIBL; Electron Mobility; FinFETs, SCEs, GaAs, GaSb.*

1. Introduction

The quest for smaller transistors centers on nanoscale technology, which drives major breakthroughs in semiconductors [1-7], by enabling hundreds of circuits on a chip through Very Large Scale and Ultra-Large Scale Integrations. However, reducing device dimensions generate short channel effects, (SCEs) [8-14] in single gate MOSFETs, which negatively influence current and cause off-state leakage. To address these challenges, FinFETs stand out as prospective electronic devices [15-30] due to their improved scalability and ability to control SCEs. The functionality of nanoscale FinFETs is now transitioning into a region where quantum mechanical effects such as quantum confinement effects are becoming discernible [31-32]. This confinement alters the energy band structure of the material, leading to discrete energy levels and affecting electron mobility. In the pursuit of further miniaturization and performance enhancement, it becomes imperative to delve into the intricate interplay between device dimensions, material properties, SCEs and electron mobility within FinFET structures. Electron mobility, a fundamental parameter governing the speed of charge carriers in a material under the influence of an electric field, is central to understanding the operational characteristics of FinFETs.

Numerous studies exploring the impact of Short-Channel Effects (SCEs) on the performance of FinFETs have been reported in the academic literature [33-40]. To the best of authors' knowledge, no study has been reported on the effect of electron mobility on short channel effects.

This work aims at comprehensively looking into the impact of electron mobility variations on short channel effects in nanoscale double gate FinFET devices using Si, GaSb, GaN and GaAs as channel materials. The focused on significant performance metrics: DIBL, SS, and threshold voltage roll-off, crucial in the determination of device performance. Simulations will be conducted using the PADRE Simulator, known for semiconductor device modeling. Understanding how electron mobility variations impact SCEs enables the development of strategies to optimize the performance of nanoscale FinFETs.

1.1. Device structure

The device structure of an n-channel double gate FinFET is shown in Fig. 1. The structure has important parts such the source, drain, gate length (channel length), and channel width (fin width or fin thickness). Before making the gate contact, the oxide is placed on the top surface of the fin, both on the side walls, and both sides of the side walls. Tox1 and Tox2 are the oxide thicknesses of the side wall.

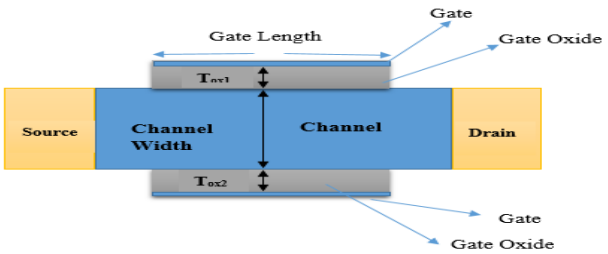

Fig. 1: Two-Dimensional Double Gate FinFET.

2. Materials and method

This section describes the materials and the method used during the device simulation.

2.1. Materials

The materials used in this research are Si, GaAs, GaSb and GaN as fin (channel) materials, silicon dioxide (SiO_2) as the gate dielectric, Silicon as base substrate and MuGFET simulation tool.

2.2. Method

The device simulation was performed in the PADRE simulator from the MuGFET tool. The impact of electron mobility on SCEs was investigated in FinFETs using different semiconductor materials. Specifically, the study examined GaAs, GaSb, GaN, and Si FinFETs and analyzed key performance metrics including DIBL, SS and threshold voltage roll-off. The oxide thickness used was 2 nm, the channel width was 10 nm, the gate length was 45 nm and the electron mobility was varied from (1000-10,000) cm^2/Vs. During the simulation, the drain/source doping was set at 1×10^{16} cm^{-3} and the channel doping concentration was maintained at 1×10^{19} cm^{-3}. While the gate bias was varied between 0 V and 1 V, and the drain bias was set between 0.05 V and 1 V. The parameters are listed in Table 1.

Table 1: Parameter Specifications Used in This Simulation

Parameter	Value
Gate Length	45 nm
Electron Mobility	(1000, 2000, 3000, 4000, 5000, 6000, 7000, 8000, 9000, 10,000) cm^2/Vs
Channel Width	10 nm
Channel Doping Concentration	1×10^{16} cm^{-3}
Source/Drain Doping Concentration	1×10^{19} cm^{-3}
Drain Bias	0.05 V, 1.0 V
Gate Bias	0 V to 1.0 V

3. Results and discussion

Presented and discussed here are the results for the impact of electron mobility variation on SCEs in nanoscale double FinFETs.

3.1. Impact of electron mobility variations on DIBL

The DIBL is defined as the difference in threshold voltage caused by increasing the drain voltage from 0.01 V to 0.05 V [41]. DIBL value can be determined using the formula stated in [42]:

$$DIBL\left(\frac{mV}{V}\right) = \frac{\Delta V_{TH}}{\Delta V_{DS}} \quad (1)$$

Where V_{TH} denotes the threshold voltage and V_{DS} denotes the drain-source voltage.
The impact of electron mobility variations on DIBL in nanoscale DG-FinFETs using GaAs, GaSb, GaN, and Si as channel materials is visualized in Figure 2. Generally, the figure demonstrates that DIBL increases with higher electron mobility in all four FinFETs. The figure shows that DIBL decreases as electron mobility increases in GaSb and GaAs FinFETs from 1000 cm^2/Vs to 2000 cm^2/Vs, thereafter it remains constant up to 10000 cm^2/Vs. This suggests minimal impact of electron mobility on DIBL within this range. This could be due to material properties. In GaN-FinFET, DIBL increases as electron mobility is increased from 1000 cm^2/Vs to 3000 cm^2/Vs after which it stabilizes between 3000 cm^2/Vs and 10000 cm^2/Vs, indicating a limited effect on DIBL. Conversely, in Si-FinFET, DIBL rises as electron mobility rises from 1000 cm^2/Vs to 3000 cm^2/Vs, drops significantly at 4000 cm^2/Vs, and remains steady up to 10000 cm^2/Vs. Si-FinFET performs better than the other FinFETs as it has the lowest DIBL value of 3 mV/V from 4000 cm^2/Vs to 10000 cm^2/Vs, while GaSb-FinFET displays the highest DIBL at an electron mobility of 1000 cm^2/Vs. Lowest DIBL value in FinFETs leads to superior device performance, energy efficiency, signal integrity, design flexibility, and reliability, making them highly desirable for a wide range of applications in the semiconductor industry.

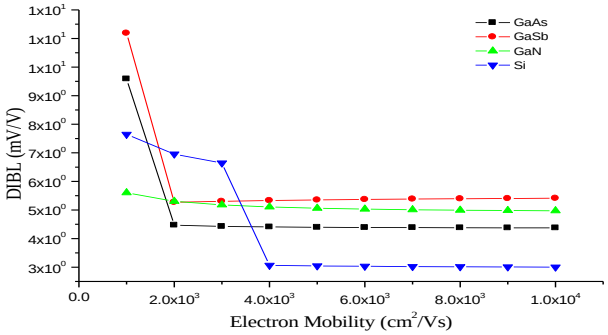

Fig. 2: DIBL vs Electron Mobility.

3.2. Impact of electron mobility variations on subthreshold swing

The subthreshold swing is the most important factor in determining leakage current. Furthermore, SS is computed using the formula [43]:

$$SS\ (mV/\ dec) = \frac{d\ V_{GS}}{d\ (log_{10}\ I_{DS}\ )} \tag{2}$$

Where V_{Gs} denotes gate-source voltage and I_{DS} denotes drain-source current.
The impact of electron mobility variations on subthreshold swing in nanoscale DG-FinFETs using GaAs, GaSb, GaN and Si as channel materials is illustrated in Figure 3. It can be observed from the figure that subthreshold swing decreases as the electron moblity increases in all the four FinFETs. The decrease in subthreshold swing with incraease in electron mobility can be explained by the improved control over the channel potential by the gate voltage due to higher mobility electrons. This allows for more efficeient modulation of the channel current, leading to a lower subthreshold swing. However, there is drastic incraese in the subthreshold swing as the electron mobility incraeses from 1000 cm^2/Vs to 2000 cm^2/Vs in GaAs-FinFETs which suggests higher leakage current between these electron mobilities. In comparison with the other FinFETs, GaN-FinFET stands out to be the best as it exhibited the lowest subthreshold swing value of 63 mV/dec at 10000 cm^2/Vs, while GaSb-FinFET is the worst in terms of SS characteristics. A lower SS enables faster switching between the on and off states of the transistor, enhancing overall device performance and responsiveness. This is advantageous in high-speed applications such as data processing and communication.

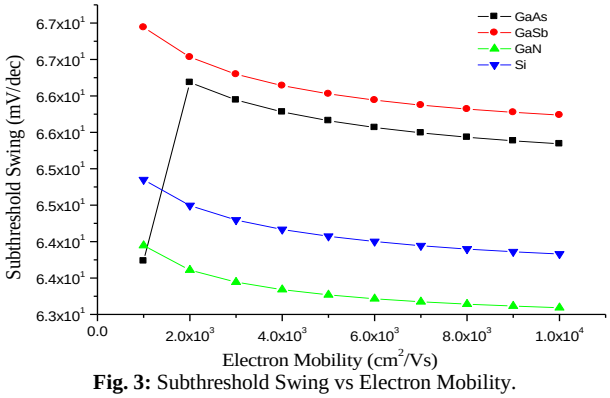

Fig. 3: Subthreshold Swing vs Electron Mobility.

3.3. Impact of electron mobility variations on threshold voltage

The threshold voltage is the gate voltage at which a transistor just begins to conduct [14]. The threshold voltage expression for a multi-gate field effect transistor (MuGFET) may be stated as [12]:

$$V_{th} = f_{ms} + 2f_f + \frac{Q_D}{C_{ox}} - \frac{Q_{SS}}{C_{ox}} + V_{in} \tag{3}$$

Where Q_{SS} denotes gate dielectric charge, C_{ox} is the capacitance in the gate, Q_D is the depletion charge in the channel, f_{ms} denotes metal semiconductor work function difference between gate electrode and the semiconductor, f_f is the fermi potential, and V_{in} is the additional surface potential to $2f_f$ that is required for ultrathin body devices to cause enough inversion charges in to the channel region of the transistor to reach threshold point.
The impact of electron mobility variations on threshold voltage in nanoscale DG-FinFETs using GaAs, GaSb, GaN and Si as channel materials is shown in Figure 3. It can be observed from the figure that threshold voltage decreases as the electron moblity increases in all the four FinFETs. When the threshold voltage decreases with increasing electron mobility, it suggests that the transistor can turn on more easily due to the improved mobility of electrons. Higher electron mobility allows for better control over the channel potential by the gate voltage, leading to a lower threshold voltage. GaN-FinFET outperforms other FinFETs in terms of threshold voltage with the lowest threshold voltage of 0.44V, at the electron mobility of 10000 cm^2/Vs while Si-FinFET is the worst in terms of threshold voltage. Lower threshold voltage in FinFET operation is essential for reducing power consumption, improving performance, enabling further scaling, facilitating operation at lower voltages, and ensuring compatibility with modern low-voltage systems.

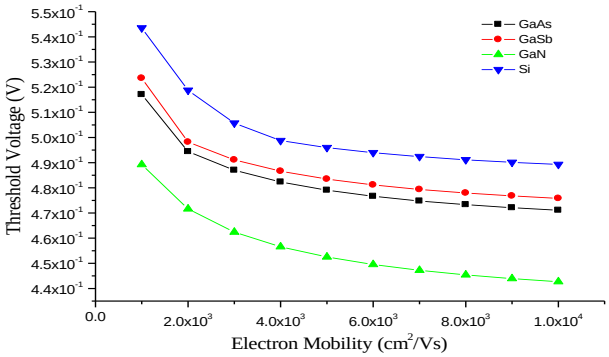

Fig. 4: Threshold Voltage vs Electron Mobility.

4. Conclusion

This work investigated the impact of electron mobility on the short channel effects in nanoscale DG-FinFET, using various semiconductor materials, namely GaAs, GaSb, GaN and Si. The study analyzed key performance metrics, including DIBL, SS and threshold voltage roll-off. The result showed that GaN-FinFET exhibited superior characteristics in terms of subthreshold swing and threshold voltage at higher electron mobility while Si-FinFET excelled in terms of drain induced barrier lowering. It can be concluded that higher electron mobility in materials plays significant role in mitigating short channel effects in FinFET devices. This finding contributes to advancing the understanding of short channel effects in nanoscale FinFETs and provides valuable insights for optimizing device performance in future semiconductor technologies. Further research can be carried out by exploring the integration of nanoscale FinFETs with emerging technologies, such as neuromorphic computing, photonic integration, or quantum computing.

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