International Journal of Engineering & Technology, 7 (1.9) (2018) 41-44

International Journal of Engineering & Technology

Website: www.sciencepubco.com/index.php/IJET

Research Paper

Design and implementation of low power encoder incorporating adaptive modulation for multi user OFDM system

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Abstract

Wireless communication system is a key element in modern uninterupted data tramsnission and reception services. In this paper, multi user Orthogonal Frequency Division Multiplexing (OFDM) system is designed with low power encoder and adaptive modualtion architectures. The proposed multi user encoder architecture is designed in Verlog HDL and simulated in Modelsim simulator. Xilinx Project Navigator is used to evaluate the performance of the proposed architecture interms of power consumptions and hardware utilizations by implementing the architecture on different virtex processors.

Keywords: *Adaptive Modulation; Low Power; Communication System; Multi User; Simulation.*

1. Introduction

OFDM plays an important role in wireless communication system. In conventional OFDM systems, single user data can be communicated to diatance location at a single time interval period. The OFDM system has the following properties as high diversity gain and high signal to noise ratio over different frequency selective and fast fading channels. Forward Error Correction (FEC) is integrated with OFDM system inorder to reduce the error rate of the symbol data transmission and reception [8]. Space diversity is adopted in OFDM system to improve the diversity properties to reduce bit error rate. The power consumption of the conventional OFDM system [9] is high which is not suitable for adavnced 4G/5G wireless communication systems. The error rate is also high due to the time varying channels. In this paper, multi user OFDM system is designed with low power encoder and adaptive modualtion architectures.

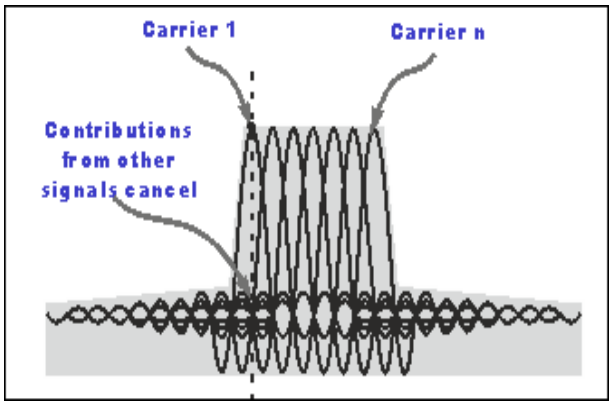

Fig. 1: Spectrum of OFDM Symbols.

Fig.1 shows the spectrum of OFDM symbolsin multi user OFDM systek which supports adaptive modualtion for low power wireless communication environment. Section II describes various conventional methodologies for OFDM design in low power applications. Section III proposes an efficient low power OFDM design technique and section IV discusses the simulation and synthesis results of the proposed architecture design. Section V concludes the paper.

2. Literature survey

Abhinav Johri et al. [2] proposed low power architecture for multi user OFDM system for improving the fitness factor. The authors used genetic algorithm for improving the fitness ratio of the proposed circuit architecture. The proposed low power architecture was applied on different hardware circuits inorder to verify the power consumption of the system. Wang et al. [1] developed low power architecture for multi user OFDM system. The authors designed and proposed their low power architecture for visible light communication system. The proposed method was constructed using simple logic gates for obtaining high efficiency and low power consumption in multi user OFDM system environment. Kalaivani et al. [4] designed low power circuit for OFDM system in area efficient methodology. The authors used Single Delay Feedback (SDF) algorithm to reduce the power consumption in FFT transformation process. The authors achieved 1053 number of slices as their proposed design implemented in FPGA processor.

Isael Diaz et al. [5] designed a low power OFDM system as receiver module for the applications of wireless local area networks. The authors achieved 239K gates and 36 mW of power consumption in 0.18 μm CMOS technology. Rajbir Kaur et al. [3] designed low power architecture for channel estimation in multi user OFDM system environment. The proposed architecture was constructed using Quadrature Amplitude Modulation (QAM) and Quadrature Phase Shift Keying (QPSK) modualtion architectures. The modulation symbols for different modulation circuits were

analyzed for error free data communication over different time varying channels.

3. Proposed system

In this paper, low power architecture for multi user OFDM system is shown in Fig. 1. The data from multi users are applied to multi user encoder which encodes the data stream into digital format which is suitable for reliable transmission through different channel environments. These encoded data are then adaptively modulated which is then applied to serial to parallel converter inorder to obtain the serial data. Then, Inverse Fast Fourier Transform (IFFT) is applied on this digital data to convert them into time domain signal. These parallel time domain signal is converted back to serial format. The cyclic code is inserted between each data which is then applied to Digital to Analog (DAC) converter. Fig. 2 (a) depicts the Multi user OFDM transmitter and Fig. 2(b) shows the Multi user OFDM receiver, respectively.

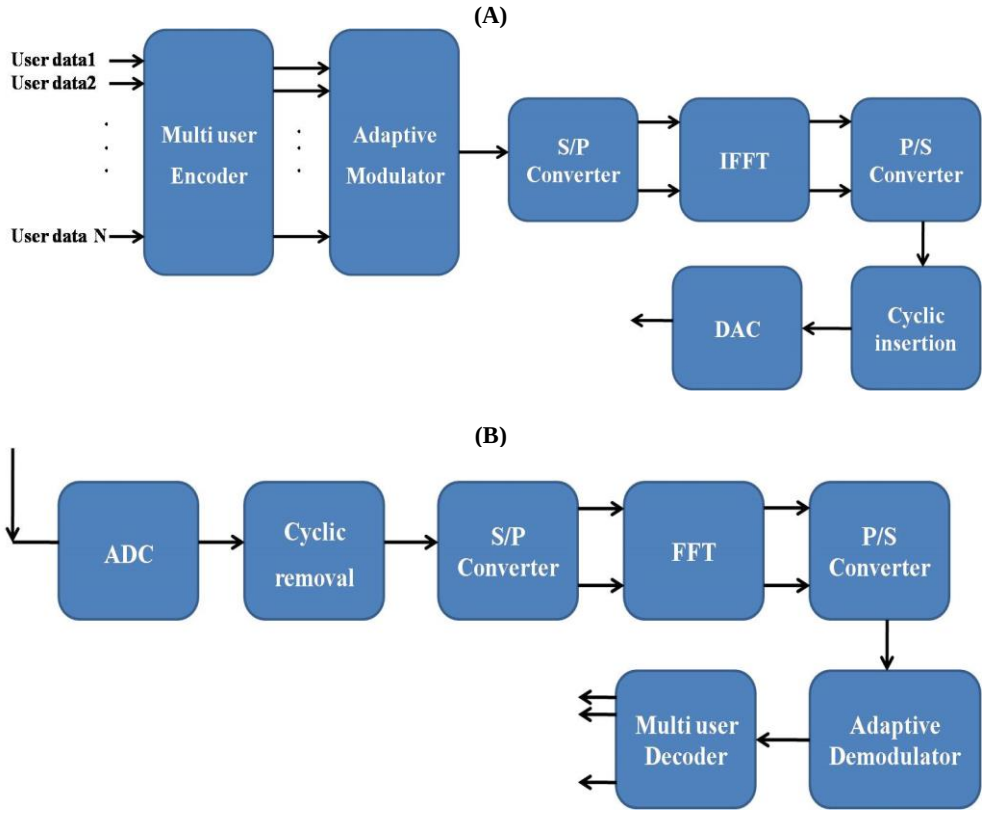

Fig. 2: (A) Multi User OFDM Transmitter (B) Multi User OFDM Receiver.

a) Low power Multi User Encoder Design

This proposed encode differ from generic encoder in the representation of single and multiple user format. The proposed encoder in this paper encodes data from different multiple users at the same time instant interval. This proposed multi user encoder consists of heuristic converter and computation blocks. The architecture of low power multi user encoder is shown in Fig. 3.

b) Heuristic converter

This heuristic converter converts the frequency domain signals into time domain signals for multi user environment. This proposed heuristic converter architecture consists of simple multiplexers and adder/subtractor units. The select lines for the multiplers and add/sub units are based on the number of ones in the data which is to be encoded. The value of select line is set to low if the number of ones in data1 is greater than the number of ones in data2. The value of select line is set to high if the number of ones in data1 is lower than the number of ones in data2. Fig. 4 shows the architecture of the heuristic converter used in this paper.

c) Computation block

The computation block is used in this paper to compute the weights of each individual user in multi user OFDM system. This block consists of simple XNOR gates which can be intergrated inorder to obtain the low power multi user encoder circuit in multi user OFDM system. The responses from various computation block units are integrtaed into single vector using multiplexer logic. The proposed architecture for computation block is illustrated in Fig. 5.

d) Adaptive Modulation

In conventional methodology, fixed modulation architecture is incorporated with conventional encoder in OFDM system for single user environment. The Bit Error Rate (BER) of the conventional modulation architecture is high due to varying channel environments. Hence, adaptive modualtion format is implemented with conventional encoder system which adaptively modulates the encoded signals based on the BER. In this proposed methodology, low end and higher end modulation architectures are integrated with proposed multi user encoder architecture which adaptively changes the modulation architecture. The lower order modulation architecture is prefered for worst channel environments (non linear variation in time varying channel environment) and higher order modulation architecture is prefered for non-worst channel environments (linear variation in time varying channel environment).

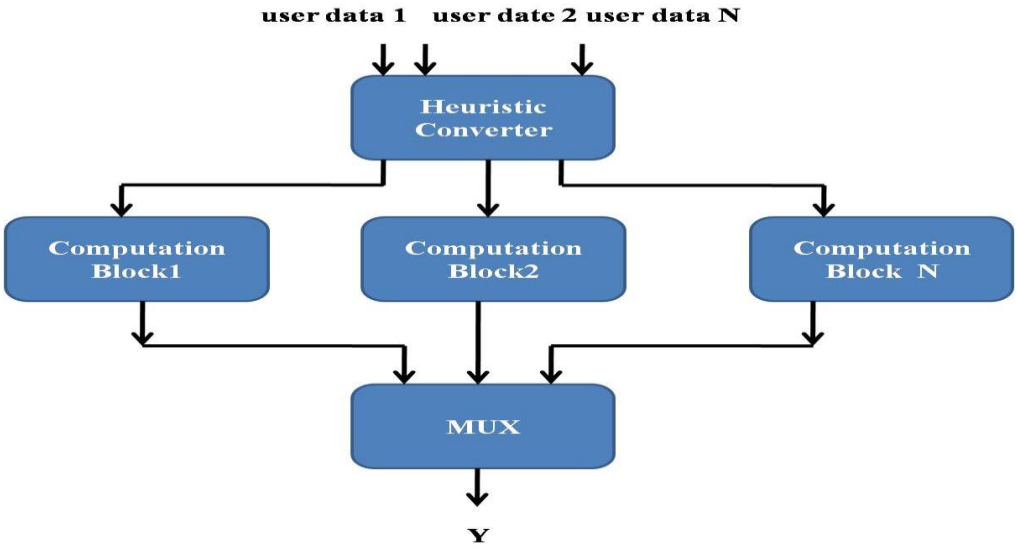

Fig. 3: Low Power Multi User Encoder Architecture.

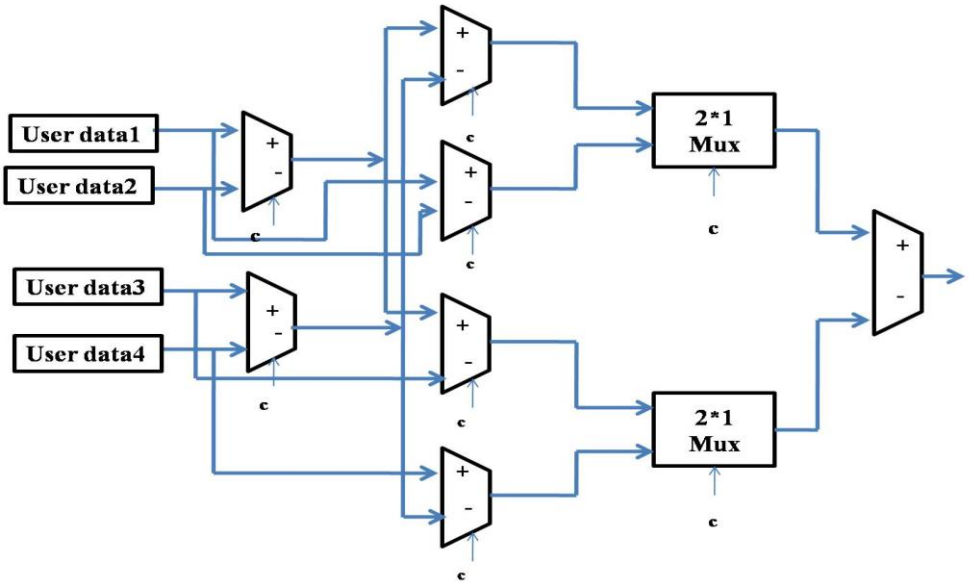

Fig. 4: Architecture of Heuristic Converter.

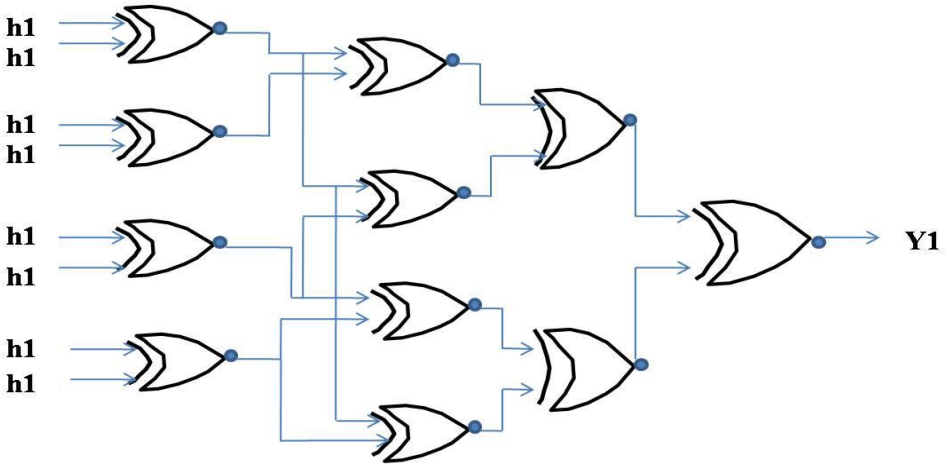

Fig. 5: Architecture of Computation Block.

4. Results and discussion

In this paper, Modelsim 5.8e simulating software is used to simulate the proposed system architecrure. Xilinx Project Navigator 12.1i synthesis software is used to synthesize the proposed system architecture.

Table 1: Hardware Consumption of the Proposed Architecture

Performance parameters	Proposed Architecture
Slices	124
LUTs	586
Gate Counts	1296
IOBs	47

Table I shows the hardware consumption of the proposed architecture interms if slices, LUTs, gate counts and IOBs. The proposed system architecture consumed 124 numbers of slices, 586 numbers of LUTs, 1296 number of gates and 47 numbers of IOBs.

Table 2: Analysis of Latency

Methodology	Latency(ns)	CMOS technology	Frequency (MHz)
Proposed	7.19	45nm	200
Ismail et al. (2013)	12.75	65nm	300
Zhang et al. (2017)	16.53	180nm	300

Table II shows the latency of the proposed encoder and conventional methods. The proposed method achieves 7.19 ns of latency with 200 MHz clock frequency on 45 nm VLSI technology. Conventional methods as Ismail et al. [6] achieved 12.753 ns of latency and Zhang et al. [7] achieved 16.535 ns of latency for encoder design in OFDM system.

Table 3: Performance Analysis of Power Consumptions on Various Virtex Processors

Family	Device Specifications	Power Consumption (mW)
Virtex	XCV50	27 mW
Virtex 2	XC2V40	29.18 mW
Virtex 2P	XC2VP2	32.97 mW

Table III shows the performance analysis of power consumptions on various Virtex processors. The proposed architecture consumed 27 mW of power on XCV50 Virtex processor, 29.18 mW of power on XC2V40 Virtex 2 processor and 32.97 mW of power on XC2VP2 Virtex 2P processor.

Table 4: Analysis of Quiescent Voltages on Different Virtex Processors

Virtex family	Virtex	Virtex 2	Virtex 2P
Quiescent V_{ccint} 1.20V	17 mA	19 mA	21 mA
Quiescent V_{ccaux} 2.50V	19 mA	23 mA	26 mA
Quiescent V_{cco25} 2.50V	12 mA	14 mA	24 mA

Table 5: Performance Comparisons of the Proposed Architecture

Methodology	Power Consumption (mW)
Proposed	27
Ismail et al. [6]	65
Zhang et al. [7]	46

**Code rate is 0.96 (15, 7) and word length is 7 bits with 8 iterations.

Table V shows the performance comparisons of the proposed encoder design in OFDM system with conventional system designs. The proposed architechture consumes 27 mW of power consumption while conventional methods as Ismail et al. [6] consumed 65 mW of power consumption and Zhang et al. [7] consumed 56 mW of power consumption. Table VI illustrates the performance analysis of proposed system interms of BER. The BER is defined as the ratio between number of correctly received bits and the total number of bits transmitted at the transmitter section.

Table 5: Performance Analysis of Proposed System in Terms of Ber

Channel environment	BER	
	Proposed system	Ismail et al. [6] (2013)
Linear	$0.073*10^{-3}$	0.975310^{-3}
Non-linear	$0.073*10^{-2}$	$0.173*10^{-3}$

5. Conclusions

Recent wireless communication system requires low power operated devices. In this paper, low power multi user OFDM system is designed which consumes low power due to the low complexity of the encoder architecture. The performance analysis interms of power consumptions and hardware utilizationson are carried out on different Virtex processors. The proposed multi user OFDM architecture consumed 27 mW of power on XCV50 Virtex processor, 29.18 mW of power on XC2V40 Virtex 2 processor and 32.97 mW of power on XC2VP2 Virtex 2P processor.

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