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Research paper

Low power and high fault coverage SIC reseeding TPG using x-filling techniques for Scan BIST

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Abstract

We proposed an optimal single input change (SIC) generator with pre-selected seed values using X filling techniques such that don't care are reseed and Xored with SIC generated value. SIC generator generates patterns with minimum switching activity and X filling techniques used to detect faults to achieve high fault coverage, in conventional methods high fault coverage obtained by increasing numbers of patterns. The novelty of proposed method is a minimal number of patterns target on the large number of fault sets achieved high fault coverage, this paper also focused on testing time to improve yield and performance of the circuits. Full scan based DFT tool Tessent is used to calculate various parameters. The results are very effective. This approach decreases the transition activity, increases the fault coverage and reduces test time up to 83% with respect to deterministic LFSR. The tool used Mentor Graphics' Tessent. Full scan insertion and DRC violation is done by DFT Advisor and DFT Visualizer respectively. We have tested the ISCAS 85'&89' and compared with conventional LFSRs.

Keywords: *Low Power Scan BIST; Sicreseedingtpg; Fault Coverage; Switching Activity; ISCAS'85 and 89 Benchmark Circuits.*

1. Introduction

Scan based techniques for minimizing shift and capture power during scan testing without any lose of fault and test coverage. This can be achieved by proper selection of seed value in test pattern generators. Fill techniques play a major role in power aware ATPG [3], The goal of X-filling algorithm is to minimize the Hamming distance between primary inputs and primary outputs, which can be implemented using zero fill and One fill techniques, In zero fills don't care are filled with logic zero and in one feel, don't care are filled with logic one. Different approaches have been proposed in selection of seed values, in [1] presents AB-filling algorithms are used to reduce capture power while feeding the first test patterns to the benchmark circuit, where in [3] focused on both shift power and capture power in test application using CSP filling techniques, Bhavsar proposed to don't care filling techniques for optimization of scan power and also focused on compression of data [2]. In [4] Lee proposed SIC based LFSR where the seed generator replaces with modified LFSR. According to to the survey we have done on the work accomplished in DFT techniques, until now, many methods were applied to scale down the power consumption during the test process. These Incorporate XOR based LFSR, which is a standard LFSR used as a test pattern generator for an appropriate power reduction of 46% during the test process [5]. BF-LFSR has been used as a test pattern generator for a power reduction of 74.89% during test procedure. In this method [BF], the correlation of the adjacent bits of the patterns generated has been increased in order to reduce the switching activity thereby reducing overall power dissipation

A technique to reduce more power consumption compared [6]&[7] SIC-BF-LFSR[8] is proposed in which the output patterns of BF-LFSR are XORed with converted Grey level patterns of a n-bit counter pattern generator to increase the correlation of the bits in the pattern thereby resulting in high-power reduction. In [14] it is proposed that a new (combinational) ATPG algorithm that reduced switching activity between successive test vectors during test application. The objective of the ATPG was to ensure that switching activity during test application was low enough to ensure safe and nondestructive at-speed testing. The new ATPG algorithm reduced average heat dissipation between successive test vectors. The proposed algorithm was implemented on ISCAS‟85 benchmark circuits and the results demonstrated that the tests generated decreased the average number of weighted transitions between successive test vectors, and fault coverage is also focused in [15], in this proposed method, two LFSRs are used one isslow LFSR and other is normal speed LFSR. The inputs of the circuit under test were provided through the slow LFSR in order to reduce the transition density at the inputs, which resulted in reduced heat dissipation during the test. A procedure was introduced to design a DS-LFSR such that high fault coverage was achieved through unique and uniformly distributed patterns. New methods of selecting inputs driven by the slow LFSR and increasing the number of inputs driven by the slow LFSR were presented, reduces of 13% to 70% in the number of transitions were observed for ISCAS benchmark circuits without loss of fault coverage using this method... In above all approaches used either modification of LFRS or changing seed values done independently, In our approach. We try to use both concepts of SIC generator that is modifying LFSRand also seed generators replace with X-filling techniques to present our TPG more effective in terms of reducing both shift and capture power, and also we reduce test application time up to 83% compared with conventional methods.

This paper is organized as follows in section II specifications of different ISCAS sequential and combinational benchmark circuits are tabulated. In section, III explains calculation of switching activity; transition density and power dissipation are analyzed. In Section IV described proposed architecture using X-filling tech-

niques. Result analysis and obtained results are specified in section V; the paper is concluded in Section VI.

2. Specifications of CUT's

The International Symposium for Circuits and Systems (ISCAS) has designed certain circuits called as the benchmark circuits that are extensively used in Design for Testability. The benchmark circuits when used in the BIST architecture as the Circuit under Test (CUT) help to clearly analyze the efficiency of a Test Pattern Generator used in testing. These benchmark circuits are both combinational (ISCAS'85) and sequential (ISCAS'89), some of the benchmark circuits are c17, c432, c499, C3540,s27, s271, s298 and s344 and s349.
In this paper, different benchmark circuits are compared by specifying their primary inputs, primary Outputs and the number of logic gates in design of each circuit. The specifications are represented in table 1.

Table 1: Specifications of Benchmark Circuits

Circuit type	Combinational				Sequential				
Name of Circuit	C432	C17	C499	C3540	S27	S271	S298	S344	S349
PI's	36	5	41	50	9	7	8	14	14
PO's	7	2	32	22	2	2	7	12	12
Number of Gates	235	15	261	1669	49	47	195	245	259

3. Switching activity and power dissipation

Switching Activity represents the transitions in the bits of the input test vector. It is defined as the measurement of change in values of a signal. The switching activity is important for the following reasons.

- Essential to measuring power in digital circuits
- Optimizing digital designs
- Can have a direct effect on quality of results

3.1. Transition density

Transition Density is defined as the average switching rate at a circuit node. Transition Density can also be called as Signal activity or Node Transition factor (TD).
Transition Density is given as
TD = Total no. of bit transitions/Total no. of bits
The algorithm to calculate switching activity and transition density is as follows:
Step 1 - Begin (for an n-bit LFSR)
Step 2 - Write the Transition matrix [A]
Step 3 - Find the number of one's in the sequence
Step 4 - Find the size of the matrix mentioned in step 2
Step 5 - Check whether the LSB and MSB bits are either 0/1
Step 6 - Calculate the Switching Activity based on different sets of LSB and MSB
Step 7 - End
The above procedure to calculate switching activity and Transition density is briefly summarized in the form of a flowchart.

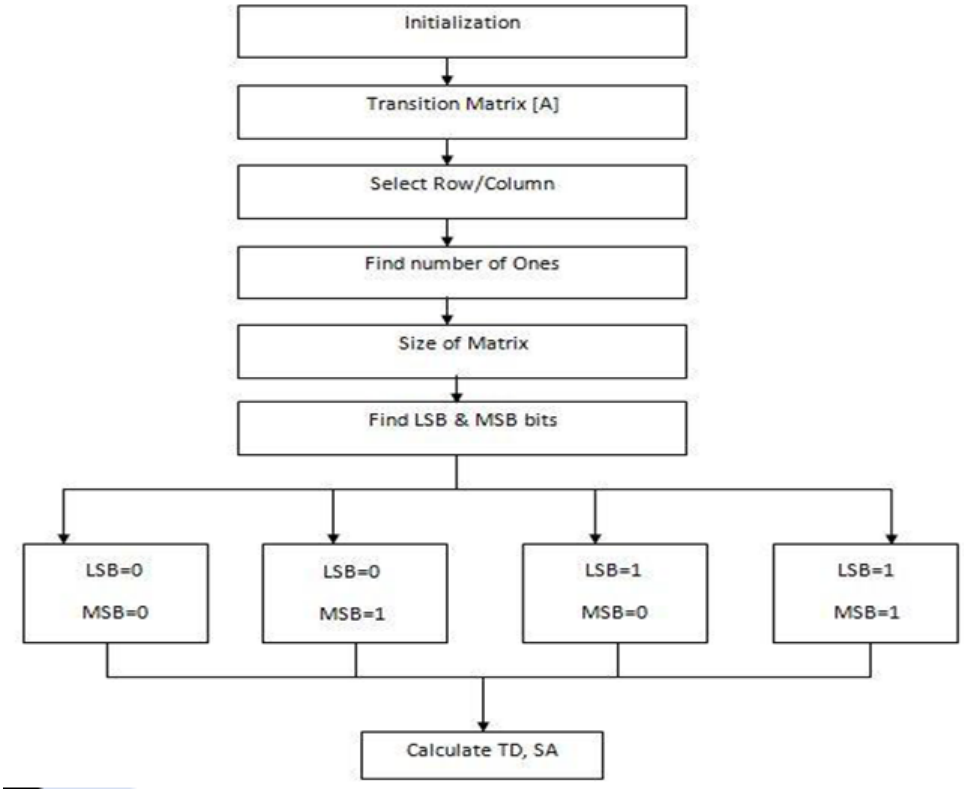


Fig. 1: Flowchart to Calculate Switching Activity.

The Switching activity for three types of Test pattern generators is calculated and the resulting number of transitions is represented in Table2 and graphical representation is also shown

Table 2: Switching Activity (SA)

TPGs	LFSR	Bit-Flipping	X-filling
Switching Activity	80	64	31

The number of transitions in the patterns generated by LFSR is shown very high compared to BF LFSR and SIC LFSR. Hence the SA is also increased with respect to number of transitions as a result the power dissipation willalso be more for LFSR compared to other two LFSRs. The relation between power dissipation and switching activity can be shown as
The main reasons for the power dissipation during testing are given below.

- According to the Moore's Law, the transistor density increases after every 18 months. Hence, circuits become more complex and difficult to test. It takes more time to test these circuits, and to save the testing time; partitioning of the circuits is required, which leads to high-power dissipation.
- Due to lack of at-speed equipment's, delay is introduced into the circuit during testing, which also dissipates power. In the testing mode, the correlation between the consecutive patterns is small, which causes large switching and hence increases the dynamic power.
- In normal mode, only a small part from the SOC works but in the test mode, all blocks of the SoC remain engaged by applying the large number of test patterns one after the other. Hence, test mode requires more power than the normal mode and responsible for increasing chip temperature.

4. Architecture of proposed TPG

Single Input Change Bit Flipping linear feedback shift register (SIC BF-LFSR) is used as a proposed test pattern generator,the architecture[2] shown in Fig 4 below consists of a seed generator (BF), an n-bit counter, a gray encoder and an exclusive-OR array. The n-bit counter and gray encoder generate single input changing patterns. C [n-1:0] is the counter output and GC [n-1:0] is the gray encoder output. The counter and BF are controlled by test clock TCK. The initial value of the n-bit counter is all zeroes, and it generates 2n continuous binary data periodically. The output of NOR operation of C [m-1:0] will be the clock control signal of BF where m<=n. It can be found obviously that BF will generate the next seed only when C [m-1:0] are all '0' and NOR output changes to '1'. The period of the single input changing sequences will be 2m.

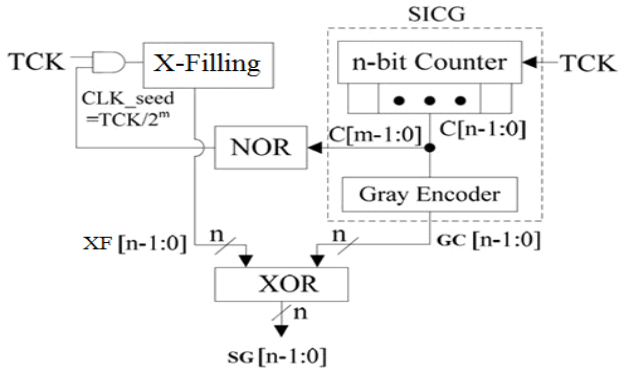


Fig. 3: Architecture of SIC BF LFSR.

Gray encoder in Fig.5.1 is used to encode the counter's output C [n-1:0] so that two successive values of its output GC [n-1:0] will differ in only one bit. Gray encoder can be implemented by following equations.

GC [0] = C [0] XOR C [1]

GC [1] = C [1] XOR C [2]

GC [2] = C [2] XOR C [3]

…

GC [n-2] = C [n-2] XOR C [n-1]

GC [n-1] = C [n-1]

The seed generating circuit BF is modified LFSR structure to apply swapping between the neighboring bits. The last bit is the selection line for the swapping process. If the last bit is '0', then swapping is performed, else nothing will change.
The final test patterns are implemented as following equations.

SG [0] = BF [0] XOR GC [0]

SG [1] = BF [1] XOR GC [1]

SG [2] = BF [2] XOR GC [2]

…

SG [n-1] = BF [n-1] XOR GC [n-1]

The BF's clock will be TCK/2m due to the control signal.
As SICG's cyclic sequences are single input changing patterns, the XOR result of the sequences and a certain vector must be a single input changing sequence too.

5. Result analysis

Tessent Scan generates and adds the most effective scan architecture for your design, ensuring high-quality test with automatic test pattern generation (ATPG). It performs scan flop replacement and stitching, analyzes your circuit for possible test limitations, does test-related design rule checks (DRCs), and automatically corrects errors.
The Tessent Scan and ATPG course will drive the development of your skills and knowledge in scan and ATPG design utilizing the Tessent Scan, Tessent Fastscan, and the DFT Visualizer. The knowledge gained for generating test patterns in this class is directly applicable for generating test patterns for designs utilizing Tessent Test Kompress. ModelSim is used to simulate test patterns to identify potential issues (mismatches) between the expected results from pattern generation and the Verilog simulation results. During this course, you will insert full scan in a design using Tessent Scan, and create high-quality test patterns using the ATPG.
In this tool for scan insertion, DFT ADVISOR is used and for DRC of violations any occurred DFT Visualizer is used and for Fault Coverage analysis FASTSCAN is used.

Table 3: Design Specifications.

Technology size / Library	TSMC 180nm CMOS/adk.atpg
DFT	Full Scan based BIST
TPG	SIC LFSR
CUT	ISCAS' 85 and 89
Fault Type	SA_0 and 1
Tool Usage	Mentor Graphics Tessent

5.1. DFT advisor and fastscan

DFTAdvisor is a utility that allows you to insert scan circuitry into your design. It follows one of two basic strategies: The first is full scan. Full scan converts every flip flop and latch into scan able flip flops, which allows the use of combinational test pattern generation. . After inserting the scan circuitry, you can then generate test vectors for your design by using Fastscan, the other strategy is partial scan. With partial scan you only insert scan circuitry in some of the memory devices.

5.1.1. Invoking DFT advisor

Invoke: - dft advisor –verilog c432.v –lib adk.atpg
Implement scan with defaults (full scan, mux-DFF elements):

- Set system mode setup
- Analyze control signals –auto
- Set system mode dft
- Run
- Insert test logic
- Write netlist c432_scan.v –verilog
- Write atpg setup c432_scan

5.1.2. Invoking fast scan

Invoke: fastscan –verilog c432_scan.v –lib adk.atpg
Generate test pattern file:

- Dofile c432_scan.dofile (defines scan path & procedure)
- Set system mode atpg
- Create patterns –auto
- Save patterns

5.2. Statistic reports

Table 4: Statistics Reports

Statistics Report C17 Stuck-at Faults	
Fault Classes	Faults (total)
FU (full)	44
DS (det_simulation)	44 (100.00%)
Coverage	
Test_coverage	100.00%
Fault_coverage	100.00%
atpg_effectiveness	100.00%
Test_patterns	7
Simulated_patterns	32
CPU_time (secs)	0.2

Statistics Report C432 Stuck-at Faults	
Fault Classes	Faults (total)
FU (full)	1078
DS (det_simulation)	1065 (98.79%)
RE (redundant)	13 (1.21%)
Coverage	
Test_coverage	100.00%
Fault_coverage	98.79%
atpg_effectiveness	100.00%
Test_patterns	63
Simulated_patterns	80
CPU_time (secs)	1.4

The results obtained from Tessent Fastscan, targeted on generated netlist of c17 combinational design as a input and is converted to scan inserted netlist for applying as a input to generate statistic report of the design. Results of some targeted ISCAS'85&89 benchmark circuits are simulated and the simultaneous results are represented in Figs 5&6.

5.3. Fault coverage and test coverage of ISCAS 85' and 89' circuits

In the fig 6.1 the Fault coverage and Test coverage are compared and here the Fault Coverage is not that much higher when deterministic LFSR is used as a test pattern generator (TPG). The patterns are generated deterministically and are not much pseudo random in order to increase the Fault coverage and also Switching Activity (SA) is also high thereby increasing the power consumption. In this case the patterns are generated by using a different Test Pattern Generator and the the patterns generated are given as input in FastScan Tool to simulate the Fault coverage (FC) and Test coverage (TC).

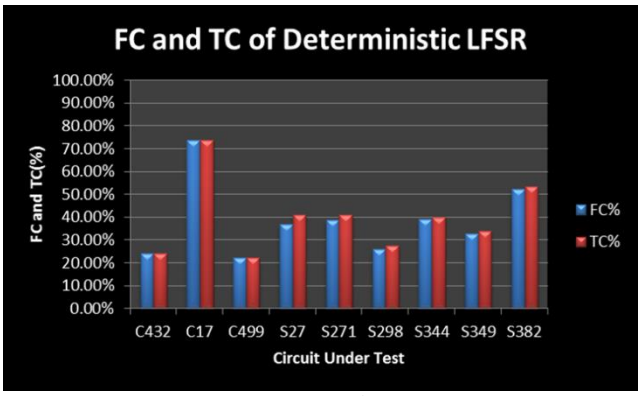


Fig. 4: Comparison of FC and TC.

5.4 Improved fault coverage and test coverage of ISCAS 85' and 89' circuits by using SIC-LFSR test pattern generator TPG

The proposed paper is focused on this type of result with improved statistic report and FC. The Fig 6 shows the Fault Coverage and Test Coverage of CUT's obtained by using Single Input Change LFSR test pattern generator. By using SIC LFSR as a TPG the results are improved upto a Fault Coverage (FC) and Test Coverage (TC) of 100% and the Switching Activity is also reduced thereby decreasing the Power consumption as it generates Pseudo random patterns.

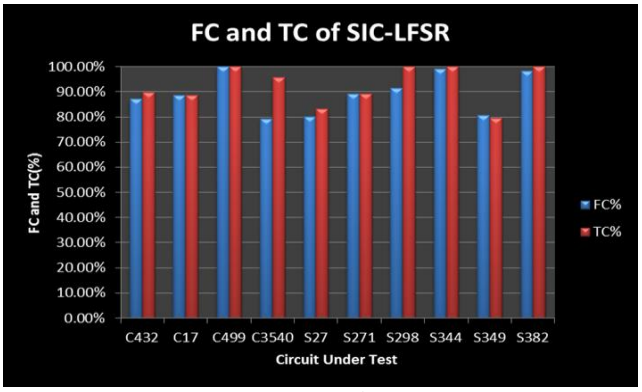


Fig. 5: Comparison of FC and TC.

5.5. Parametric results

There are different kind of Parameters that are to be considered for better analysis and to observe the progress. Some of the parametric results are analysed and represented in this project. In Table 6.1&6.2 different parameters are shown like Number of Patterns, ATPG effectiveness, Total Faults inserted and CPU time. A deep comparison can be made between the two proposed LFSR's by using these parameters.

5.5.1. Deterministic LFSR

Table 5: Parametric Results for Deterministic LFSR

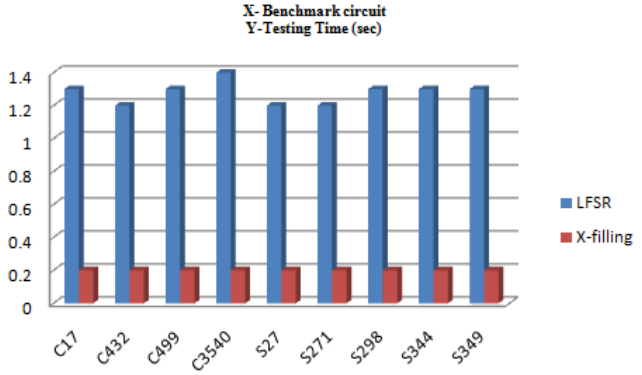
Name of the circuit	C17	C432	C499	C3540	S27	S271	S298	S344	S349
FC%	73.68	23099	22.26	59.27	36.84	38.89	25.91	38.95	32.96
TC%	73.68	23.99	22.26	85.65	41.18	41.18	27.29	39.69	33.85
No. of Patterns	6	14	6	80	3	5	5	4	3
ATPG Effectiveness%	100	100	100	100	100	100	100	100	100
No of Faults	38	888	552	5642	76	412	552	534	534
CPU Time	1.3	1.2	1.3	1.4	1.2	1.2	1.3	1.3	1.3

5.5.2. SIC – LFSR

Table 6: Parametric Results for SIC-LFSR

Name of the circuit	C 17	C4 32	C4 99	C35 40	S2 7	S2 71	S2 98	S3 44	S3 49
FC%	10 0	87. 11	10 0	79.2 7	80. 19	89. 22	91. 35	99. 12	80. 60
TC%	10 0	89. 89	10 0	95.6 5	83. 33	89. 22	100	100	79. 43
No. of Patterns	7	55	55	187	6	8	35	36	26
ATPG Effective-ness%	10 0	100	10 0	100	100	100	100	100	100
No of Faults	44	970	12 14	762 8	106	102	636	682	688
CPU Time	0. 2	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2

5.5.3. Analysis of processing time



Here in the Fig 6.3 it can be seen that the CPU time drastically reduced when compared to Deterministic LFSR and thereby it is much faster to calculate fault coverage and other parameters when compared to conventional methods.

6. Conclusion

This paper presented the design and analysis of SIC Reseeding TPG for Logic Built-in Self-Test. The Low Transition technique is general and can be applied to almost all Test Pattern Generators. Among all the LFSR's SIC-LFSR with X-filling will be having the lowest power consumption while testing the Circuit under Test. Our method for Low Power is based upon reducing the number of transitions. Transitions are reduced by applying XOR Gate between n-counter bits converted to Grey level codes and the seed generated from X-filling techniques. SIC-LFSR is independent of circuit under test and flexible to be used in both BIST and scan-based BIST architectures, the Fault coverage is achieved for ISCAS Benchmark Circuit's by using Deterministic LFSR & SIC LFSR. Fault Coverage achieved for all ISCAS Benchmark circuits is above 95% and improved CPU processing time up to 83%.

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