International Journal of Engineering & Technology, 7 (1.5) (2018) 209-216

International Journal of Engineering & Technology

Website: www.sciencepubco.com/index.php/IJET

Research paper

MATLAB/simulink study of multi-level inverter topologies using minimized quantity of switches

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Abstract

Multilevel Inverters (MLI) have very good features when compared to Inverters. But using more switches in the conventional configuration will reduce its application in a wider range. For that reason a modified 7-level MLI Topology is presented. This new topology consists of less number of switches that can be reduced to the maximum extent and a separate gate trigger circuit. This will reduce the switching losses, reduce the size of the multilevel inverter, and cost of installation. This new topology can be used in Electrical drives and renewable energy applications. Performance of the new MLI is tested via. Total harmonic distortion. This construction structure of this multilevel inverter topology can also be increased for 9-level, 11-level and so on and simulated by the use of MATLAB/SIMULINK. A separate Carrier Based PWM Technique is used for the pulse generation in this configuration.

Keywords: *Multilevel Inverter, Conventional Cascaded MLI, PWM, Level Shifting PWM.*

1. Introduction

Multilevel Inverters (MLIs) can be used in medium and high voltage applications for example in renewable energy sources, industrial drives, blowers, fans, laminators and conveyor systems. Small voltage steps in MLIs results in withstanding proficient voltage, minimal harmonics, enhances the electro-magnetic compatibility, eliminated the on/off losses, and excellent power quality [1-7].

Cascaded MLIs, Diode-Clamped MLIs, Flying Capacitor MLIs are the different types of MLIs types that have been developed so far. It is mentioned that simplicity is the main advantage of the Cascaded MLI. But increase in levels will increase the number of switches. Hence it is a contradictory in case of Cascaded MLI. Then arises the concept of "switch reduction". So Cascaded Multilevel Inverter has undergone many researches and still new trends have been introduced in the evolution of renewed Multi level inverters. Cascaded CMLI consists of 12 switches for getting 7-level output. Later 9-switch 7-level topology is introduced by eliminating three power ON/OF devices from the main Conventional CMLI. Then the configuration has been modified by reducing another 2 switches hence getting 7-switch 7-level configuration. And on later another new topology is constructed by reducing one switch that is 6-switch 7-level topology [8-15].

For the concept of decreasing the switches to optimal likely extent and suppressing the difficulty, a new topology is presented using five switches. This is the least possible reduction for a 7-level MLI. This 5-switch 7-level topology is a special arrangement with 4-DC input voltage sources.

Decrease in the quantity of switches will suppress the on/off losses and the cost of the circuit construction is also reduced. The performance of the designed model is verified by various fixed switching Frequency PWM i.e PD, POD, APOD PWM techniques using MATLAB/SIMULINK.

2. Level shifting carrier based PWM

PWM technique is applied for the purpose of Pulse generation. Among all the PWM techniques Carrier-Based technique is the easy one. It is again divided into Level and Phase shifting CBPWM's. Phase shifting CBPWM generates large harmonics when compared to the Level shifting CBPWM. Hence, Level Shifting CBPWM is applied in this designed system for pulse generation. This Level shifting CBPWM is again divided into 3 types [16-19]. They are

A. Phase disposition PWM

In this PWM technique, N-1 carrier signals are used for the generation of N output voltage levels. All the carrier signals are equal in magnitudes, having same frequency and are in phase. In this PWM method, sine reference signal is compared with the vertically shifted triangular carrier signal.

B. Phase opposition disposition PWM

In this POD PWM method, entire triangular carrier signals upward the origin axis is having the same frequency/ amplitude and in phases with one each other. In the same way, the entire carrier signals downward the origin axis is having the same frequency/magnitude and all are in phase with each other. Still, the carrier signals upward the origin axis is phase shifted by 180 degrees when compared to the carrier signals downward the origin axis.

C. Alternative phase opposition disposition PWM

APOD PWM method, entire triangular carrier signals are having the same/amplitude. Hence, each and every carrier signal is shifted by phase of 180 degrees when compared to each other.

3. Proposed 5-switch 7-level topology

This 5-switch 7-level topology is the redesigned structural configuration of the six switch topology by removing one switch reaching the five switch model. Compared to the conventional configuration and existing topologies, this 5-switch structure is the simplest design. This topology consists of 4 DC input voltage sources for 7 levels, 5 DC input voltage sources for 9-levels and 6 DC input voltage sources for 11 levels and so on.
The General expression for level number of output voltage is

L=(2*S-3),
Where L=no.of o/p voltage levels
S=no.of switches
L=(2*Vdc-1)

Where Vdc=no.of DC Input Voltage sources
sole pulse pattern of triggering the switches at proper instants, the design of PWM generation makes the circuit differ from other topologies. In this configuration, switches S1, S2, S3 must be unidirectional in order to avoid the distortions in the output waveform. Reducing the number of switches will make the circuit user friendly and compact. Switch reduction benefits in the lowering of switching losses. In this configuration H-Bridges are not used. The switches S4 and S5 are used for the purpose of polarity reversal. In Table-1 switching operations of switches are mentioned by 0 and 1. 0 indicates OFF state and 1 indicates ON state.

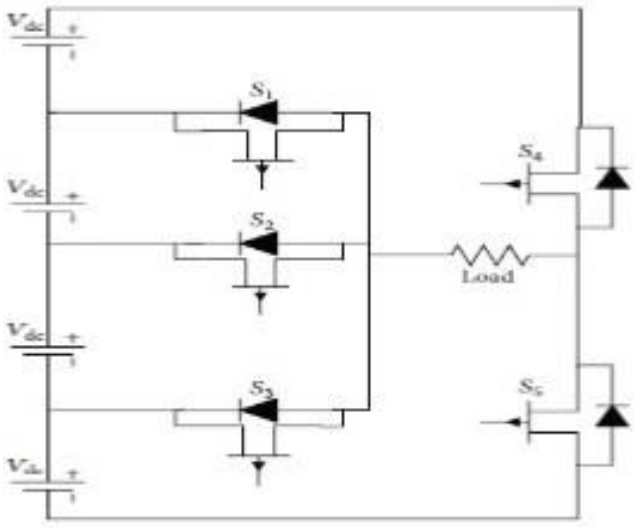
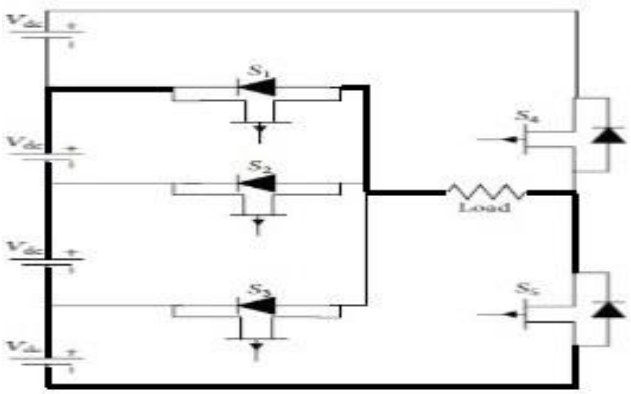
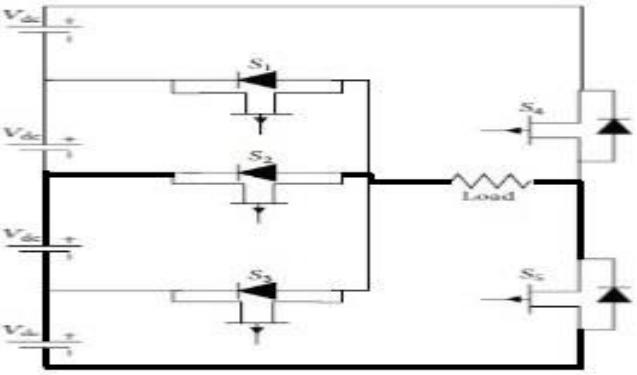


Fig. 1: 5-Switch 7-Level Topology

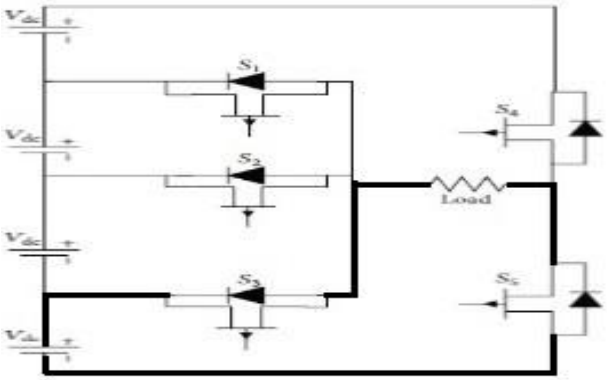
A. Modes of Operation



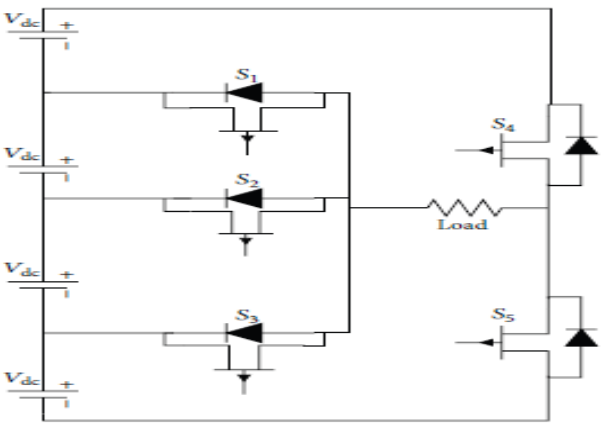
state-1



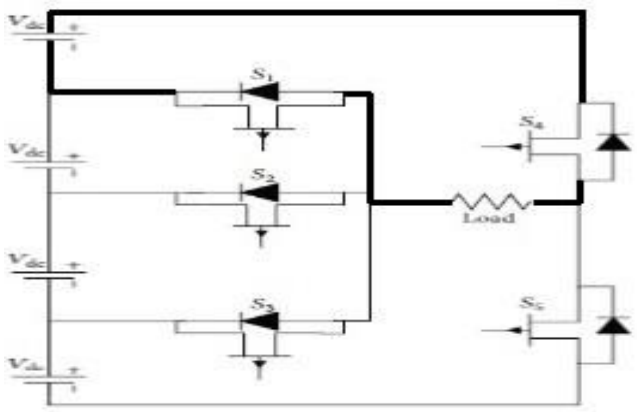
Mode-2



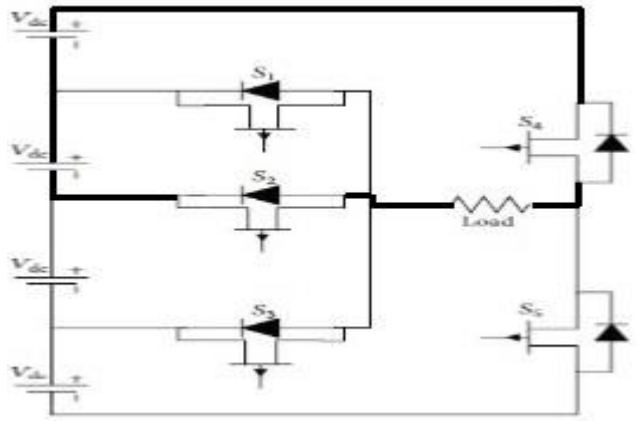
state-3



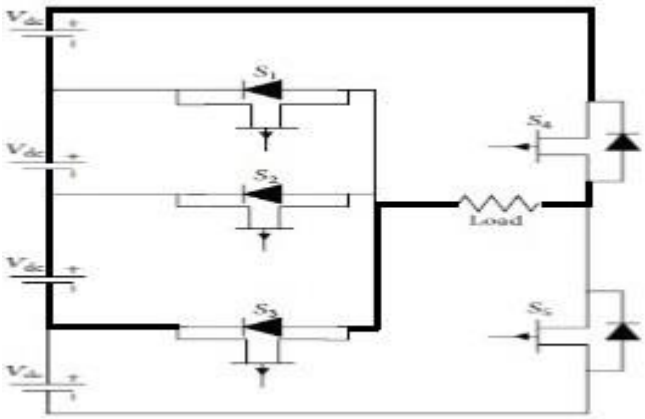
state-4



state-5



state-6



state-7

Table 1: Switching Topology of 5-Switch 7-Level MLI

Sl.No	S1	S2	S3	S4	S5	o/p Voltage
a	0	0	1	0	1	+1Vdc
b	0	1	0	0	1	+2Vdc
c	1	0	0	0	1	+3Vdc
d	0	0	0	0	0	0
e	1	0	0	1	0	-1Vdc
f	0	1	0	1	0	-2Vdc
g	0	0	1	1	0	-3Vdc

4. Simulation circuit

B. 5-Switch 7-Level MLI

The new topology circuit of 7-level MLI is constructed by the use of 5 MOSFET switches and 4 DC voltage sources. Among these 5-Mosfet Switches, 3- MOSFET switches are connected in between the 4 DC voltage sources and the remaining 2- MOSFET switches are used for the polarity reversal mechanism. Each DC input voltage values are 10V DC. Here Resistive load is used whose value is 10Ohms. The MOSFET block parameters are

FET resistance=0.01 Ohms
Internal diode resistance = 10 Kilo Ohms.

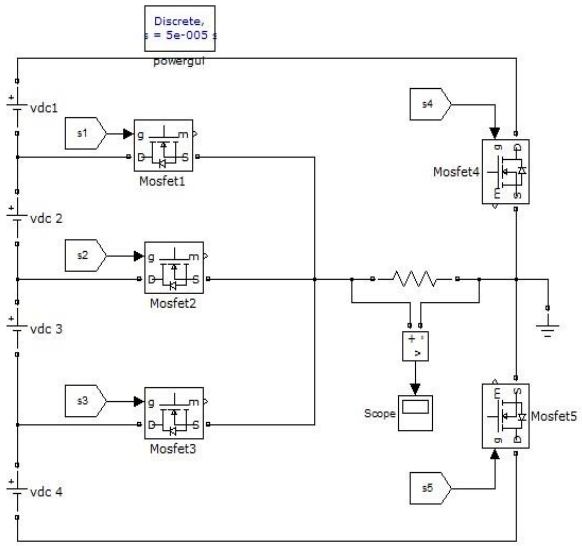


Fig. 2: Simulation circuit for 5-Switch 7-Level Topology

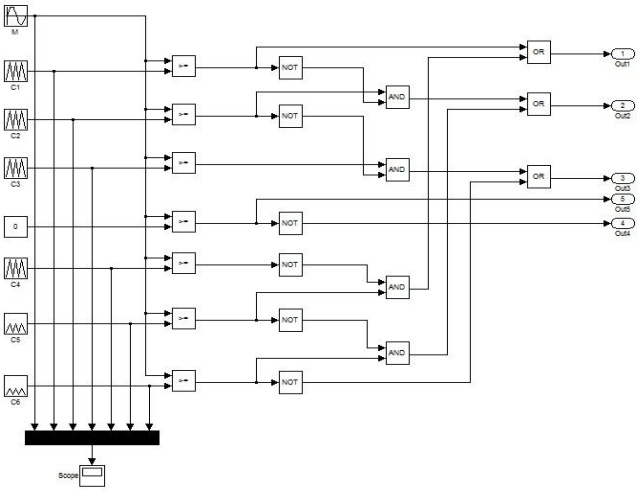


Fig. 3: Sub Circuit for 7-level MLI

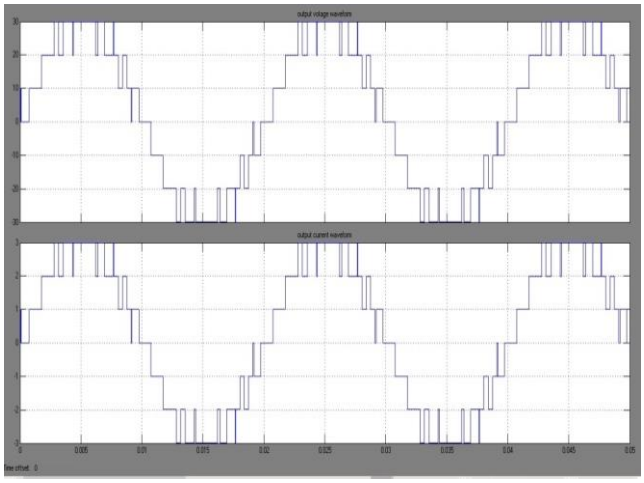


Fig. 4: Output voltage and current waveforms for 7-level MLI

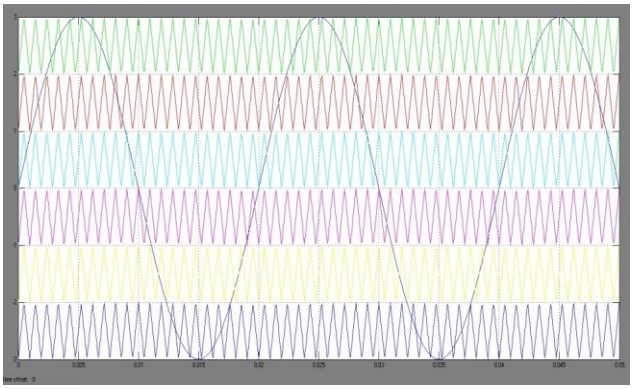


Fig. 5: PD PWM for 7-Level MLI

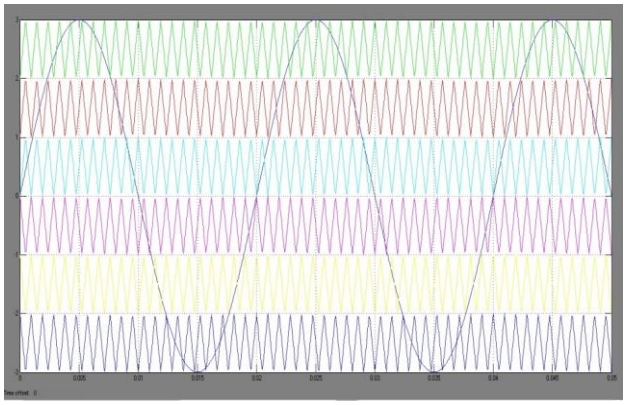


Fig. 6: POD PWM for 7-level MLI

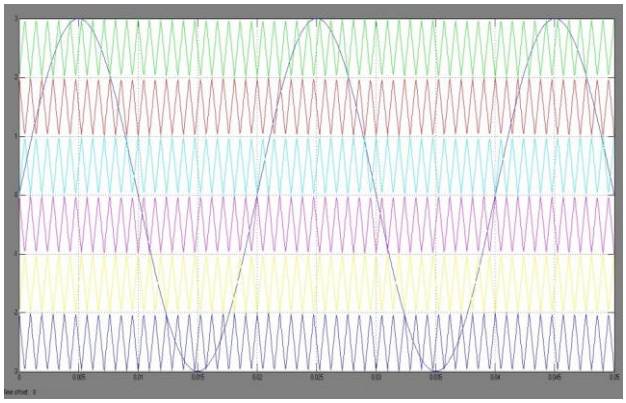


Fig. 7: APOD PWM for 7-level MLI

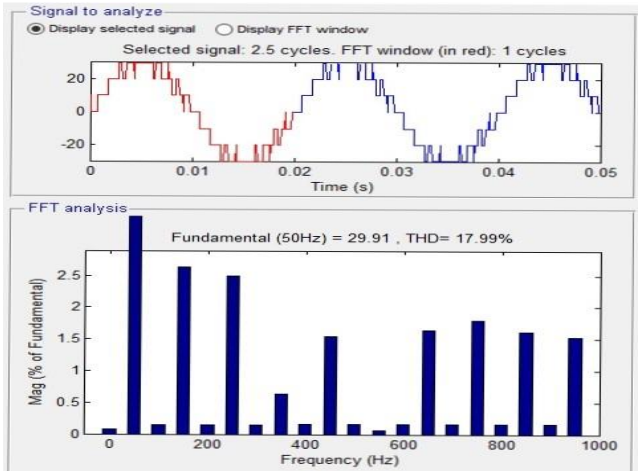


Fig. 8: FFT Analysis for PD PWM of 7-level MLI

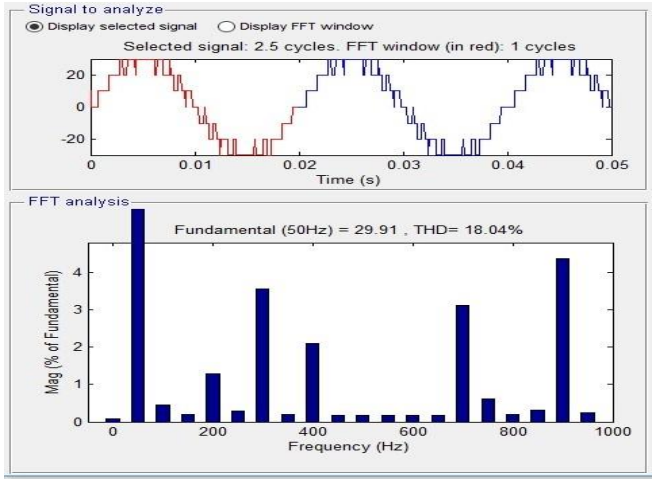


Fig. 9: FFT Analysis for POD PWM of 7-level MLI

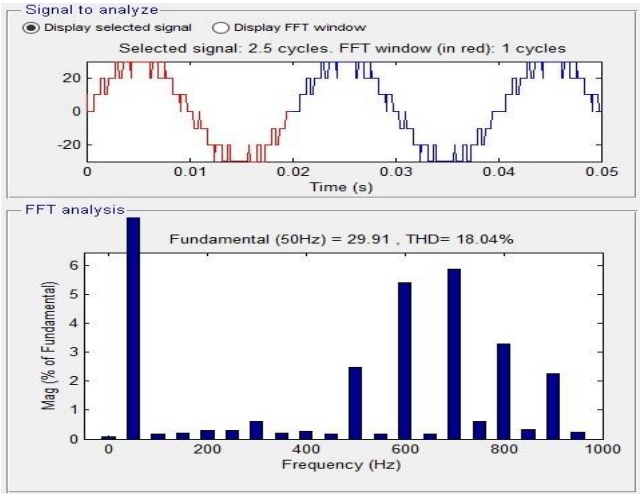


Fig. 10: FFT Analysis for APOD PWM of 7-level MLI

C. 6-Switch 9-Level MLI

This topology is also constructed in the same configuration of 5-switch 7-level MLI. In this we use 5 DC voltage sources and 6 MOSFET switches. In this also 4 MOSFET switches are connected in between the 5 DC voltage sources and the remaining 2 MOSFETs play the role of Polarity reversal. The DC input voltage is 10V dc and the load used is a Resistive load whose value is 10 Ohms. MOSFET block parameters are same as the 5-switch 7-level topology. In Table-2 switching operations of

switches are mentioned by 0 and 1. 0 indicates OFF state and 1 indicates ON state.

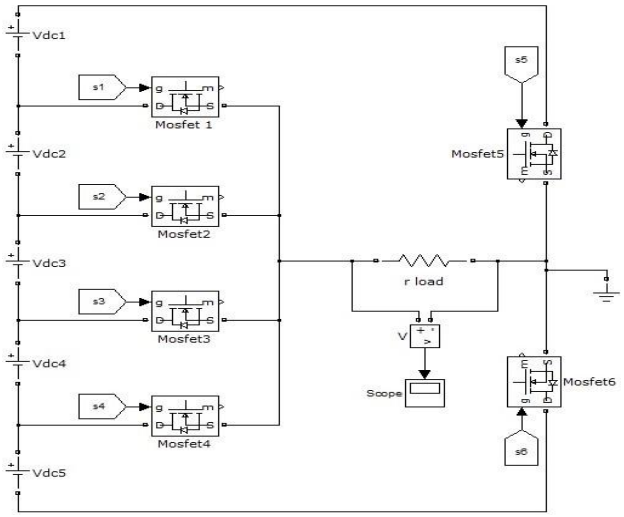


Fig. 11: Simulation Circuit of 6-switch 9-level MLI

Table 2: Switching Topology of 6-Switching 9-Level MLI

Sl.no	S1	S2	S3	S4	S5	S6	o/p voltage
a	0	0	0	1	0	1	+1Vdc
b	0	0	1	0	0	1	+2Vdc
c	0	1	0	0	0	1	+3Vdc
d	1	0	0	0	0	1	+4Vdc
e	0	0	0	0	0	0	0
f	1	0	0	0	1	0	-1Vdc
g	0	1	0	0	1	0	-2Vdc
h	0	0	1	0	1	0	-3Vdc
i	0	0	0	1	1	0	-4Vdc

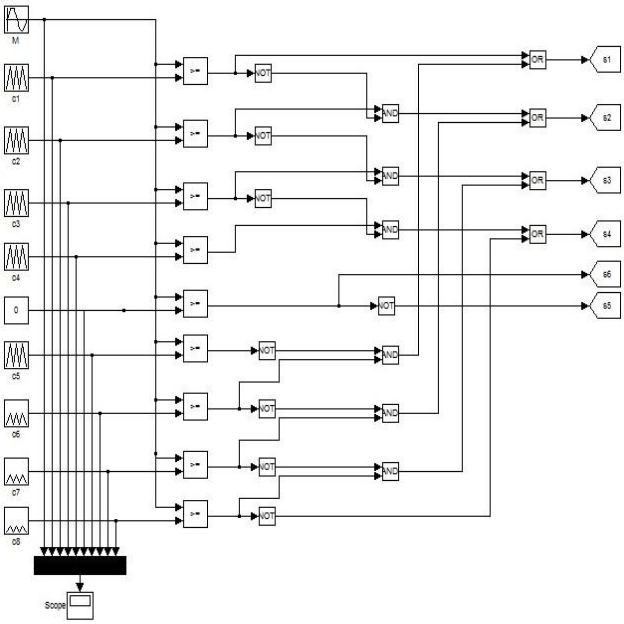


Fig. 12: Sub circuit for 9-level MLI

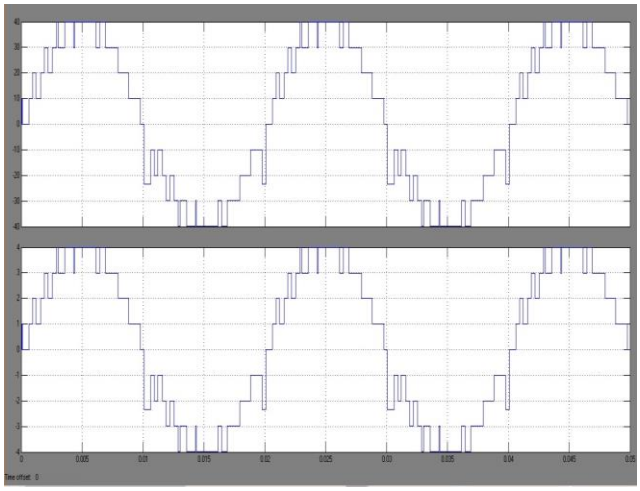


Fig. 13: Output voltage and current waveform for 9-leveel MLI

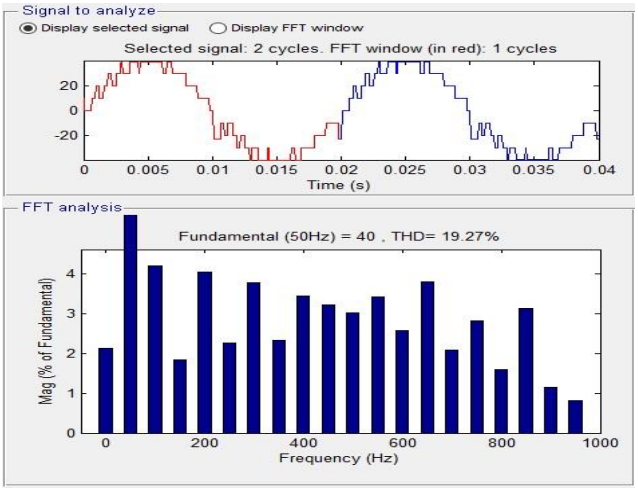


Fig. 14: FFT analysis for 9-level PD PWM

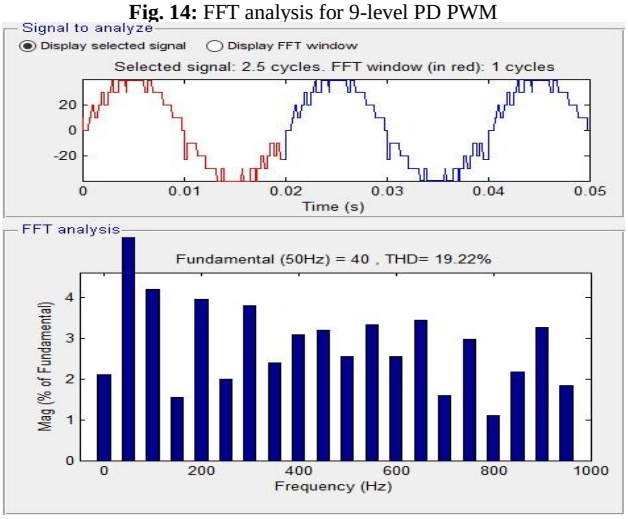


Fig. 15: FFT analysis for 9-level POD PWM

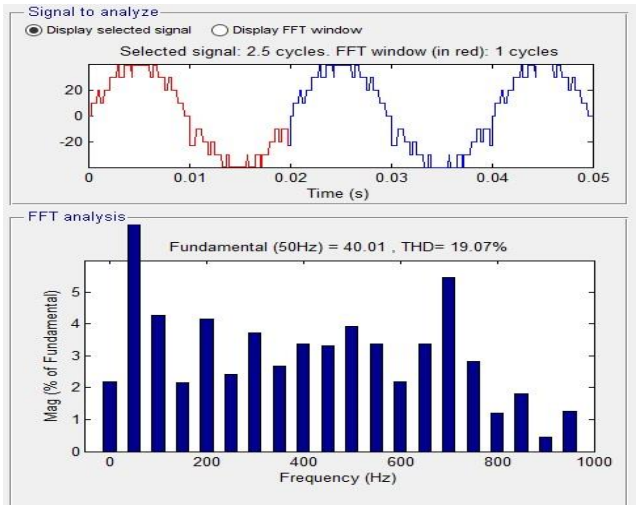


Fig. 16: FFT Analysis for 9-level APOD PWM

D. 7-Switch 11-Level MLI

In this circuit 7 MOSFET switches and 6 DC voltage sources are used. 5 MOSFET switches are connected between the 6 DC voltage sources and the remaining 2 switches are used for the polarity reversal. MOSFET block parameters are the same as the above configuration. In Table-3 switching operations of switches are mentioned by 0 and 1. 0 indicates OFF state and 1 indicates ON state.

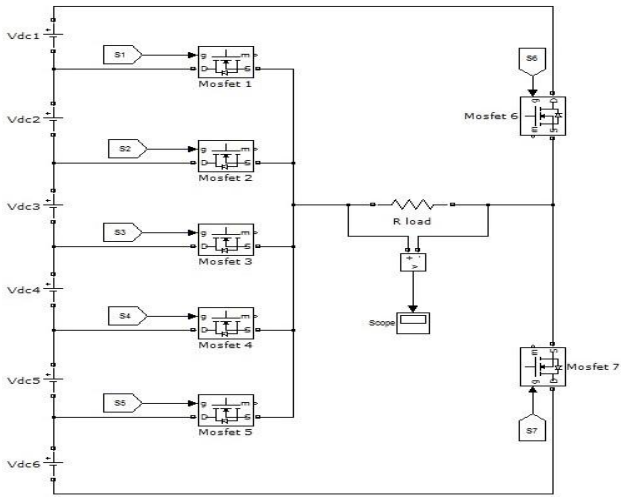


Fig. 17: Simulation circuit for 11-level MLI

Table 3: Switching Topology of 7-Switch 11-Level MLI

Sl.no	S1	S2	S3	S4	S5	S6	S7	o/p voltage
a	0	0	0	0	1	0	1	+1Vdc
b	0	0	0	1	0	0	1	+2Vdc
c	0	0	1	0	0	0	1	+3Vdc
d	0	1	0	0	0	0	1	+4Vdc
e	1	0	0	0	0	0	1	+5Vdc
f	0	0	0	0	0	0	0	0
g	1	0	0	0	0	1	0	-1Vdc
h	0	1	0	0	0	1	0	-2Vdc
i	0	0	1	0	0	1	0	-3Vdc
j	0	0	0	1	0	1	0	-4Vdc
k	0	0	0	0	1	1	0	-5Vdc

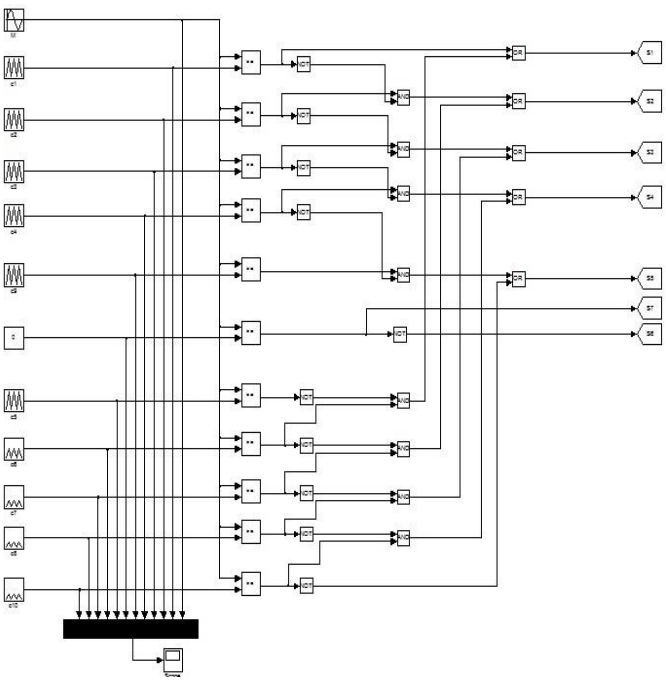


Fig. 18: Sub circuit for 11-Level MLI

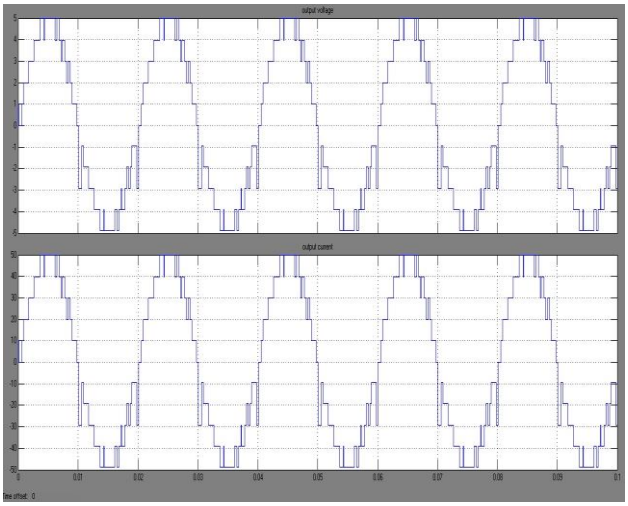


Fig. 19: Output voltage and current waveforms for 11-level MLI

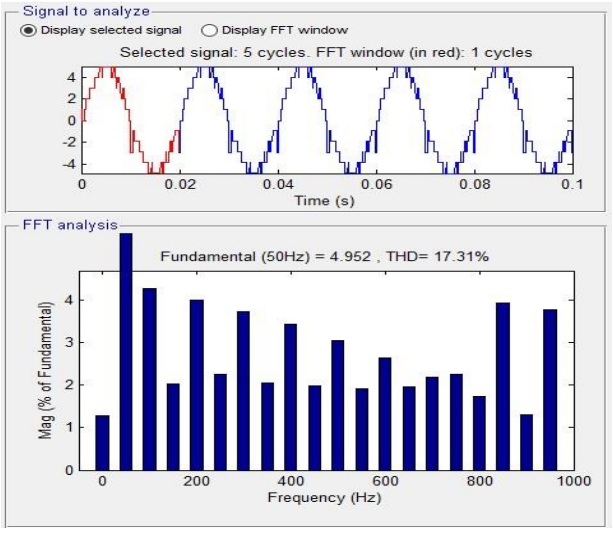


Fig. 20: FFT Analysis for PD PWM of 11-levelMLI

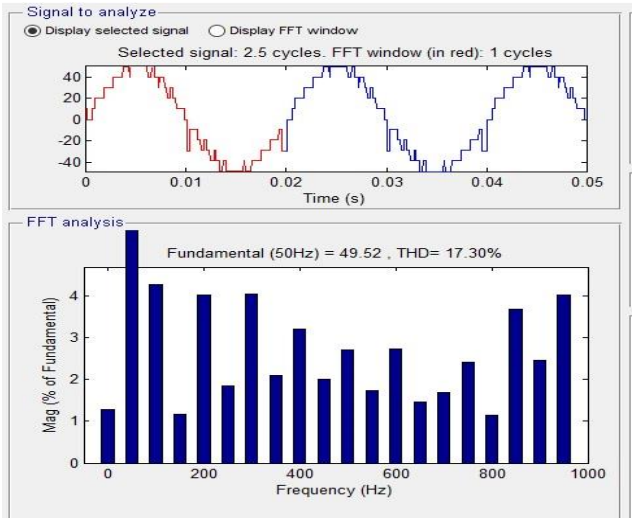


Fig. 21: FFT analysis for POD PWM of 11-level MLI

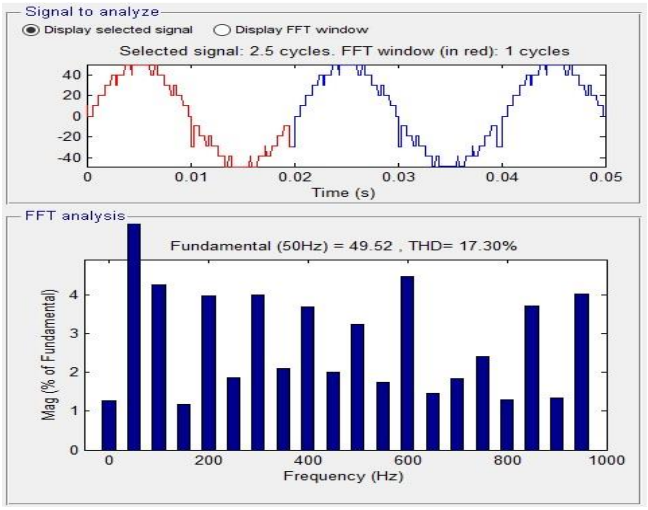


Fig. 22: FFT Analysis for APOD PWM of 11-level MLI

Table 4: Comparison of Proposed MLI With other MLI's

Inbuilt Structure	Flying Capacitor	Diode Clamped	Cascaded 7-level	7-level 9-switch	7-level 7-switch	7-level 6-switch	7-level 5-switch
No.of Capacitors	14	6	-	-	-	-	-
No.of Diodes	-	≥8	-	-	-	-	-
No.of Switches	10	10	12	9	7	6	5
No.of Sources	-	-	3	3	3	4	4

Table 5: THD of 7-Level,9-Level,and 11-Level MLI"S

PWM Technique	5-switch 7-level	6-switch 9-level	7-switch 11-level
PD PWM	17.99	18.04	18.04
PD PWM	19.27	19.22	19.07
PD PWM	17.31	17.30	17.30

5. Conclusion

New topology of 7-level 5-switch MLI is successfully studied by the simulation circuit using MATLAB/SIMULINK. 9-level and 11-level MLI's are also executed by the use of above topology. Effectiveness of the topologies are studied by using THD. This new topologies are simple in design and operation when compared to other MLI structures. Switching losses for 7-level, 9-level and 11-level MLI's are also very less when compared to other topologies.

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