International Journal of Engineering & Technology, 7 (1.5) (2018) 26-30

International Journal of Engineering & Technology

Website: www.sciencepubco.com/index.php/IJET

Research paper

Bit wise and delay of vedic multiplier

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Abstract

The Vedic multiplier is derived from the ancient mathematics called Vedic mathematics .The ancient mathematics has different sutras in that we use Urdhva Tiryagbhyam sutra which means clock wise and vertically . As we know that binary multiplication is not possible so that instead we use binary addition or subtraction instead of it. The key process for the multiplication is the speed of the processor. The fastest mode of multiplication is the Vedic multiplier. In this paper we want to show the delay and utilization of components available for the multiplier by executing the code. The comparison of delay from some papers was also proposed in this paper. The research is going on the Vedic mathematics to overcome the problems on the conventional mathematics. In future Vedic multiplier plays an important role in the DSP (Digital Signal Processing).As it is the fastest and efficient mode of operation. In this paper I am calculating the bit wise delay up to 32-bit. The whole analysis was done in Xilinx. The ISM wave forms for every bit up to 32-bit was to be obtained. The utilization, used, available, utilized analysis was also taken. The whole process was done in XILINX software.

Keywords: *Vedic multiplier, Delay, Digital Signal Processing*

1. Introduction

Vedic Mathematics is an antiquated arrangement of mathematics[3] which takes a shot at Vedas which was reproduced by Jagadguru Swami Sri Bharati Krishna Tirthaji Maharaja around 1911 and 1918 from certain Sanskrit scripts. It is perhaps the most refined and profitable numerical structure conceivable One of such effective method has been utilized to plan of a multiplier.

In DSP multipliers are the fundamental components. Increase is the key perspective, whereby change in computational speed of augmentation declines the preparing time of Digital Signal Processors. Multiplier squares makes utilization of quick Fourier changes.. A quicker strategy for increase in light of antiquated Indian Vedic arithmetic is focused on in this paper. Among various strategies of increases in Vedic arithmetic, UrdhvaTiryagbhyam is powerful. UrdhvaTiryagbhyam is a general augmentation recipe pertinent to all instances of multiplication. For expansion of incomplete items in the multiplier[3].

2. Methodology used

2.1 Urdhva tiryagbhyam

General extension formula utilized is UrdhvaTiryagbhyam Sutra3 proper to all instances of addition. It truly signifies "Vertically and clockwise". How the methodology of the duplication of two, three and four digit numbers is showed up in Fig. 1 using UrdhavaTiryagbhyam Method. The digits on the two closures of the line are duplicated and the outcome is incorporated with the past convey. At whatever point at least three lines are accessible, each one of the outcomes are added to the past convey. The last digit of the number henceforth gained goes about as one of the outcome digit and the rest go about as the convey for the accompanying stride. At first the outcome is taken is zero[3].

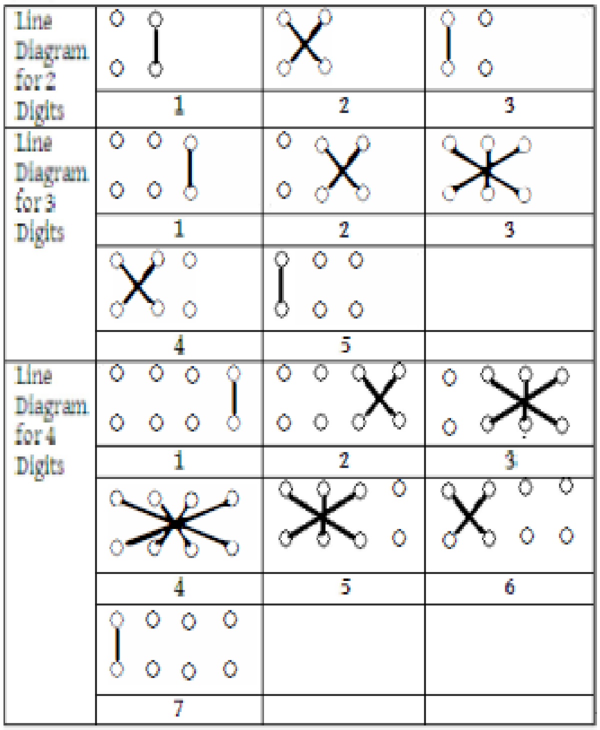

Fig. 1: Vedic multiplier implementation

2.2 Logisim circuit of 2*2 bit Vedic multiplier

The last two digits under go AND operation ,after that the second row first digit perform AND operation with first row second digit and the AND operation take place between second row second digit and first row first digit then the summation (half-adder)between the two AND operations was performed. At last the first two digits under go AND operation [13].

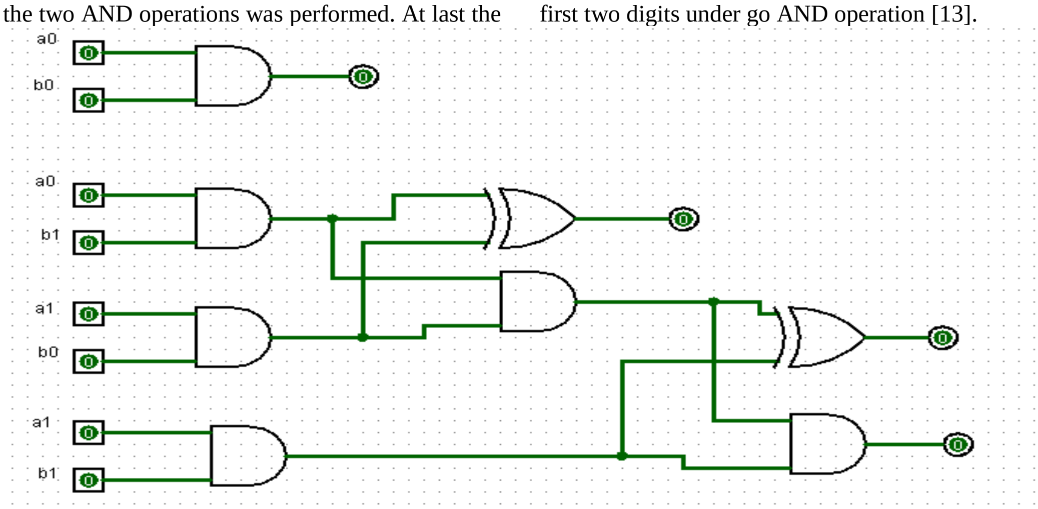

Fig.2.2: Bitimplementation of Vedic multiplier

The whole circuit implemented in logisim was shown in Fig 2.The same process will take place for the 4 –bit, 8-bit, 16-bit, 32-bit. The results are obtained for the individual bits for our requirement. From the results we are obtaining the delays and utilization of the components was also obtained in the XILINX software while executing[6].

3. Xilinx Model Sim Simulations

2*2 Vedic multiplier wave forms

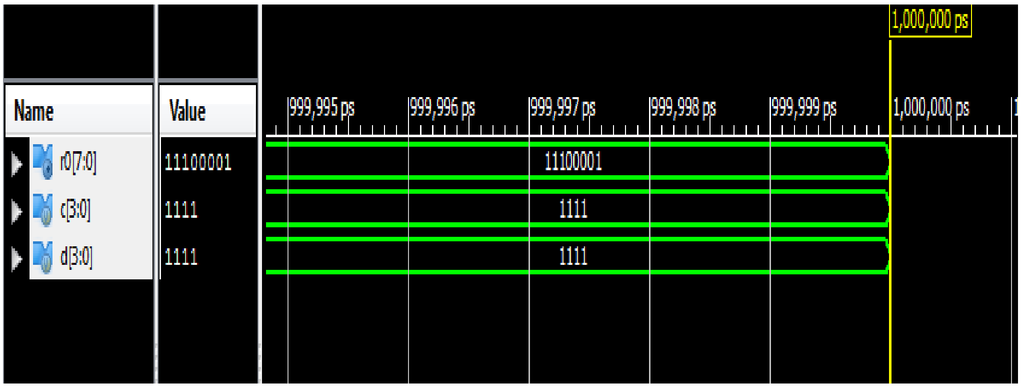

Fig. 3: 2 Bit wave form

Figure3 describes the movements to build two 2 bit numbers[6]. Changing over the above figure to an equipment comparable we have 3 and gates which will go as 2 bit multipliers and two half adders to add the item to get the last item. Here are the equipment purposes of interest the multiplier Where "an" and "b" are two numbers to be multiply and "q" is the result. With this graph we are presently arranged the code in Verilog effectively utilizing and gates and HA (half adders). To make the design more modular we endeavor code for HA first and a short time later instantiate it to have the last product.

4*4 vedic multiplier wave forms

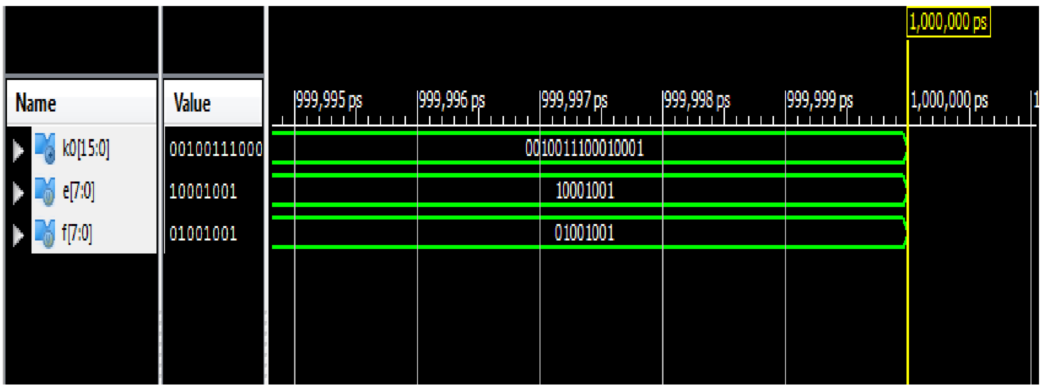

Fig. 4: 4 Bit wave form

Using 4 such 2x2 multipliers and 3 adders we can assemble 4x4 bit multipliers as showed up in the layout. Legitimate instantiating of the 2x2 multipliers and adders. We have to first make code for 4bit and 6 bit adders[6].
Each piece as showed up above is 2x2 bit multiplier. Beginning 2x2 multiplier inputs are "A1 A0" and "B1 B0". The last square is 2x2 piece multiplier with inputs "A3 A2" and "B3 B2". The middle one shows two, 2x2 bit multiplier with inputs "A3A2" and "B1B0" and "A1A0" and "B3B2". So the last delayed consequence of augmentation, which is of 8 bit, "S7S6S5S4S3S2 S1S0".

8*8 Vedic multiplier wave form

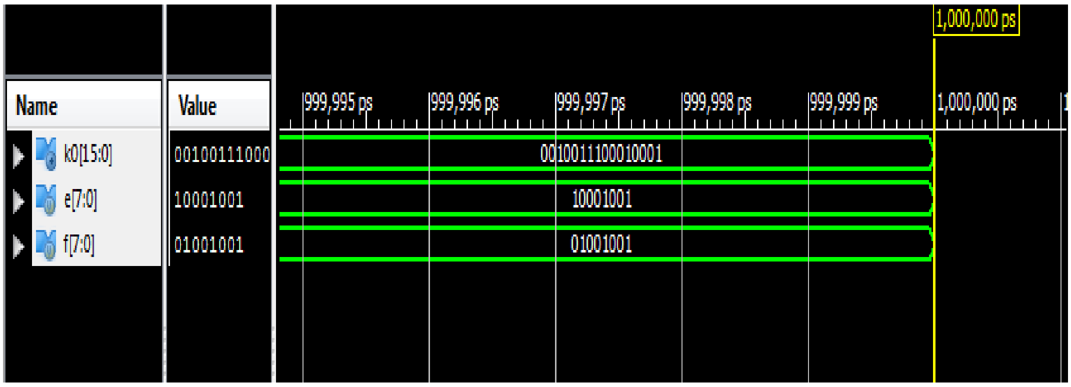

Fig.5: 8 bit wave form.

Like the past layout of 4x4 multiplier, we require 4 such 4x4 multipliers to make 8x8 multipliers[6]. Here we need to first arrangement 8bit and 12 bit adders and by suitable instantiating of the module and associations as showed up in the figure5 we have made a 8x8 bit multiplier. As of right now of time it is fundamental for you to try and confirm the RTL code and check if the equipment is according to our design. Arrangement Ahead apparatus by Xilinx gives better perspective of the hardware output with configuration elaborate alternative . Elude the development tree chart to know the methodology for 8x8 multiplier.

16*16 Vedic multiplier wave form

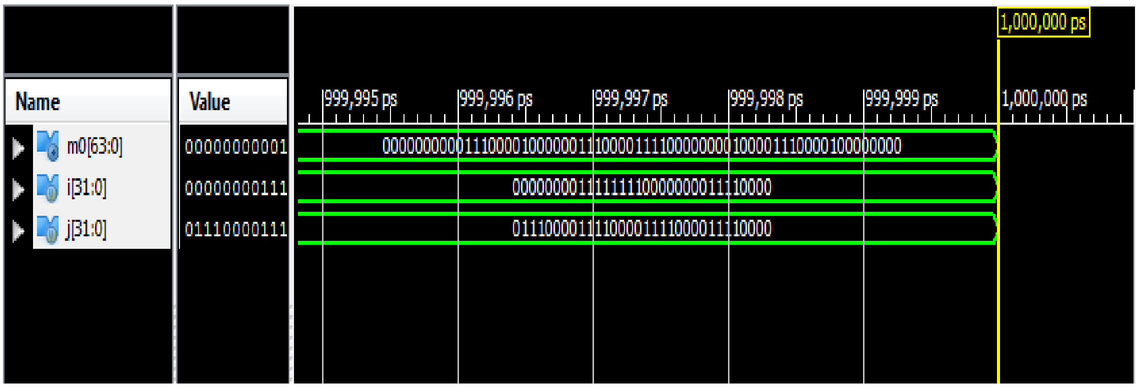

Fig. 6: 16-bit wave form.

We take after the same stratage as though there ought to be an event of past multipliers and make 16x16 multipliers appeared in fig 6. The framework of 16×16 piece is a practically identical action of 8×8 squares in an advanced path as the introductory stage in the setup of 16×16 square will be assembling the 8 bit (byte) of each 16 bit information. These lower and upper bytes sets of two inputs will shape vertical and transversely thing terms. Each information byte is care with by an alternate 8×8 Vedic 15 multiplier to convey sixteen halfway thing pushes. These partial things columns are then incorporated a 16-bit carry look ahead adder in ideally to make last bits[6]

32*32 Vedic multiplier waveform

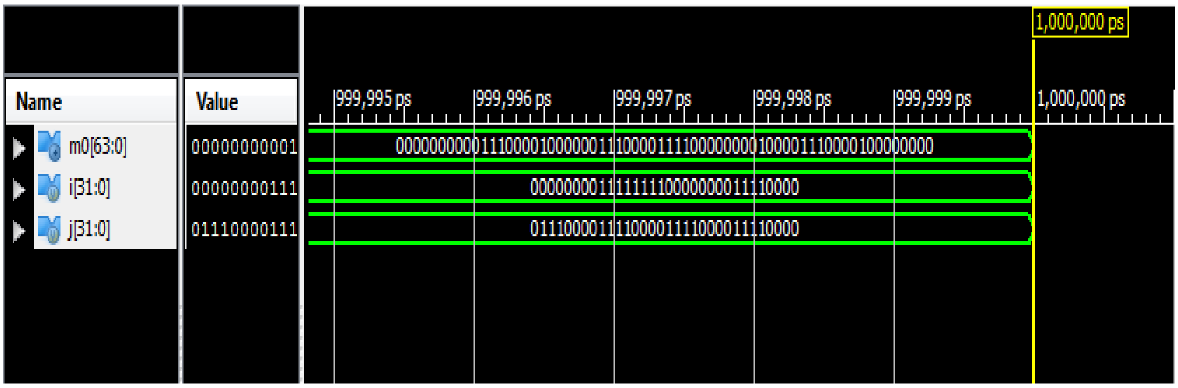

Fig. 7: 32-bit wave form.

Same like the above we can obtain this wave forms from the 16*16 Vedic multiplier as shown in fig7.By using the format of the Vedic multiplier we can obtain the wave forms for the higher order also [6].

4. RTL Schematics of vedic multiplier

The RTL schematic for the Vedic multiplier was inter related to each other individually the 2-bit was used to obtain 4-bit,the 4-bit is used to obtain8-bit,the 8-bit is used to obtain 16-bit,16-bit is used to obtain32-bit. Without the formation of one bit another bit was not obtained. The RTL schematic of 2-bit was stated below figure8.

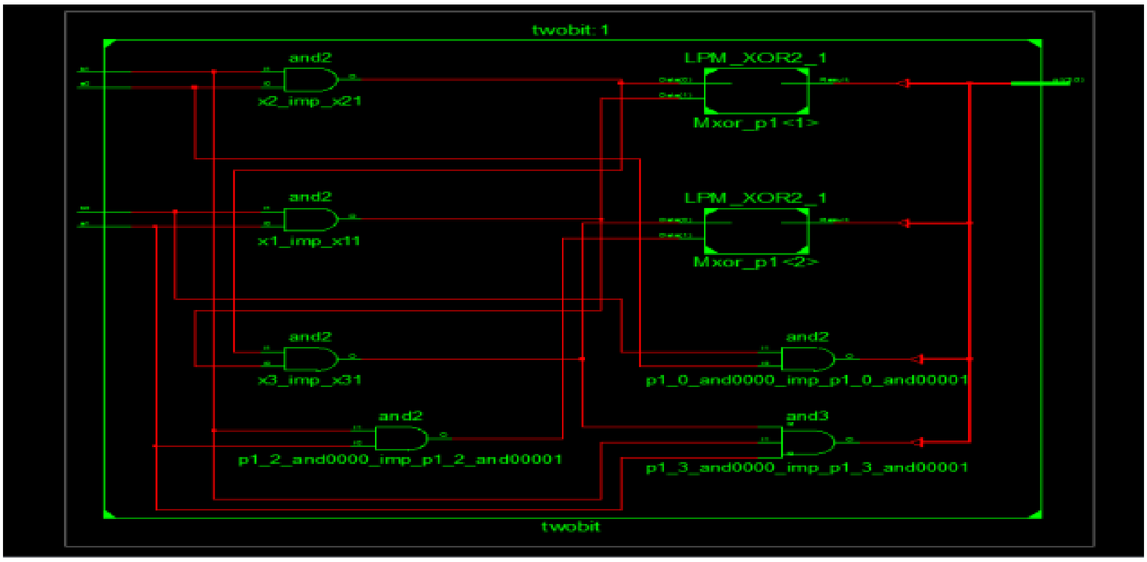

Fig. 8. RTL schematic of 2-bit vedic multiplier.

5. Delay analysis with respect to different papers and different multipliers

2*2 Multiplier:
The delay of 2-bit Vedic multiplier was shown below
Maximum combinational path delay:6.376ns

4*4 Multiplier:
The delay of 4-bit Vedic multiplier was shown below
Maximum combinational path delay:12.542ns

8*8 Multiplier:
The delay of 8-bit Vedic multiplier was shown below
Maximum combinational path delay:19.416ns

16*16 Multiplier:
The delay of 16-bit Vedic multiplier was shown below
Maximum combinational path delay:25.825ns

32*32 multiplier:
The delay of 32-bit Vedic multiplier was shown below
Maximum combinational path delay:32.237ns

Table 1: Table showing delay comparison for 16 bit and 8 bit in previous papers

Bit wise	Delay
16-bit	50.952ns
8-bit	23.64ns

Table 2: Table showing delay comparison for 16 bit and 8 bit in our present papers

Bit wise	Delay
16-bit	25.825ns
8-bit	19.416ns

For 16-bit Vedic multiplier using urdhavaTiryagbhyam multiplier in [6]was 50.952ns but in our model we get the delay of 25.825ns.

For 8-bit Vedic multiplier using urdhvaTiryagbhyam multiplier in [6] was 23.644ns but in our model we get the delay of 19.416ns.

We can say that utilization of the components and delay is less in the proposed paper than the reference paper.

6. Advantage

The speed increases for the reversible logic of the multiplication process will occur in same time so by this system reaction is not different for different inputs and all will gives output at same time.

7. Limitation

In this the limitation is that if we increase the number of bits that appended by this the number of flip-flops increases and by this the size increases by this the Power consumption increases.

8. Applications

- Micro processors
- Filtering process (FIR)
- Digital signal processors
- IF stages of the receiver

9. Conclusion and future scope

The conventional multiplication methodology requires additional time and territory on silicon than Vedic calculations. All the more fundamentally dealing with speed increments with the bit length. This will help at long last to speed the preparing work, as it some assistance with being certainly appreciated that the multiplier is the real building square of FFT.

Multipliers can be designed to take after the strategy for Vedic multiplication. The disadvantage of designing any higher bit multiplier is that the lower bit multipliers can't be cascaded to acquire a multiplier capable for increasing more number of bits, as an account of adders. The Vedic multiplier can be utilized to solve this issue. For instance we can outline 64-bit Binary multiplier can be utilized to design a 32-bit binary multiplier.

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