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Research paper

CMOS Front-End of LNA for GPS and GSM wireless applications

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Abstract

This paper describes a layout of a CMOS Low Noise Amplifier for reconfigurable packages which include GPS, GSM Wi-Fi applications. The improvement of a notably linear Radio front-stop, able to function with Galileo and GPS satellite signals suitable for coexisting in a mobile opposed environment for area based offerings, pleasing the fundamental necessities for a mass market product which includes low cost, low footprint, good accuracy, low strength intake and high sensitivity. primarily based on a wideband enter matching, the LNA stages cowl all band of hobby even as reaching a great change-off between excessive gain, low noise parent and coffee electricity intake. The complete simulation analysis of the circuit results in the frequency range of 1.4 GHz to 2 GHz. The noise figure is 1.8 dB at 1.4GHz and rises to 3.4 dB at 2 GHz. The input return and output return losses (S_{11}, S_{22}) of the LNA at a frequency range between 1.4 GHz and 2 GHz are $S_{11=}$ -12 dB, S_{22} =-44.73 dB at 1.77 GHz and S_{22} =-26.47 dB at 2 GHz. The overall gain of the LNA (S_{21}) is 13 dB at 1.4025 GHz, 3rd order input intercept point (IIP3) = -3.16 dBm and -1dB compression point is -12.56 dBm. Input Impedance of 50Ω, 3dB Power Bandwidth of 450MHz, and Power Dissipation of 2.7mW at 1.2V power supply.

Keywords: *CMOS Technology, Front-End Receiver, LNA, GPS, GSM, Low Noise Figure, Wireless Communications.*

1. Introduction

Radio Frequency (RF) industry has taken a drastic change since the days of Marconi, who introduced radio communication [3]. In responding to the demand for a low-cost but high performance wireless front-end, many intensive researches on CMOS radio-frequency (RF) front-end circuits have been carried out. The ultimate goal is to minimize the trade-off between high performance and low-cost, low power consumption design.

Recently, the global positioning system (GPS), which was originally developed for military purposes, is widely used to obtain location information for applications such as ocean remote sensing, car navigation systems fabricated in a CMOS process, since its size, cost, and power consumption have been significantly reduced [1]. GSM and GPS based tracking system will provide effective, real time vehicle location, and reporting. A GPS- GSM based tracking system will inform where your vehicle is and where it has been, how long it has been. The system uses geographic position and time information from the Global Positioning Satellites. The use of GSM and GPS technologies allows the system to track vehicle and provides the most up-to-date information about ongoing trips [13,14, 20, 21]. This system finds its application in real time traffic surveillance. It could be used as a valuable tool for real time traveler information, congestion monitoring, and system evaluation.

The signal delivered by antenna in modern wireless systems can be in the sub-microvolt range underscores the acute need for low noise amplification. The low noise amplifier is the most important component to compensate the noise figure in a RF front-end module shown in Fig.1. The key design parameters of
LNA are the high gain, low noise figure and high linearity. The linearity becomes more and more important in modern digital wireless system because a complex digital modulation where the RF signals usually have high peak-to-average ratio. Therefore a highly linear LNA is demanded in a wireless receiver to reduce inter-modulation distortion. The linearity of LNA is described by its input referred 3rd order intercept point. Thus, LNA should boost the desired signal power while adding as little noise and distortion as possible so that the retrieval of this signal is possible in subsequent stages in the system [11, 12]. Hereby, low noise amplifier should be matched with the antenna characteristics. The characteristics of antenna are excellent input and output matching and high gain.

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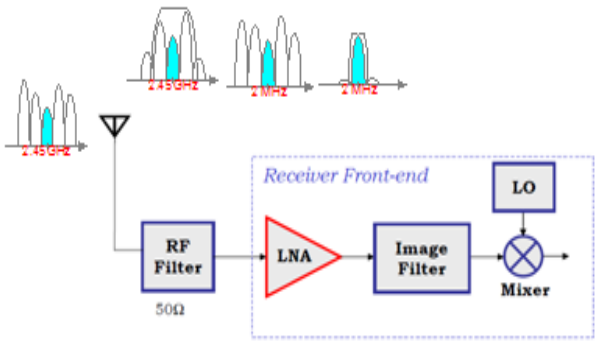

Fig.1: Block diagram of Receiver Font-End

2. Design parameters of LNA

The following design parameters are used to construct to the low noise amplifier "[2, 9].

- **Noise Figure**: This specifies the noise performance of a circuit or device. Noise Figure measures the SNR degradation as a signal pass through a system. If a system has no noise the NF=1, F=0dB. The ratio of input SNR to the output SNR it can be expressed as

$$\mathrm{NF} = \frac{\mathrm{SNRin}}{\mathrm{SNRout}}$$

Where SNR denotes the signal-to-noise ratio at a particular node, as the LNA is the first block of the receiver, its NF decides the NF of the entire receiver chain. Noise figure of an LNA is considered to be less than 3dB.

- **Gain:** Gain of LNA should be large enough to minimize the noise contributions of subsequent stages. However, the choice of gain leads to a compromise between noise figure and linearity, as high gain may saturate subsequent devices.
- **Input Return Loss (input matching):** For maximum power transfer from the antenna and the LNA, the input return loss (S_{11}) of the LNA should be low; else the antenna will reradiate part of the input signal.
- **Stability:** The LNA should be stable of all source impedances at all frequencies. If the LNA begins to oscillate at any frequency, it becomes heavily non-linear and its gain becomes highly compressed. A measure of stability is Stern stability factor and defined as,

$$k = (1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2)/(2|S_{12} * S_{21}|)$$

Where

$\Delta = (S_{11} * S_{22} - S_{12} * S_{21})$- S_{12}*S_{21})

If K > 1 and Δ<1, the circuit is unconditionally stable.

- **Linearity:** Linearity of the LNA is defined by its IP_3 and P_{1dB} points. The LNA does not limit the linearity of the receiver. Owing to the cumulative gain through the RX chain, the overall IP_3 and P_{1dB} points are automatically limited. So in LNA design, its linearity is of least concern.
- **Sensitivity:** It can be define as minimum signal level that a system can detect with acceptable signal-to-noise ratio at the output. It can be expressed as.

$$P_{in\,min} = \left[-\frac{174\ dBm}{Hz} + NF + 10logB\right] + SNR_{min}$$

- **Dynamic Range:** It can be defined as the ratio of maximum input level that the circuit can tolerate to the minimum input level at which circuit provides a reasonable signal quality.

$$DR = \frac{P_{in\,max}\ [dBm]}{P_{in\,min}[dBm]}$$

3. LNA topologies

A low noise amplifier (LNA) serves as the first receiving gain stage required to sufficiently amplify a small incoming RF signal for further signal processing. Also, it must meet several specifications at the same time. The essential requirement of a LNA is to amplify the signal without adding additional amount of noise and distortion while at the same time it should consume a minimal amount of power. The circuit topology of an LNA is very important, because it determines the essential performance of the LNA, such as the introduced noise figure, linearity, gain and power consumption. There are two main advantages of using inductive source degeneration topology in this work to realize the input impedance matching. First, it does not introduce additional noise as in the case of a shunt input resistor used to match the signal source. Second, it does not restrict the value of g_m like in the case of the common-gate configuration [5]. To optimize the low noise amplifier design, the suitable topology should be selected for low power and low voltage. There are lots of methods to adjust the input impedance of the amplifiers [2,6]. Four distinct methods are.

A. Resistive Termination
B. Shunt-Series Feedback
C. Common Gate Amplifier or ($1/g_m$) Termination
D. Inductive Degeneration.

A. Resistive Termination

In Resistive Termination Topology, a 50Ω Resistor (R) is simply placed across the input terminals of a common-source amplifier (Fig. 2(a)) with a source resistance (R_S) and an output resistance (R_L) [2].

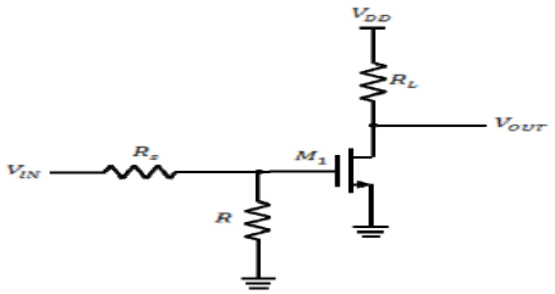

Fig.2(a): Resistive Termination

However, this additional resistor introduces thermal noise that increases the amplifier's NF and attenuates the signal before the transistor, resulting in unacceptably high noise. This method utilizes a resistor at the input terminal of the LNA to provide a 50Ω input resistance.

B. Shunt-Series Feedback

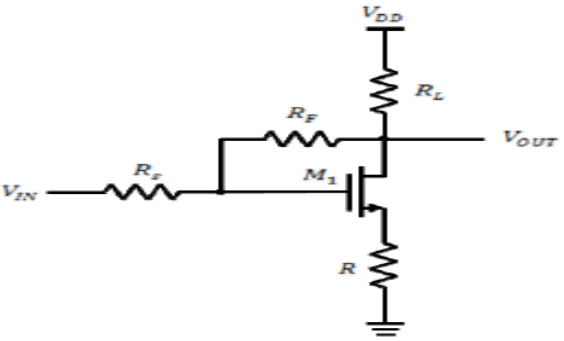

Fig.2(b): Shunt-Series Feedback

In a shunt-series feedback topology shown in Fig.2(b), before amplification the resistor R does not cause attenuation of signals. It is expected that the noise figure in shunt-series feedback amplifier is improve than that of a resistive termination amplifier [5]. On the other hand, the resistor feedback network remains a source of thermal noise. However this method generally has high power dissipation compared to others with similar noise

performance and requires accurate on-chip resistors that actually are not available in existing CMOS Technologies. It is difficult to trade of among gain, small noise figure and good input and output matching.

C. Common Gate Amplifier or (1/gm) Termination

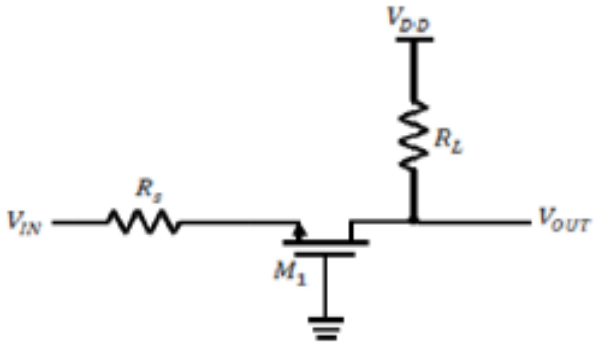

Fig.2(c): $1/g_m$ Termination

The common gate topology is another circuit implementing resistive input impedance (Fig. 2(c)). Characteristics of the common-gate topology are that the resistance looking into the source terminal equals (1/ gm). The major drawback of CG topology is high input-referred noise and less gain.

D. Inductive Degeneration

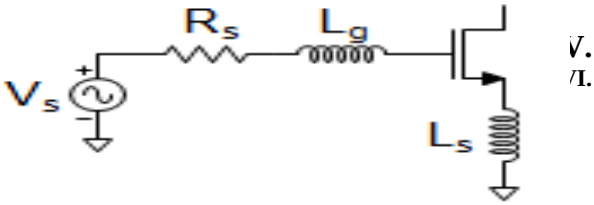

Fig.2(d): Inductive Degeneration

An inductive source degeneration topology [5] shown in Fig.2(d) is commonly used to create resistive input impedance without the noise of real resistors. This topology provides resistive input impedance at the resonant frequency without the thermal noise of an ordinary resistor and degrading the noise performance of the amplifier. It provides higher gain with a low noise figure [2].

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4. Impedance Matching Technique

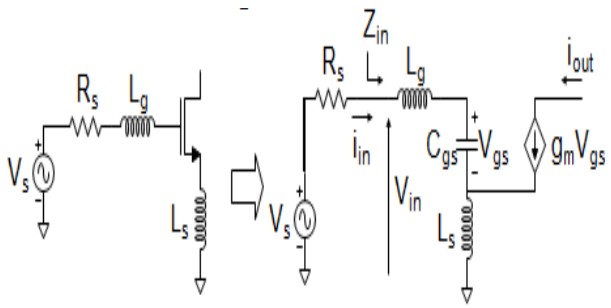

Fig.3: Equivalent circuit of input matching network with source inductive degeneration

Above fig.3 shows the traditional cascade structure with the inductive source degeneration. Its small signal equivalent circuit for impedance calculations [4,8].

$$V_{in} = I_{in} sL_g + I_{in}\frac{1}{sC_{gs}} + (I_{in} + g_m V_{gs})sL_s$$

$$= I_{in} sL_g + I_{in}\frac{1}{sC_{gs}} + (I_{in} + g_m I_{in}\frac{1}{sC_{gs}})sL_s$$

$$= I_{in}\left[s(L_g + L_s) + \frac{1}{sC_{gs}} + \frac{g_m L_s}{C_{gs}} \right]$$

$$\text{Zin} = \frac{Vin}{Iin}$$

$$Z_{in} = s(L_g + L_s) + \frac{1}{sC_{gs}} + \frac{g_m L_s}{C_{gs}}$$

$$\omega_0^2 = \frac{1}{(L_g + L_s)C_{gs}}$$

$$\frac{g_m L_s}{C_{gs}} = R_s$$

Where C_{gs} and g_m are the intrinsic gate-to-source capacitor and the transconductance of M1, resp. When the input impedance matching network composed by L_g, L_s and C_{ex}, resonating at the operating frequency, the imaginary part of Z_{in} is eliminated. The impedance becomes a pure real part and only relevant to L_s and C_{gs}, therefore, by adjusting Ls and C_{ex} can easily realize to real 50Ω resistance at the input o the LNA [7,10].

This paper focuses on LNA (Low Noise Amplifier) of RF Front-End. To meet the design requirement, it needs to make a balance between noise figure and linearity. This proposed architecture includes source inductive degeneration LNA. And also it must meet the requirements of common design features for the receiver front-end like Noise Figure (NF), input-referred third-order intercept point (IIP_3) and input power 1-dB compression point (CP_{1dB}), and Conversion Gain. Low power consumption as well as good noise performance is a great challenge to design.

5. Circuit Design and Analysis

The schematic of LNA is a fully integrated LC-tuned cascode amplifier with the inductive source degeneration provides a good input-output isolation; Input Impedance is obtained using the source degeneration inductor Ls and Gate inductor L_g sets the resonant frequency.

After choosing the suitable technology and topology, next step is to choose the size of the input device. The below equations are used to design the source inductor Ls, gate inductor Lg, drain inductor Ld and width of the input device W.

$$Ls = \frac{g_m}{C_{gs}} = \frac{R_s}{w_T}$$

$$w_T = 2\pi f_T$$

$$L_g = \frac{Q_L R_s}{w_0} - L_s$$

$$L_d = \frac{1}{w_o^2 C_L}$$

$$\text{Cgs} = \frac{1}{\text{w}_0^2(\text{Lg} + \text{Ls})}$$

$$W = \frac{3C_{gs}}{2C_{ox}L_{min}}$$

The inductance L_s and L_g and the additional capacitance C_{gs} consist of the input matching network of this LNA to match the signal source impedance (50Ω) at the operating frequency. Where g_m is the transconductance of the device, C_{gs} is the gate source capacitance and Rs is the source resistance which is equal to 50Ω. f_T in equation is the unity gain frequency of the MOS transistor. Q_L is the Q factor of the inductance which is chosen as 2.67. ω_o is the center frequency which is chosen to be 2GHz. In equation C_{ox} is the oxide capacitance and L_{min} is the minimum channel length which is 180nm in this design.. When the received signal becomes strong enough, the gain of LNA is adjusted to a lower value, in order not to saturate the following circuits. Since the useful signal

becomes strong enough when the gain of LNA lowers, the noise has little effect on the BER performance of the receiver. So we should optimize the noise performance with the weakest signal and the highest LNA gain. Based on the traditional cascade structure as analysis the LNA schematic as shown in Fig.4.

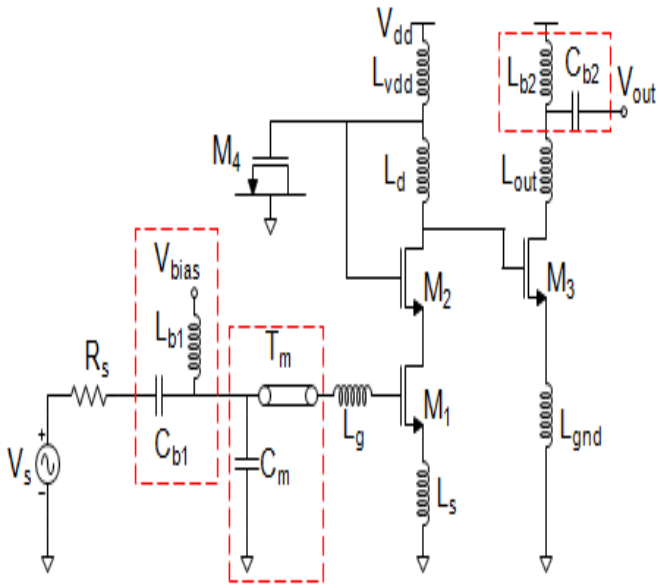

Fig.4: Schematic of proposed LNA

6. Simulation Results and Discussions

The LNA has been implemented in a TSMC 0.18µm RF Process. The lengths of all the transistors adopt the minimum channel length 0.18µm to obtain a higher cutoff frequency. The main component parameters of the LNA are listed as follows:

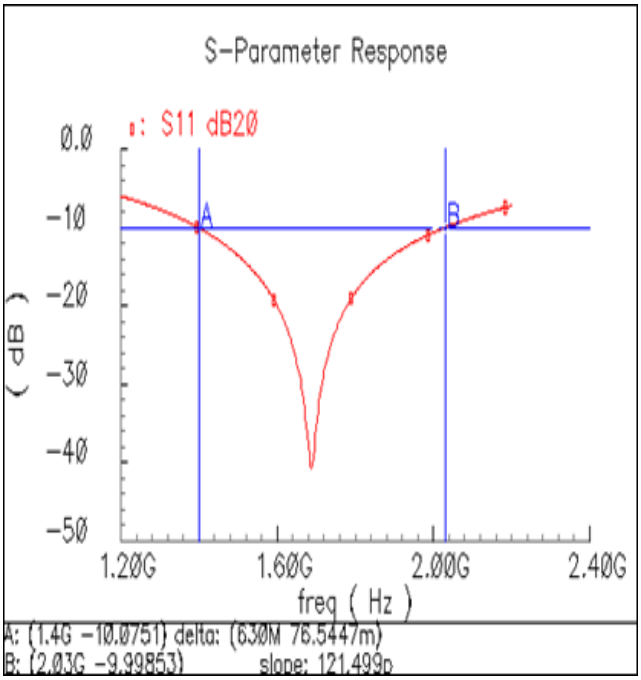

Fig.5: The simulation of input/output return losses.

The input return and output return losses (S_{11}, S_{22}) of the LNA are -12dB at a frequency range between 1.4 GHz and 2 GHz.

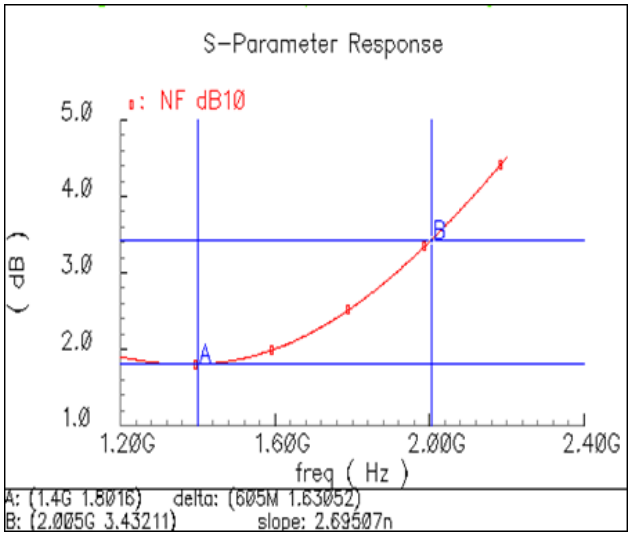

Fig.6: The simulation of Noise Figure

Above fig.6 presents the noise figure simulation of the proposed LNA. It can be seen that the noise figure is 1.8 dB at 1.4GHz and rises to 3.4dB at 2 GHz.

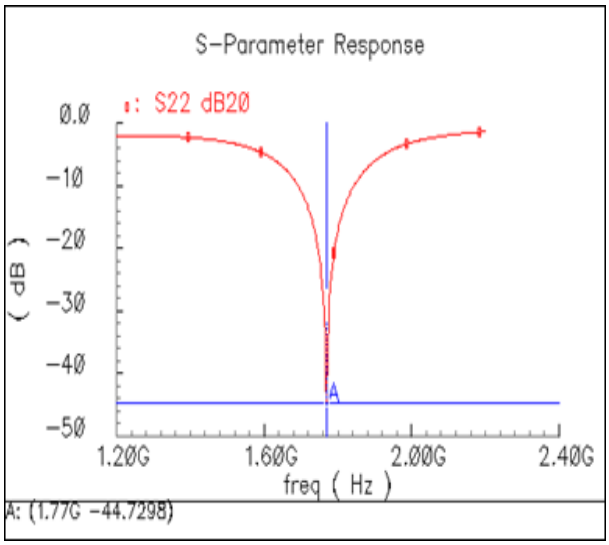

Fig.7: S_{22} =-44.73 at 1.77 GHz

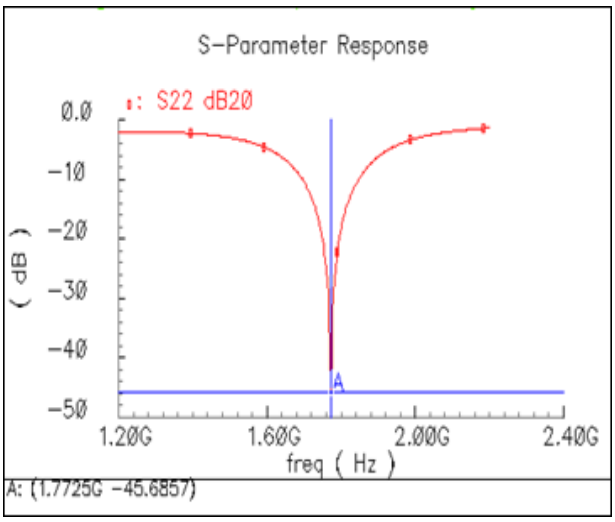

Fig.8: S_{22} =-45.68 at 1.7725 GHz

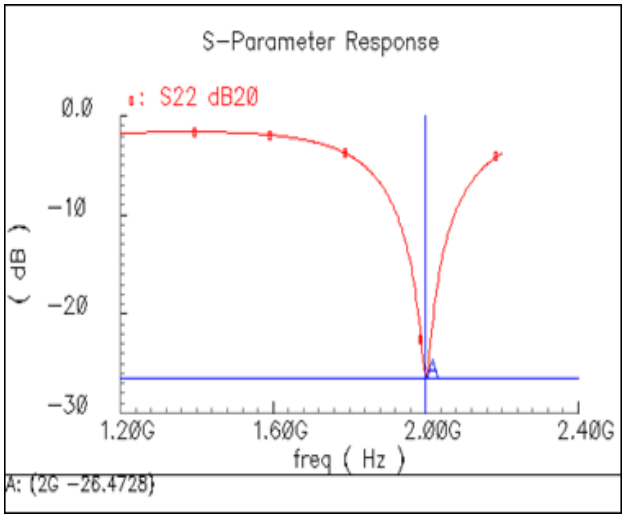

Fig.9: S_{22} =-26.47 at 2 GHz

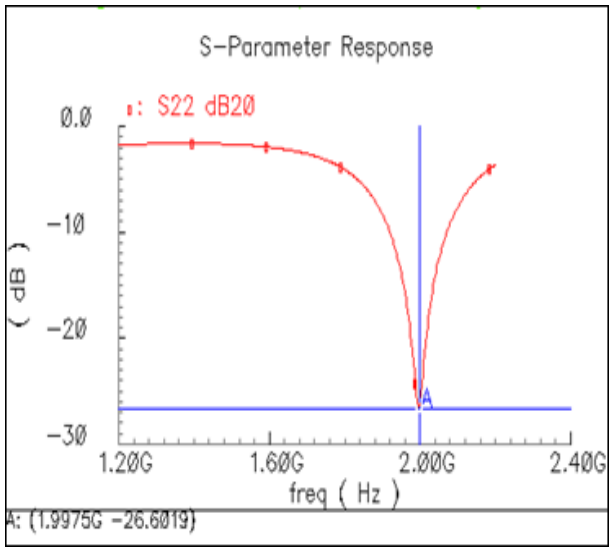

Fig.10: S_{22} =-26.60 at 1.9975 GHz

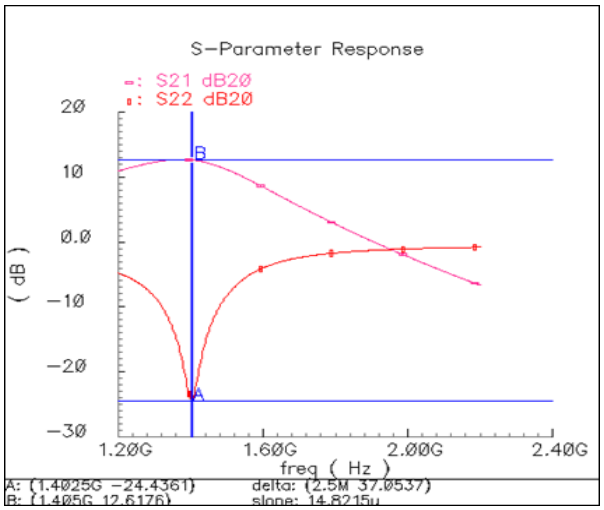

Fig.11: The overall gain of the LNA (S_{21}) is 13dB at 1.4025 GHz

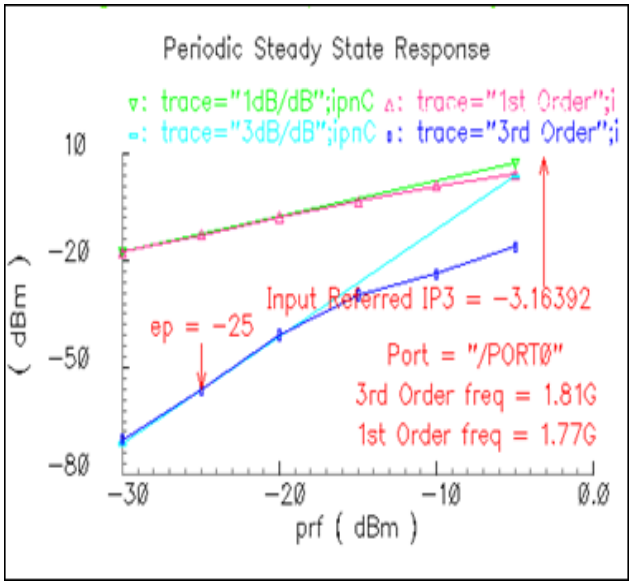

Fig.12: 3rd order input intercept point (IIP_3)

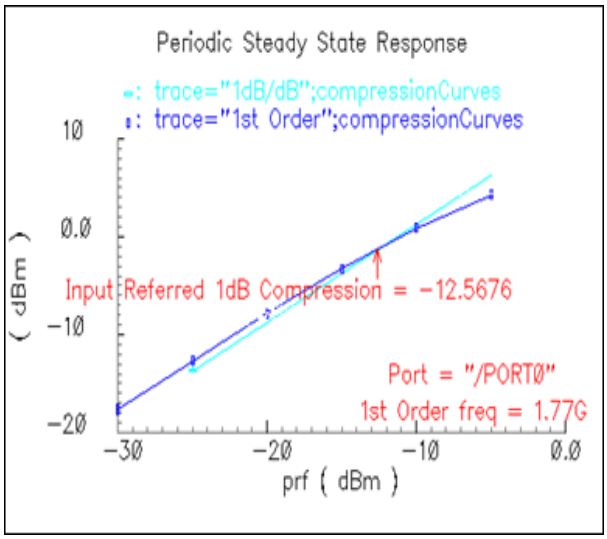

Fig.13: -1dB compression point.

7. Conclusion and Future Scope

Simulation results showed increased voltage gain with lower power consumption. Designed LNA has also better input impedance matching and suitable power gain. Hence Different topologies of the Low Noise Amplifier are studied keeping in view the low noise requirements. The inductive source degeneration topology is chosen such that there is no noise due to the input circuitry. With this topology, the required input impedance of around 50Ω is achieved. The output load is a tuned circuit, constituting of a load inductance and the input capacitance of the following circuit. The amplifier is first designed to achieve noise optimization. The topology choose produced acceptable results.

With the advancing technology, inductors of different values, with reasonably good Q values can be integrated for RF circuits. The performance of the circuit can be improved with the availability of a variety of inductor values at hand. The linearity of the circuit can be still improved from what is achieved in this work.

The Table1 summaries the important parameter of the proposed LNA along with reported other" LNA work existing in literature.

Table 1: Comparison of proposed LNA with previously published papers

Parameter	**Achieved value**	Ref [1]	Ref [5]
Center Frequency(GHz)	**1.4 to 2GHz**	1.1 to 1.6GHz	1.57 to 1.9GHz
Voltage Gain(dB)	**22**	---	19
Noise Figure(dB)	**1.8 to 3.4**	6.48	2.9
IIP_3(dBm)	**-3.16**	-14	-17
Input return loss S_{11}(dB)	**-12**	-10	--
Power gain S_{21}(dB)	**13**	--	11.2
Output return loss S_{22}(dB)	**-44.73 to -26.47**	--	--
1-dB compression point(dBm)	**-12.56**	--	--
P_{dis} (mW)	**2.7**	7.2	2.7
Supply Voltage(V)	**1.2**	1.2	1.2
Technology	**0.18µm CMOS**	0.18µm CMOS	0.18µm CMOS

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