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Research paper

Improvement of SRAM stability using read and write assist techniques

Pullareddy A [1]*, G Sreenivasulu [2], R Veerabadra Chary [3]

[1] *Research Scholar, Dept. of E.C.E, Sri Venkateswara University College of Engineering, A.P ,India*
[2] *Professor, Dept. of E.C.E, Sri Venkateswara University College of Engineering, A.P ,India*
[3] *Sr.Manager, INVECAS, Ind Ltd.*
**Corresponding author E-mail: avulapullareddy@gmail.com*

Abstract

The objective of this paper is to demonstrate how to improve the read stability of the SRAM cell using the read assist technique. SRAM cell stability is the primary concern for the present and future technologies due to process variations like Vt and Vdd scaling, etc. So it requires additional circuit techniques such as write and read to assist to improve the stability of SRAM memories. To accomplish the non-destructive read operation, we need to either weaken the pass transistor or strengthen the pull-up transistor during the read operation. Towards decrease of pass transistor strength, we implemented the lower word line voltage as read assist circuit. The lower word line voltage will help the selected and un-selected columns (for higher column mux options) during a read operation. But during write operation the lowered word line voltage scheme will impact the write operation. So, in order to improve the read margin we used read assist technique at the same time to ensure that write operation is successful we combined the negative bit line write assist scheme along with read assist technique. The proposed assist circuit gain the power and read margin improvement of 10%, 30% respectively. We observed the read margin analysis at process, voltage and temperature corners.

Keywords: *Assist Circuit; Read Margin; Read Stability; SRAM; Write.*

1. Introduction

Moore's law motivates the technology scaling in order to improve the performance features such as speed, power consumption and area. Static random access memory (SRAM) is a static memory cell which is extensively used in various electronic systems. It is faster and consumes less power as compared with other memory cells. In the present day, the design of SRAM cell stability is the major challenges in SRAM memory. Increasing the technology scaling and process variability, write margin and cell stability (SNM) reduces. The definition of SRAM bitcell stability is depend on the mode of SRAM operation. In read mode, the static noise margin (SNM) is used, and it shows the measure of SRAM robustness. The SNM limits the cell stability and determines the minimum supply voltage (Vmin) of the SRAM cell. The conventional 6T SRAM cell structure is shown in the Fig. 1. It is composed of two cross-coupled inverters (M1- M4) with two pass transistors (M5, M6) connected to complementary bit-lines (BL, BLB). Both pass transistors are connected to word line (WL) to perform the access write and read operations through the bit lines. The 6T SRAM cell is operate in three modes [1]: Hold, write and read. All modes have its own operating margin. In the standby mode, the word line (WL) is applied to low voltage (GND). In order to keep its data properly, the back to back connected inverters are must sustain bi-stable operation.

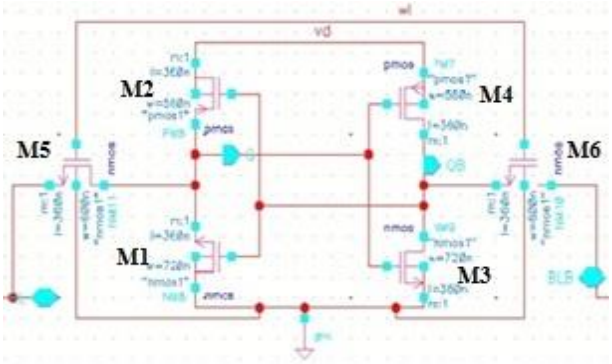

Fig. 1: Conventional 6T SRAM Cell.

When in the write mode, bit-lines are connected to opposite voltage levels through a write driver circuit. Then, with WL held high the data on bit-line written to the internal storage node of the bit cell. In read mode, the bit-lines are initially pre-charged to VDD. Then with a word-line is selected (VDD) bit-line discharges via M6 and M3 (node Q=0), so that the differential voltage develops across the bit-lines [2]. This sufficient differential voltage is apply to a sense amplifier to detect the state of the cell.
The remaining sections are organized as follows. Section II: deals with the related work. Section III: discusses the proposed circuit technique. Section IV: presents the simulation results carried out using the Cadence virtuoso tool. Section V: conclusion.

2. Related work

2.1. SRAM cell failure metrics

Mainly there are three failure modes in the SRAM cell [3]: Write-ability, readability and read stability. Write-ability failure occurs when the internal cell node voltage does not reach to the desired voltage level during a write operation. Readability failures occur when read bit lines discharge level in specified time is less than the offset of the sense amplifier. Read stability failures occurs when bit cells content flip accidentally during the read operation. The classical method of calculating SRAM cell stability is based on measuring the static noise margin (SNM) of the cross-coupled inverters in SRAM cell. The SNM is a measure of the maximum extent of noise voltage that can be allowed at the inverter nodes without flipping the cell. In the coming section, we discuss the improvement of read stability. To address the minimum voltage requirement and parametric yield loss due to SRAM failure many techniques are available. It can be characterized in the following categories: SRAM cell modifications, circuit techniques, body biasing.

2.2. SRAM cell modifications

When the SRAM cell ratios are increased the read margin value increases. As the SRAM cell ratio increases the current going through the pull-down NMOS transistor increases, and it will help in the improvement of readability of the SRAM cell. Reduced word line voltage technique increases the read margin fairly high compared to conventional 6T SRAM cell with different cell ratios. Even so, it needs an extra area in terms of transistors when compared to the proposed read assist technique.

2.3. Circuit techniques

To make a successful non-destructive read operation, one option is to reduce the strength of the pass transistor or/and strengthen the pull-up transistor during the read operation. We can improve the read margin by using one of the below mentioned read assist circuit techniques [4].

2.3.1. Lowered wordline voltage (LWL)

Word line voltage is reduced by a Vt drop using an NMOS device [5], [13]. Which is applied to the gate to source voltage of pass transistor and this voltage level is lower than the supply voltage. Therefore, the pass transistor will be weakly driven. Reducing WL voltage helps SNM, but it degrades WM for the selected bit cells.

2.3.2. Cell VDD boost (VDDB)

Supply voltage across the cell is increased above the VDD [6]. Thus, it improves the Vgs there by the strength of the pull up transistor and thus sufficiently improves read stability in read mode. However, VDD boost degrades to write margin during write mode. So, VDD boost should not be used for the selected columns during write.

2.3.3. Negative VSS

Reducing GND below the ground level improves read stability [7], [14]. Negative GND is the most effective of all readability assist techniques as it increases the Vgs on both the pull down and pass gate transistor by pulling the internal node holding '0' below ground. Unfortunately, this technique has a very high-energy cost for memory arrays, because GND lines have large capacitance.

3. Proposed circuit techniques

3.1. Lowered word line voltage read assist

Among the all above circuit techniques, the lower word line read assist circuit provides the better stability improvement. We proposed a unique design that selectively reduces the word line voltage level (WL) to less than the SRM cell supply voltage during the read mode, using a single voltage supply. Through reducing the voltage across the pass transistor, its ON current (in Fig. 1) will decrease. This will make decrease the voltage across the SRAM cell internal node (Q/QB) and, hence, increase the cell stability. As it can be seen in Fig. 2, this LWL scheme provides the lowest WL voltage at FS corner, which is the worst corner for read stability.

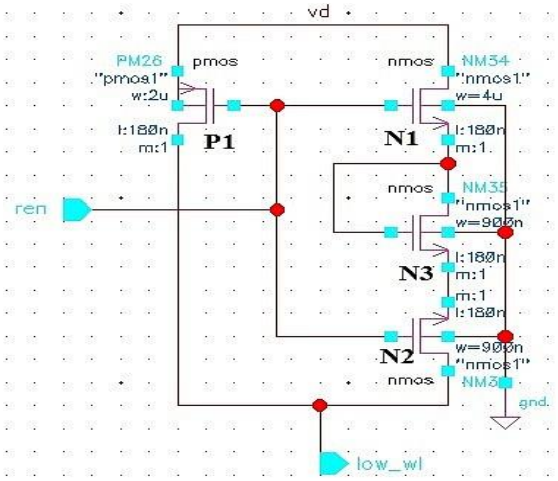

Fig. 2: Lowered Wordline Voltage Generation Read Assist Circuit.

Circuit operation: Word line voltage will be reduced by a Vt drop using an NMOS device [8]; It uses a simple diode connection (nMOS) as shown in the Fig. 2.to reduce the voltage on the word line during read operation by nMOS threshold voltage. When read enable signal 'ren' is low (i.e., write operation) then the PMOS (P1) ON and deliver exact VDD without degraded value, because the property of PMOS transistor provides strong VDD. When 'ren' is high (i.e., read operation), then NMOS transistor (N1-N3) are active and one end of the N1 transistor connected to VDD. Because the property of NMOS that it will not deliver the strong VDD, and so it provides the less than the VDD voltage (i.e. VDD-Vtn). In the same path, N3 is connected, which is a simple diode connection and its gate connected to drain. Due to this it's always ON and diode ON resistance exists on it. Since there is a voltage drop across the resistance and hence the voltage is further reduced. Now, again this reduced voltage connected to one end of the N2 transistor, the other end of N2 is taken as lowered word line voltage. Here the transistor N3 which is a MOS diode will reduce the voltage level. We can add more transistors (N-only) for more voltage reduction. Read assist circuit will be placed in the word line driver area. This proposal is simple to implement and has a low overhead in terms of area, power, and speed.

3.2. Need of negative bit line voltage write assist with reduced word line voltage

As we are reducing the wordline voltage level by using the read assist circuit it will reduce the wordline voltage of both the selected and un-selected columns (for cmux is equal to or greater than 2). The un-selected columns will be in read mode so the reduced word line voltage will help in improving the read margin. Even so, if we want to do the write operation in the selected column, then the reduced word line voltage will impact the write operation. So, in order to improve the write-ability of the selected column we need to use the write assist circuit [1]. The combination of read assist and write assist circuits will improve both read margin and write-ability. Fig. 3 represents the negative bit line write assist circuit used to generate the negative bias voltage across the bit lines for improving the write-ability.

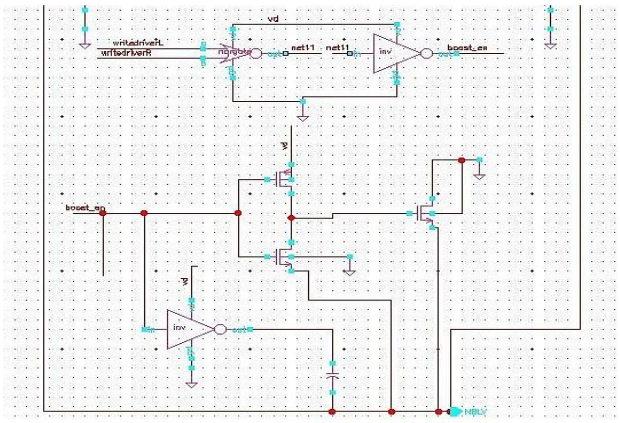

Fig. 3: Generation of Negative Voltage Write to Assist Circuit.

3.3. Negative bitline voltage write assist

One of the best writes assist circuit techniques to combine with read assist is the Negative Bit-line Scheme. The principle behind this approach is that bit line voltage is pulled into negative (below ground potential), which will increase the strength (Vgs) of the pass transistor [9]. With the increased Vgs, the pass transistor will discharge the cell node "1" below the Vtp of the cross-coupled PMOS of the SRAM latch, which ensures proper write operation of the bit cell. At low power supply applications the conventional SRAM memory couldn't complete the write operation within the specified word line pulse width due to the lower Vgs or lower drive-ability on pass transistor [10].

The proposed negative bit line voltage writes assist circuit scheme will help the write operation at reduced word line pulse width at lower power supply. Fig. 3 shows the negative bit line circuit technique for expanding the write margin. Making use of a self-determining circuitry as for the BL and BLB, it is essential to adjust the timing of forcing one of them to a negative bias. It includes write assist enable circuit, boosting capacitor (Cboost), connected to bit-lines BL and BLB, and inverter circuit. When the boost_en signal is high, then the write assist circuit enabled. The negative bit line (NBL) voltage circuit will generate the negative bias, and it will couple the negative voltage across the bit line, whichever is discharging thereby it pulls the bit line voltage to a negative level. The amount of negative voltage levels on bit line to depend on the boost capacitance (Cboost) Vs bit line capacitance (CBL). More the bit line capacitance less will be the negative boost level. Similarly, more the boost capacitance higher the negative bit line levels. Therefore, negative bit line voltage level depends on ratio of Cboost / (Cboost+ CBL).

This negative bit line voltage helps for the faster discharge of the SRAM cell node "1" and improves the write-ability operation. We need to ensure that the negative bit line voltage level should not create any false write operation on the half-selected bit cells [11]. Also the negative bit line level should not create any reliability issues for the pass transistor due to higher Vgs [12]. If, the boost_en signal is low the write assist circuit is disabled and both the bit lines are connected to the pre-charged voltage level of VDD.

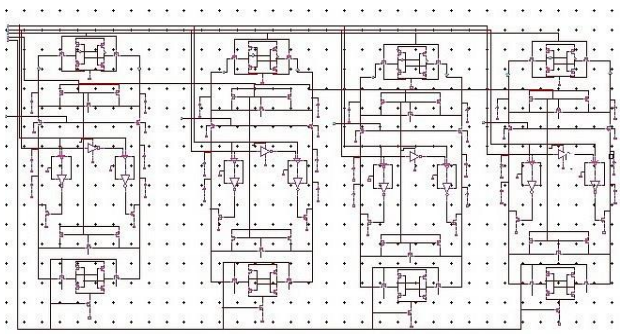

Fig. 4: One Row of SRAM.

Fig. 4 represents part of the SRAM array using the read assist circuit. It consists of lowered wordline voltage read assist circuit, negative bit line writes assist circuit and four SRAM cells. Columns are separated by CSEL (column selection) signal represented as CSEL_0, 1, 2 and 3 with common wordline, this can be exposed at simulation waveforms. Single column has pre-charge circuit, write driver and sense amplifier circuit. Common WL is used to enable the write or read operation. When WL, CSEL and WE (write enable) signals are high, then the input data (Din) written into the SRAM cell as shown in the Fig. 5. When we provide the sense amplifier enable signal 'SEN' to be high, then the bit lines are in read mode and data available at the cell node is observed at the sense amplifier output.

4. Experimental results

The Simulation for the proposed read assist technique is performed in Cadence tool with a supply voltage of 1. 2V. The stability of the cell is compared with conventional and proposed read assist circuit. The effect of temperature and threshold voltages (process corners) on the read margin value observed. Fig. 5 shown the simulation waveform of the SRAM array using without read assist circuit. The first three signals are represented as data input 'Din', write enable signal 'WE' and word line signal 'WL'. The SRAM cell internal nodes are denoted by 'Q' and 'QB'. The first two pulses of the word line represent the write operation and third pulse used in the read operation. Here we observed that when first column is selected (CSEL_0 is high) for write/read operation, other columns are unselected (CSEL_1, 2, 3 is low). During the read operation unselected column cell node levels are changed, this was undesirable and known as readability failure. It can be shown in the Fig. 5.

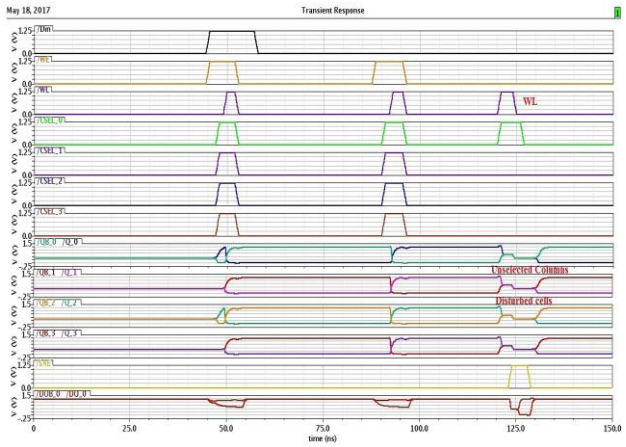

Fig. 5: Simulation Waveform of SRAM Array without Read Assist Circuit.

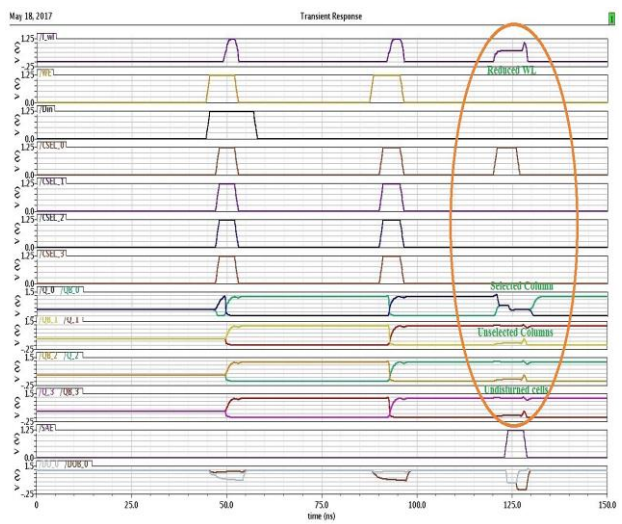

Fig. 6: Simulation Waveform of SRAM Array with Read Assist Circuit.

Fig. 6 shows the simulation waveform of one row of the SRAM array using the lowered word line voltage read assist circuit. The first signal 'l_wl' represents the reduced word line voltage. During the write operation the lowered word line voltage (l_wl) will impact the write operation (i.e. write-ability issue), it overcomes by using the negative bit line write assist technique for the selected write operation. In read mode, the word line voltage is reduced i.e. the third pulse of l_wl signal. It is applied to unselected column, and hence the cell's node are not disturbed, so it improves the read margin of the SRAM cell, i.e., the cell nodes of the SRAM do not flip in the read operation as it can be observed in Fig. 6.

Table 1: Comparison of Calculated Parameters with Conventional and Proposed Method

Parameter	Conventional method	Proposed method
Power (uw)	58.03	53.02
Delay (ns)	39.06	40.03
Wordline volage (v)	1.2	0.7

The key parameters such as performance, power and read margin values are measured for both conventional and proposed assist circuit techniques summarized in table 1. From the table 1, proposed lowered wordline read assist circuit gain the power and read margin improvement of 10%, 30% respectively. But the performance is effected at the cost of 3% reduction.

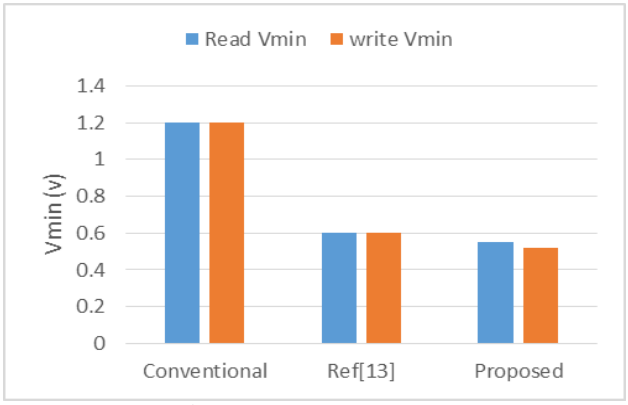

Fig. 7: Impact of Read and Write Assist Techniques on Vmin.

Fig. 7 represents the analysis of read and write assist technique for minimum supply voltage (Vmin) required to SRAM cell operation. The conventional 6T SRAM cell without assist circuit techniques required Vmin is 1.2v. By applying the assist circuit techniques the Vmin is reduced from 1.2v to 0.57v for read operation and 1.2v to 0.53v for write operation.

Read Margin at PVT:

At Process Corners: Read margin of the proposed read assist technique for the different process corners include TT (True NMOS, True PMOS), SS (Slow NMOS, Slow PMOS), FS, SF and FF is measured. From the examination, it is observed that the worst read margin value is at FS corner.

At temperature variations: Read margin of the proposed technique is measured at different temperature variation from -40ºC to 120ºC. From the Fig. 8 it is observed that as the temperature increases from -40 to 120ºC the read stability of the SRAM cell is decreased.

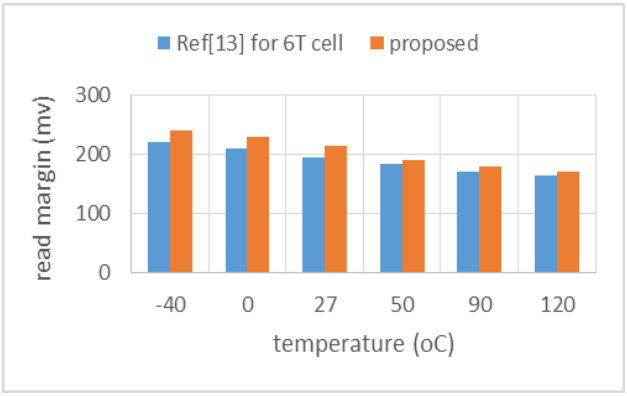

Fig. 8: Read Margin at Various Temperature Conditions.

5. Conclusion

In the proposed work read assist scheme has been analysed with lowered word line voltage during the read mode for 6T SRAM cells considering process corner and temperature variations. The proposed read assist will impact the write-ability. So, to overcome write-ability impact we developed the negative bit line voltage writes assist circuit for improvement of write-ability. We compared the experimental results of 6T SRAM cell with and without using read assist circuit technique. From the results, the proposed combination of read and write assist techniques helps the improvement of cell stability and write-ability. The proposed combination not only helps in the stability enhancement of the memory cell, but it also impacts on SRAM cell Vmin, i.e. the value of Vmin is low compare with other methods. The energy consumption of the developed circuit scheme is less compared with other techniques. Furthermore, the proposed technique validates higher read margin, and it makes a better alternative in nanometre technologies for SRAM read stability. It has been observed that the worst-case read margin is with Fast NMOS and Slow PMOS (FS), high read margin value at SS process corner.

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