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Low power and high speed D-latch circuit designs based on carbon nanotube FET

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Abstract

In this paper we propose low power and high speed D-latch circuits, base on carbon nanotube field effect transistor. D-latches are the important state-holding elements and systems performance enhancement will be achieved by improving the flip-flop latches structure. The circuit designs are simulated by HSPICE .In this paper the consumption result of the circuit parameters such as delay, power and PDP for our three different D-latch circuit design in various voltages and different temperatures.

Keywords: Carbon Nanot*ube; Carbon Nanotube Field Effect Transistor; D-latch; High speed; low power.*

1 Introduction

Using MOSFET technology to approach the novel circuit designs will be encountered our circuit to achieved the worse area, delay and power consumption ,so that we should replace the ancient silicon technology with a new nanotube technology with a nanometer dimensions also have better delay and power consumption[1],[2].Carbon nanotube field effect transistors with excellent properties such as high carrier mobility to near ballistic transport and high carrier velocity for fast switching is a promising candidate for silicon technology. CNTs are graphene sheets rolled into cylindrical and the direction of wrapping graphene is chirality [3]. The diameter of carbon nanotube the can be expressed as [4]:

$$D_{CNT} = \frac{a\sqrt{n^2 + m + m^2}}{\pi}$$

Where (n, m) represented chirality and the bandgap of carbon nanotube is:

$$E_G = \frac{0.84}{d\,(nm)}$$

The threshold voltage of the CNFET is equal to half of the bandgap and can be expressed as:

$$V_{th} = \frac{0.84}{d\,(nm)}$$

The carbon nanotubes are used in CNTFET as a channel and two types of CNTFET are: schottky Barrier CNTFET (SB-CNTFET) and MOSFET-like CNTFET as shown fig.1.In MOSFET-like source and drain are made of doped carbon nanotubes and the intrinsic semiconducting carbon nanotubes are used in the channel region. The channel in the Schottky barrier (SB) CNTFET is a intrinsic semiconducting carbon nanotube and direct contacts of the metal with the semiconducting nanotubes are made for source and drain regions [5],[6].

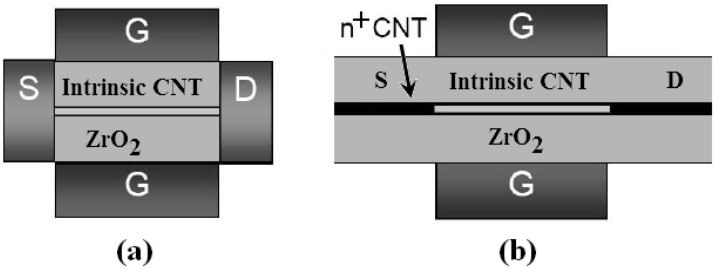


Fig. 1: (a) Schottky barrier (SB) CNTFET (b) MOSFET-like CNTFET.

2 Designs of circuit

2.1 First CNTFET circuit design

Our circuit design consists of five P-Type carbon nanotube field effect transistors and five N-Type CNTFETS. (Fig.2). If (D, clock) = (0, 0), we have "1" on the output. If input is equal to"1" when clock=0 the output is"0" .When clock is "1", when clock=1 the output node copy the last voltage so that we have the previous value on the output node. Simulation results of the first design are shown in table 1.

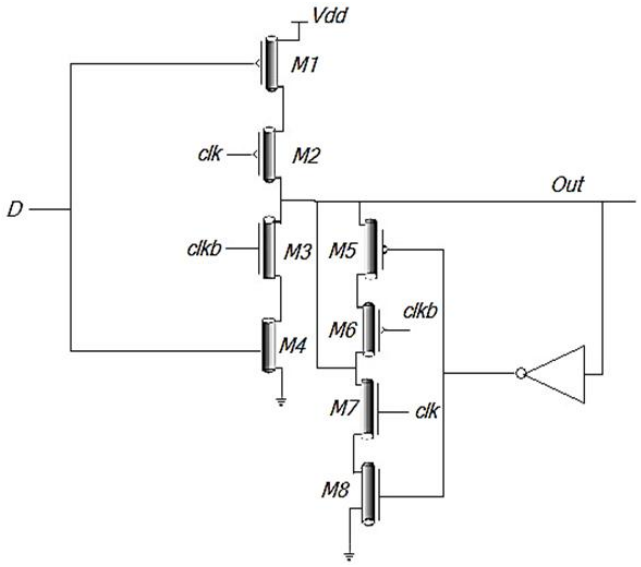


Fig.2: First CNTFET circuit design

Table.1 simulation results of the first design

Supply voltage	Delay	Power	PDP
0.6v	1.82E-12	8.41E-07	1.53E-18
0.8v	1.54E-12	1.38E-06	2.13E-18
1v	2.45E-12	2.09E-06	5.12E-18
1.2v	2.93E-11	2.79E-06	8.20E-17
1.4v	1.68E-11	3.82E-06	6.40E-17
1.6v	1.01E-11	5.10E-06	5.13E-17

2.2 Second CNTFET circuit design

In this design we have eight carbon nanotube field effect transistors.M1 and M2 are used as a transmission gate (Fig.3). When the clock is"1" M1 and M2 will be on. S is the input node therefore we have D- NOT on the output node and also when we have CLOCK ="0" M1 and M2 will be cut off and M4, M5 will be ON also we have achieved better and full swing output. The delay, power and PDP for our second design in different supply voltages are shown in Table2.

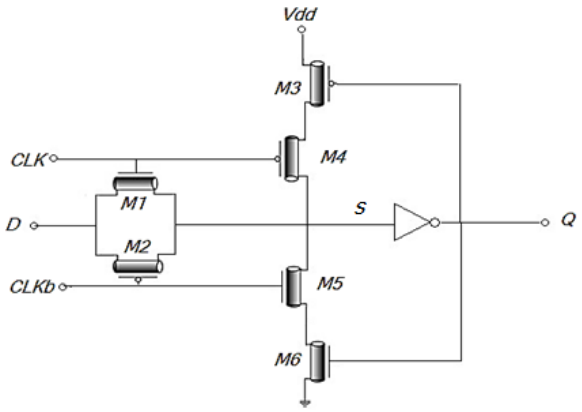


Fig.3: Second CNTFET circuit design

Table.2 simulation results of the second design

Supply voltage	Delay	Power	PDP
0.6v	3.44E-10	7.04E-08	2.42E-17
0.8v	1.17E-11	1.31E-06	1.54E-17
1v	1.87E-12	2.07E-06	3.87E-18
1.2v	5.51E-12	2.89E-06	1.59E-17
1.4v	6.92E-12	3.91E-06	2.71E-17
1.6v	9.54E-12	8.58E-06	8.19E-17

2.3 Third CNTFET circuit design

This design consist of two P-Type carbon nanotube field effect transistors and also we have two N-type CNTFETS. We use M2 and M3 as a transmission gate (Fig.4).If D and clock are equal to "1", M2 will be on and we have "0" on the output node .If (D , clock)=(0,1), M3 will be on and we have "1" on the output . If D="1" when clock=0 M2 will be on and we have output="1" .If D and clock are equal to "0" M3 will be on and we have "0" on the output node. Simulation results of the third designs in different voltages are listed in table.3.

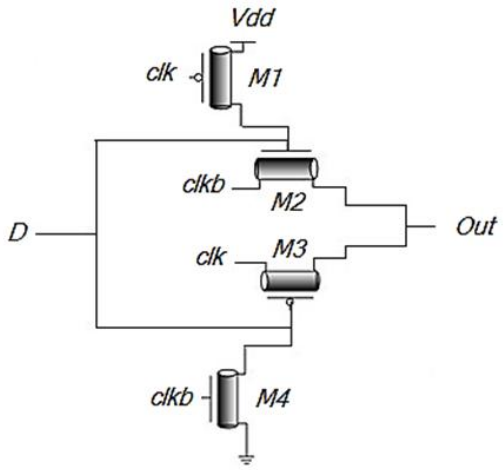


Fig.4: Third CNTFET circuit design

Table.3: simulation results of the third design

Supply voltage	Delay	Power	PDP
0.6v	7.55E-13	1.60E-06	1.21E-18
0.8v	7.53E-13	1.60E-06	1.21E-18
1v	5.75E-13	1.61E-06	9.28E-19
1.2v	9.72E-13	1.62E-06	1.57E-18
1.4v	7.79E-13	1.61E-06	1.25E-18
1.6v	5.90E-13	3.26E-06	1.92E-18

3 Simulation comparisons

All the circuits are simulated by using the compact model [7],[8] in HSPICE. All the circuit parameters such as power consumption, delay and power delay product (PDP) in different voltages and different temperatures (0°C to 100°C) are achieved .Fig.(5,6) and 7 show the comparison results of our three D-latch circuit designs, proposed based on carbon nanotube field effect transistors.

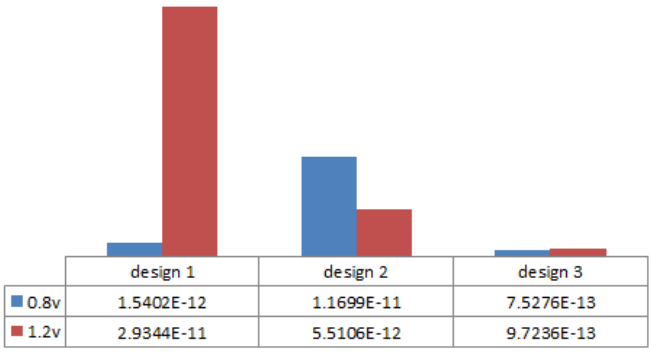


Fig. 5: Delay comparison chart for 0.8v and 1.2v

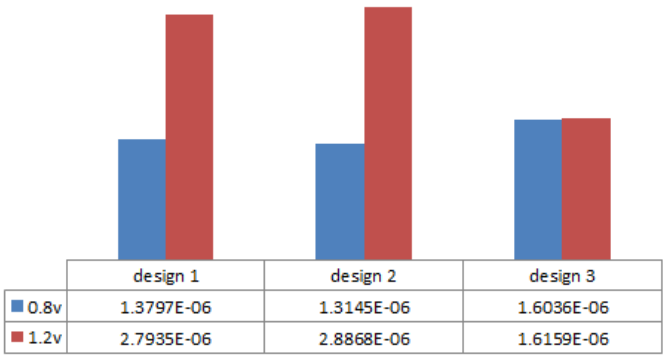
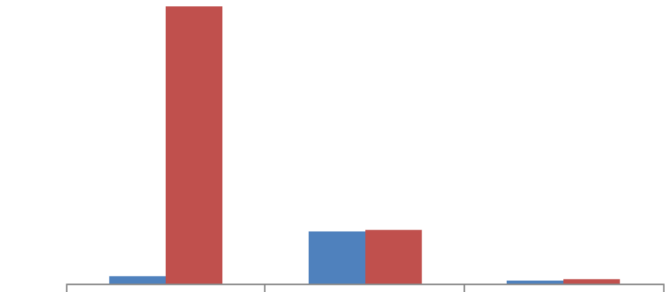


Fig. 6: Power comparison chart for 0.8v and 1.2v



	design 1	design 2	design 3
0.8v	2.125E-18	1.5378E-17	1.2071E-18
1.2v	8.1972E-17	1.5908E-17	1.5712E-18

Fig. 7: PDP comparison chart for 0.8 and 1.2v

4 Conclusion

In this paper we presented three different designs of D-latch. The simulations show that by using carbon nanotube field effect transistors we have achieved a significant improvement in delay, power and power delay product. The results in different voltages (0.6, 0. 8, 1, 1.2 and 1.6) leads in that have the best performance in our third circuit design. Simulation results of different temperatures (0°C-100°C) shows that we do not have any prominent change in delay, power and power delay product.

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