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Research Paper

Software defined radio platform with wideband tunable front end

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Abstract

The paper presents a Software Defined Radio (SDR) development platform with wideband tunable RF (Radio Frequency) front end. The platform is based on the SB3500 Multicore Multithreaded Vector Processor and it is intended to be used for a wide variety of communication protocols as: Time Division Duplexing/Frequency Division Duplexing Long Term Evolution (TDD/FDD LTE), Global Positioning System (GPS), Global System for Mobile/General Packet Radio Service (GSM/GPRS), Wireless Local Area Network (WLAN), Legacy Worldwide Interoperability for Microwave Access (WiMAX). As an example, we describe briefly the implementation of the LTE TDD/FDD communication protocol. As far as we know, this is the only LTE category 1 communication protocol entirely developed and executed in software (SW), without any hardware (HW) accelerators.

Keywords: *Multicore Processing; Parallel Programming; Software Radio.*

1. Introduction

For the last few years, as processors became more and more powerful, being capable of executing multiples of billions of operations per second, power efficiently, the SDR has become reality, marking the beginning of a new era in the wireless communication arena. Some of the most significant and incontestable advantages of the SDR are enumerated in sequel:

1) Reconfigurable and more flexible communication protocols. Specific functions as filters, modulation schemes, encoders/decoders etc. can be reconfigured adaptively at run time.
2) Several communication protocols can be stores in the nonvolatile memory and also can coexist in certain conditions. The possibility of using the same HW platform for running totally different communication protocols offers significant versatility and cost saving for the end user as well as for the service provider.
3) Remotely reconfigurable, providing easy and inexpensive SW versions control, and also an easy way of adding new features.
4) Development time is significantly reduced providing an accelerated time to market.
5) It provides the most attractive way of dealing with new standard releases and in the mean time assures the backward compatibility.

Most of the existing SDR platforms are built around a combination of processors and FPGAs, making the development rather complicated. Multiple software development and simulation tools need to be used together to develop and validate one specific communication protocols. Our platform provides a simple solution, consisting of one digital signal processor (DSP), the SB3500, and C based software development tools, all developed by the same team. Our development platform has only two major building blocks, the front end RF transceiver and the SB3500 System on Chip (SoC). The data converters are incorporated in the RF transceiver.

2. The hardware

2.1. The SB3500 sistem on chip

The SB3500 consists of 3 Sandblaster Extended (SBX) 2.0 DSP Architecture Cores, depicted in Fig. 1. The core attributes are as follows:

- 600MHz clock rate
- 4-way threaded
- 32KB I-cache
- 256KB D-memory
- Wide Vector Unit – 256b; 16, 16b Multipliers; 9600 MMAC/s

HSN (High Speed Synchronous Network) interconnect

- point-to-point ring
- 2.4GBs/link

ARM926EJ-S

- 300MHz clock rate
- 16KB/16KB cache
- 32KB/16KB Tightly Coupled Memory (TCM)

The chip (65nm LP) has been in production since the fourth quarter of 2009.

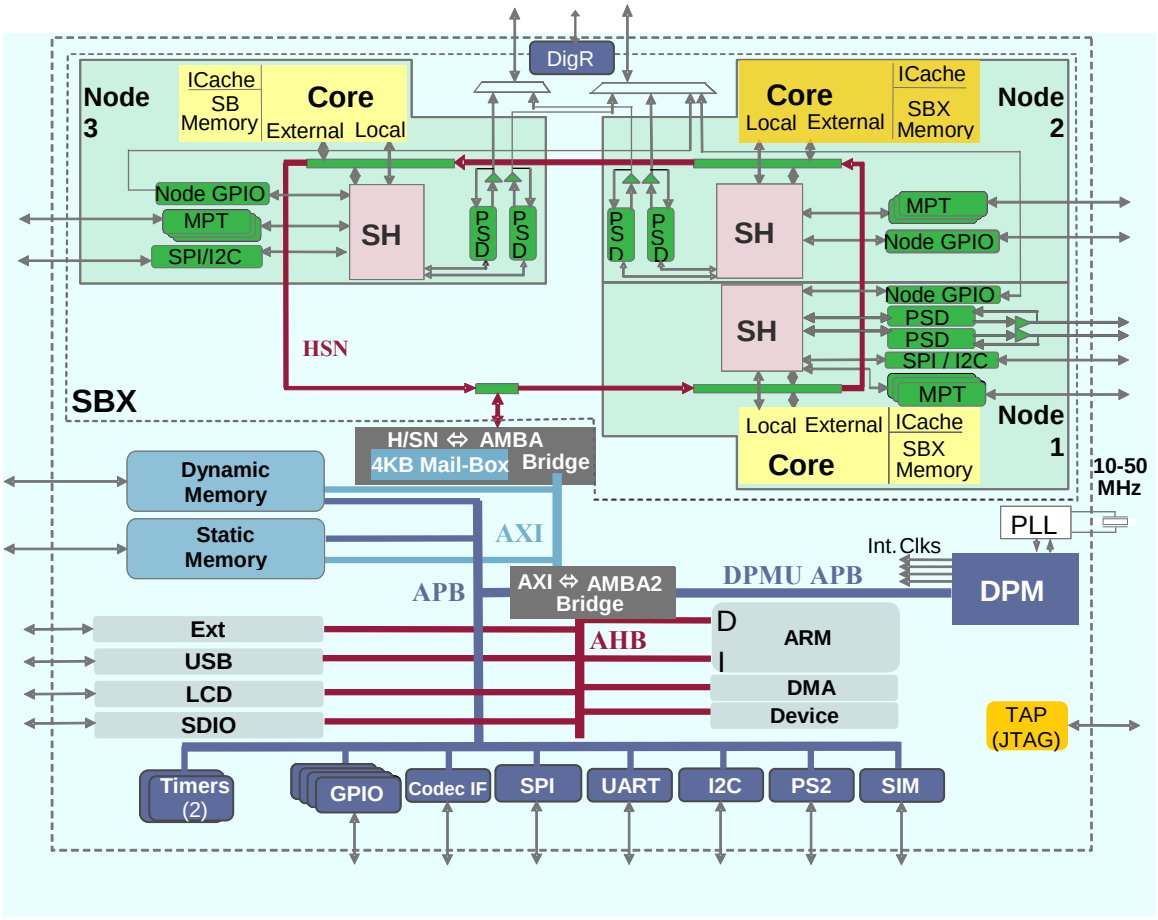

Fig. 1: Sandblaster SB3500 Soc Diagram

The SOC has incorporated most of the peripherals required for a modern communication, fixed or mobile, device. The chip features are depicted in Table 1.

Table 1: Sandblaster SB35000 Features

High Performance, Low-Power Design	Three SandBlaster® Extended (SBX) DSP Cores
1.2 V +/- 10% Core Voltage 65-nm Low Power Technology 2.5 / 1.8 V +/- 10% Input/Output Voltage	Four Hardware Threads per Core 32K-Bytes Instruction Cache per Core 256K-Bytes Data Memory per Core 9.6 Billion MACs per Core @ 600MHz operation
Integrated ARM926EJ-S Processor 16K-Bytes, each Instruction & Data Cache 16K-Bytes/32K-Bytes Instruction & Data TCM	Timers 4x32-Bit Timers per Sandblaster® Core 3x24-Bit, Timers/Pulse Generators Per Sandblaster® Core, cascade-able and configurable for external system clock operation 2xGlobal 32-Bit general purpose Timers Real-Time Clock (RTC) SoC Watchdog Timer Power Management control timers, for event processing
DMA Controllers 12 SBX Direct Memory Accesses, one Per Thread ARM Bus DMA, multi-channel	Configurable Dynamic and Static Memory Controllers Supports Synchronous: MDDR, SRAM Supports Asynchronous: SRAM, ROM, NOR/NAND Flash
Configurable I/O 2GB External Address Space 32 Dedicated GPIOs, plus 64 multifunction I/Os	Serial Peripherals Five SPI™, each with multi-address selects Five I2C™ interfaces SDIO Master & Slave Interfaces PS2 Interface (Mouse, Keyboard)
UARTS Two UARTs, one configurable for IRDA (115 Kbps)	Camera Interface 8-bit/10-bit interface with internal queue
LCD Controller Up to 1024 x 768 Resolution Supports STN, Color STN (super-twisted nematic), high reflective (HR)- thin-film-transistor (TFT), TFT Up to 64K-Colors and 15 Gray Shades Pointer overlay	Dedicated RF Data Interfaces Four 16-bit Parallel Ports (Programmable for UL or DL data) DigRF Version 3.09 baseband interface
Other features Programmable Interrupt Controller USB On The Go (OTG) Interface AC '97 / I2S Codec Interface with S/PDIF support Smart Memory Card Interface Keypad Interface Integrated Device Power Management Unit Commercial BGA Package 13mm x 13mm	External Communications Interface 4K x 16-bit DP memory interface for communications with optional Applications Processor

2.2. The RF transciever

The analog RF front end is a Multistandard 3G/4G transceiver provided by Maxim Semiconductor Inc [1]. The chip block diagram and features are presented in Fig. 2 and Table 2 respectively.

Table 2: Maxim Transceiver Features.

TDD / FDD LTE Support
IF Amplifiers
Data Converters
Channel Selection Filters
Decimation/Interpolation Filters
Fractional N Synthesizer
Selectable Bandwidth
All TX/RX LTE Bandwidth

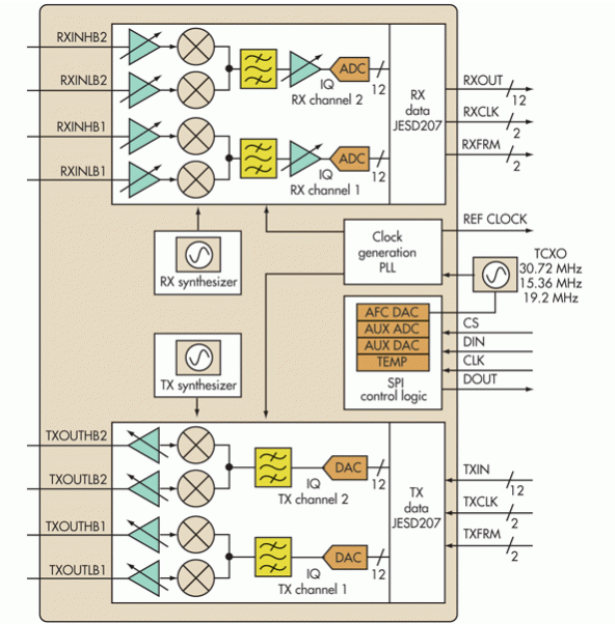

Fig. 2: Maxim Multistandard 3G/4G Transceiver [2].

2.3. The OST (optimum semiconductor tech.) SDR card

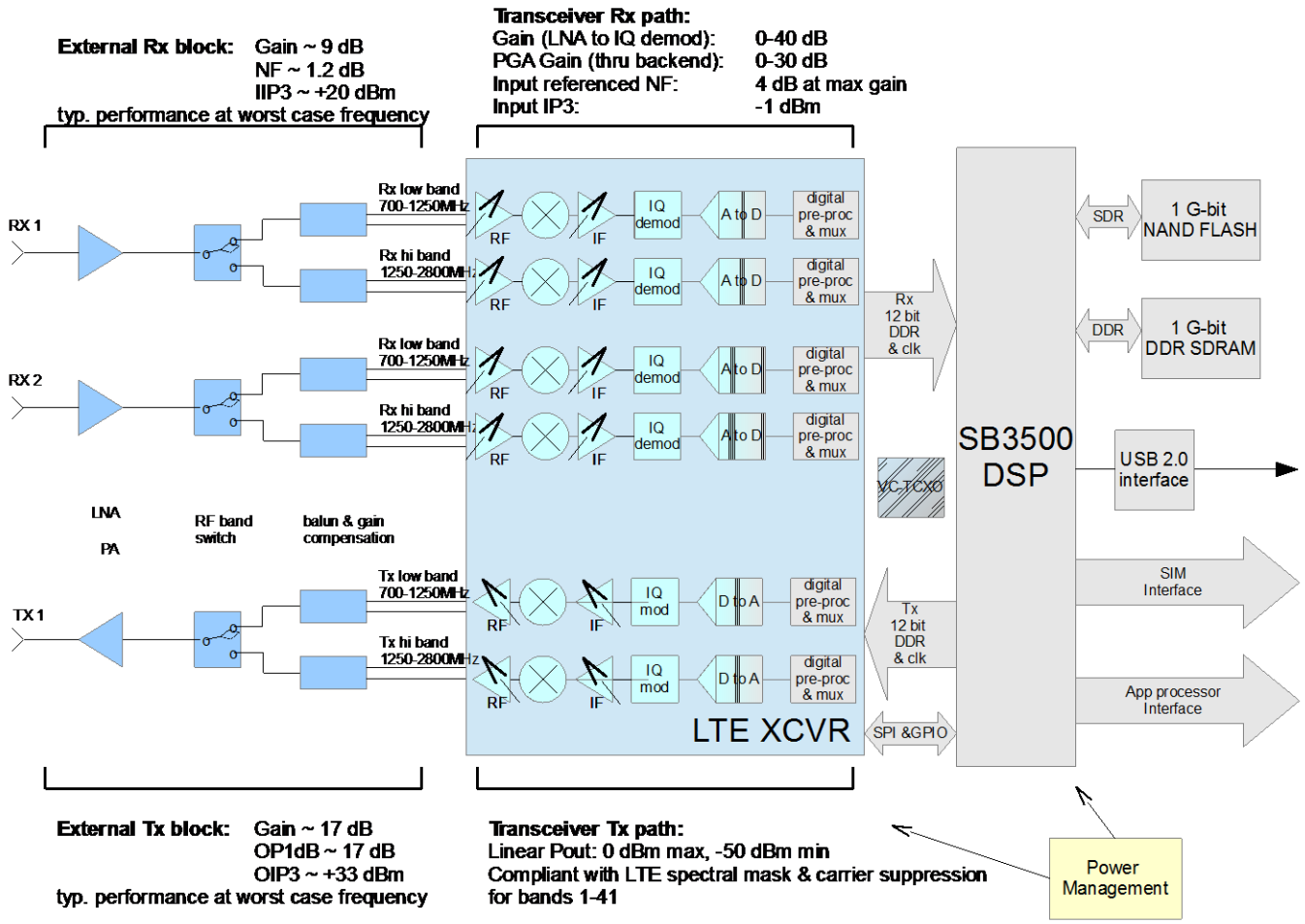

Fig. 3: The Simplified OST SDR Card Diagram.

The basic block diagram of the SDR card is presented in Fig. 3. It consists of two major blocks, the RF transceiver and the DSP interfaced through parallel data path. This SDR card represents an evolution of a previous design, presented in great details in reference [3]. Fig. 4 illustrates the OST SDR card with the following features:

- SB3500 Baseband processor: provides physical layer (PHY) and stack layer processing, 128MBytes external DDR, 128MBytes external Nand-Flash
- MAX2580, configurable RF Transceiver; dual RX SMA ports; single TX SMA port; TDD or FDD operation; optional external reference clock SMA port
- USB 2.0 OTG device interface: connection to Host PC, as user interface; SIM card interface
- Dual UARTS on external connector
- SB3500 Integrated Development Environment (IDE) port for diagnostic and DSP SW debugging; SB3500 ARM JTAG port
- Connector with external interface communications to SB3500 device
- 16-bit interface to SB3500 dual port static memory
- Housed in 4 x 2 x 1 inch form factor

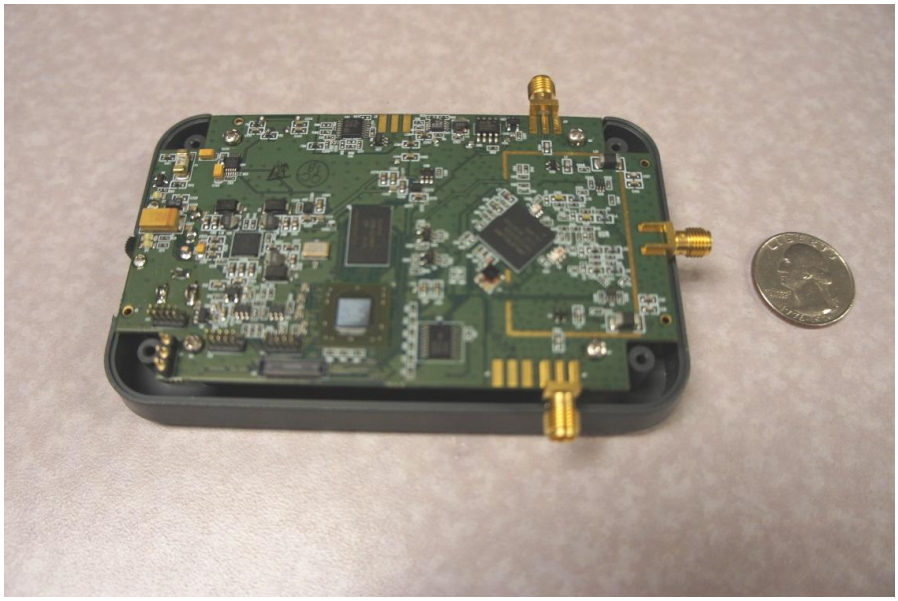

Fig. 4: The OSD SDR Card Top View

3. The LTE system implementation

TDD-LTE and FDD-LTE are based on Orthogonal Frequency Division Multiplexing (OFDM). In an OFDM system, the spectrum is divided into orthogonal sub-carriers. Each of the sub-carriers is modulated by a low rate data stream. The sub-carrier spacing is fixed to be 15 KHz or 7.5 KHz for Multimedia Broadcast Multicast Service (MBMS). One of the key advantages in OFDM systems is the robustness against multipath delay spread. The OFDM symbols allow the introduction of a guard period between each symbol to eliminate inter symbol interference due to multipath delay spread. Details on the implementation and performance of the LTE in the SB3500 processor can be found in [4].
For the interested reader, more details about the LTE communication protocol and practical design, implementation and testing issues, in general, can be found in references [5-11]. In the following, we will describe, only briefly, our implementation. The current implementation supports dual mode, FDD and TDD. It can operate in SISO (Single Input Single Output) or 2x2 MIMO (Multiple Input Multiple Output) modes. The bandwidth support is for 1.4MHz, 3MHz, 5MHz, 10MHz, and 20MHz with complete PHY, supporting all required LTE channels. The LTE partitioning diagram on SB3500 processor and number of threads allocation is represented in Fig. 5.

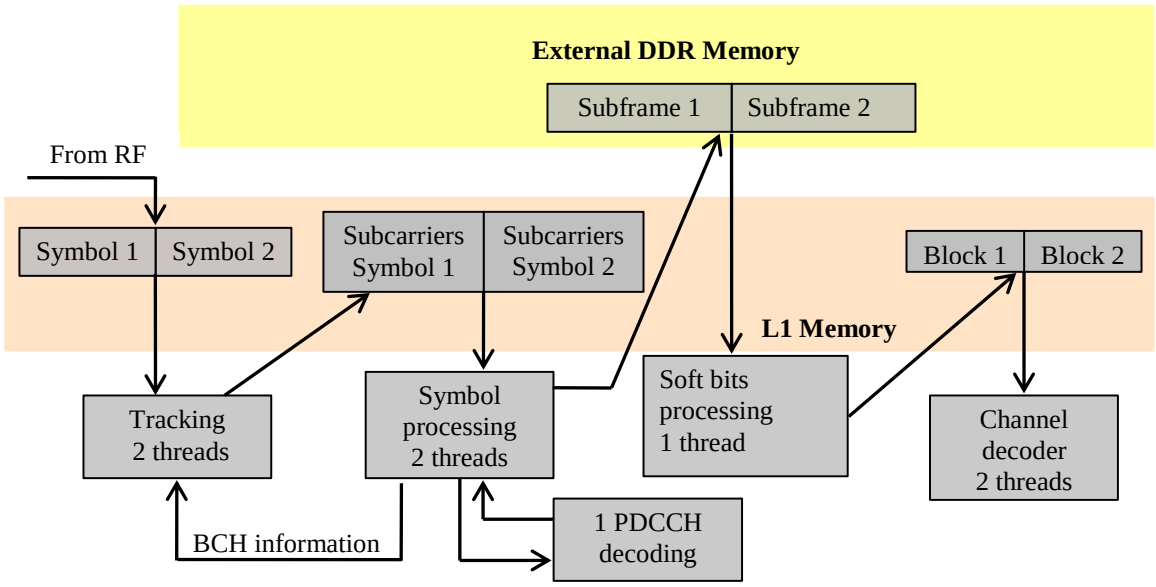

Fig. 5: LTE Partitioning on SB3500

Data from the A/D is saved in the L1 memory, two symbols at a time, and processed in parallel by multiple threads as shown in the figure 5. The L1 memory also holds the subcarrier data and two data blocks required by the channel decoder. The sub-frame data, due to its large size, is kept in the external memory. In the figure, BCH stands for Broadcast Channel while PDCCH for Physical Downlink Control Channel.

4. Results and discussion

LTE Modem Statistics

Cell Search		BCH		PCFICH		PHICH	
Cell ID	0	Phase	0	CFI	2	Mu	2
CP Mode	0	Mu	2	NReg	240	Phich Duration	0
Timing Offset	-4	Phich Duration	0	NCce	26	Decoded Phich	0x3
Samples Frequency Offset	2 Hz	NRB	50	Control Size	2		

PDCCH

PDCCH Detected	10002	PDCCH Undetected	2	PDCCH FER	0.01 %
Format 1A DCI Pass/Fail	5000/0	Format 0 DCI Pass/Fail	5002/2		

DCI Format 1A				DCI Format 0			
Format	1	VRB Type	0	Format	0	Hopping	0
HARQ ID	0	NDI	0	hop_n_prb	0	allocnum	11
RV	0	TPC	0	Mod	2	TPC	0
AllocNumBits	11	NGap	0	N_PRB	18	CyclicShift	0
l_crb	50	Mod	4	UL Index	0	AssignIndex	0
TBS	9912			CQI	0	TBS	2536

PDSCH

Physical Bits	28080	CRC Passed	4995	CRC Failed	5	FER	0.1 %
Peak Throughput	**27376 kbps**	Average Throughput	**14624 Kbps**				

Fig. 6: LTE Test Mode Snapshot

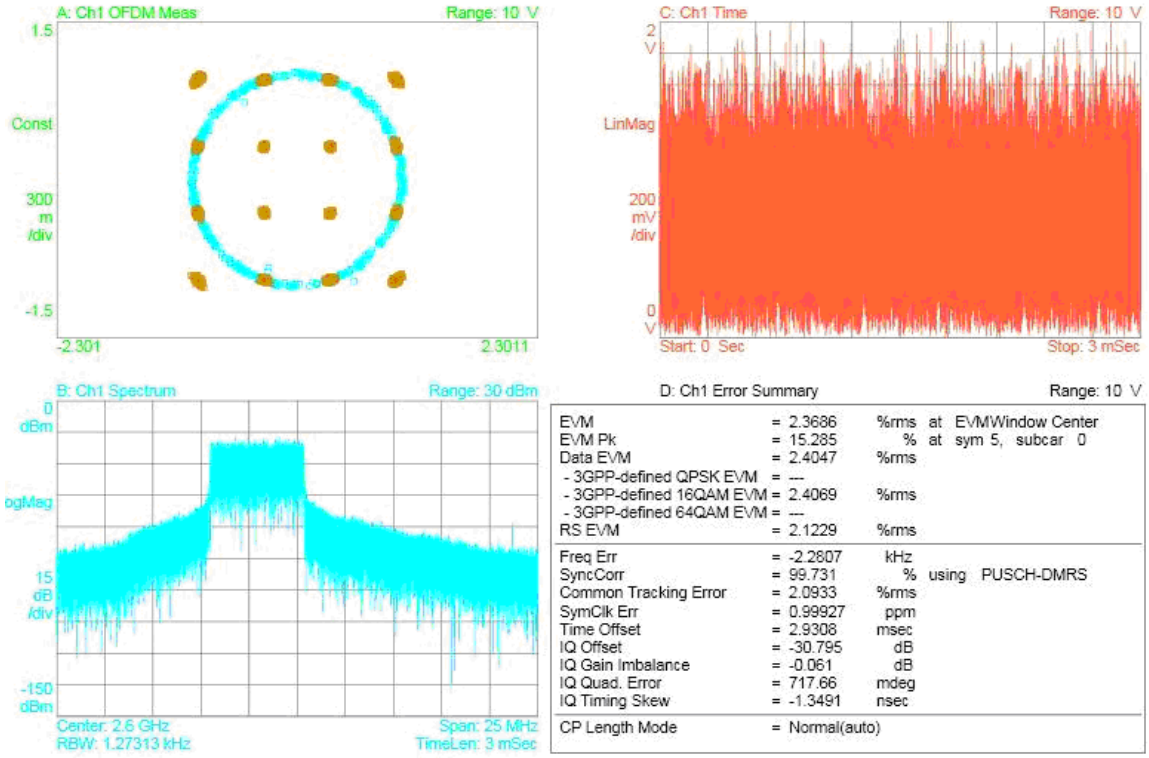

Fig. 7: Snapshot From Agilent MXK N9026A Signal Analyzer

Fig. 6 shows a screen capture of one of the real time test modes, running at 27Mbps peak and 14.6 Mbps average data rate down link in single receive mode. A snapshot from the Agilent MXK 9026A signal analyzer shows in Fig.7 the average Error Vector Magnitude at 3.3% in 16QAM modulation mode, well beyond the 3GPP Release 8 requirements for LTE.

5. Conclusion

Our multimode SDR development platform is capable of executing most of the existing commercial and military communication protocols up to 25Mbps peak rate on the downlink and up to 10Mbps peak rate on the uplink. Also, another advantage is that multiple communication protocols may coexist on the same communication device, in the external memory. The unit can be reconfigured on the fly based upon radio frequency spectrum availability and/or propagation conditions. It provides an integrated SW/HW development platform dramatically reducing the development time and implicitly the time to market.

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