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Research paper

Efficient design of a reversible 2-to-4 decoder in quantum dot cellular automata using Toffoli gates

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Abstract

This research presents an optimized design of a 2-to-4 decoder in Quantum-dot Cellular Automata (QCA) using a new formula developed from the Reversible logic. The proposed QCA decoder architecture employs 112 cells and occupies an area of 0.13μm², achieving a significant reduction in size compared to previous designs. The circuit is designed using a single-layer approach, enhancing its efficiency and minimizing power dissipation. Simulation results using the QCA Designer simulator version 2.0.3 demonstrate the enhanced functionality of the suggested decoder in regard to functionality and also efficiency, making it a promising candidate for future nanoscale integrated circuit applications.

Keywords:*Decoder, Reversible Gate;Quantum-Dot Cellular Automata;QCA Designer Simulator;Toffoli Gate.*

1. Introduction

For the last few decades, CMOS technology is commonly used as the preferred option for implementing very large-scale integrated circuits[1], [2], [3]. The concept of system portability is being achieved using new circuit design concepts that focus on minimal power dissipation, high device density, and small dimensions [4] . Motivated by Moore's law, recent decades have seen a continued trend of CMOS-based device shrinkage. This trend faces a number of unique and difficult challenges, especially as these devices show an increasing resistance to further scaling [5]. The challenges encountered in downsizing MOS structures in CMOS technology provide an incentive for investigating nanotechnology. Short channel effects, tunneling phenomena, and increased power consumption and delay are all potential consequences of shrinking MOS components. These difficulties highlight the necessity of identifying substitutes for conventional CMOS technology [6]. Quantum-dot Cellular Automata (QCA) is considered CMOS technology's replacement. Considering its comparatively tiny molecular or atomic dimension, exceptionally low power consumption, and fast switching [7], [8], [9], [10]. The QCA technology is transistorless; it does not use electrical current and transforms information through the Coulomb interactions between electrons in quantum cells [11], [1]. One of the greatest challenges in conventional electronics has long been heat dissipation. Landauer demonstrated in [12] how heat dissipation results from bit erasure. Reversibility has been proposed as a way to address this problem in conventional irreversible logic [13], [14].

A decoder is a kind of combinational digital circuit that selects a line from the 2n lines of output according to the combination among then input lines [15]. [6] presented an effective 2-to-4 decoder that was successfully implemented in QCA and built usingthree-input majority voters.The layout is improved by significantly lowering the amount of QCA wire crossings and cell numbers. The suggested decoder makes use of clock phasing and single-layer wire crossing, requiring 212 cells in a 0.25μm^2 region. The MV32 gate forms the foundation for the creative idea used in the creation of the suggested QCA decoder. In the work of [16], only three 3-input majority gates and three inverter gates were employed. There exist two single-layer and three-layer implementations for the proposed 2-to-4 QCA decoder; they require three and four clock cycles, respectively, and only use 56 and 62 cells. In a different work, [1] uses a new fault-tolerant three-input majority gate to offer a dependable and efficient coplanar 2-to-4 decoder. The proposed majority gate has eleven straightforward QCA cells in its design. The proposed majority gate has an area of 0.01 μm2 and an energy consumption of 1.49×2-2 MeV, respectively. The development and evaluation of a reversible decoder to reduce information loss and thereby heat dissipation are examined in [17]. This design utilizes popular quantum gates, including the Toffoli, CNOT, and Pauli X gates. Different configurations of decoders are investigated regarding garbage output, ancilla input and quantum cost, delay, along with other metrics.

In [14], three brand-new reversible gates are introduced that are capable of handling many logical processes at once. This study demonstrates updated circuits for 3-to-8 and 2-to-4 decoders, as well as the two distinct general decoder designs that make use of these gates. In connection to their performances, the suggested decoder circuits' power, hardware complexity, ancilla inputs, garbage outputs, and gate count are all studied. However, it is noted that the circuitry for the 2:4 decoder has been constructed differently, utilizing a variety of irreversible gates, and simulated using a QCA simulator. There seem to be some inherent issues with this technology, such as increased power usage and possible information loss. Irreversible gates may lead to inefficiency and uncertainty in the decoding process since they do not ensure a direct mapping of inputs to outputs. The irreversible nature of these gates causes ambiguity since different input states

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may map to the same output state, potentially resulting in information loss. The impact of information loss and its consequences, such as increased power consumption, may not be fully understood when simulating circuits with irreversible gates using QCA simulators. The aforementioned observations indicate that there exists an unexplored research deficit with respect to the advancement of reversible decoders in QCA technology.

This work presents a novel 2-to-4 decoder in QCA with an innovative approach by employing the reversible Toffoli gate. A circuit known as a toffoli gate has three inputs and three outputs, and every input and output corresponds exactly to one another. The decoder architecture that is being suggested will employ four toffoli gates. QCADesigner 2.0.3 will be used to model the suggested design.

1.1. Reversible logic

A reversible logic gate is a form of logic device in which there are exactly as many inputs as there are outputs, guaranteeing a one-to-one mapping [18], [19], [20]. In this arrangement, every set of input vectors produces a distinct set of output vectors, preventing information loss and lowering power dissipation [21]. Reversible logic circuits are defined by minimum input constants, a minimal quantity of reversible gates, and a minimal quantity of garbage outputs.

Alternatively, every cell in the Quantum-dot Cellular Automata (QCA) comprises quantum dots, also known as sites positioned at the corners of a square cell. [21]. The dots contain the majority of the charge. Two mobile electrons that can tunnel between the dots are also present within the cell. It is not possible for electrons to tunnel out of cells due to potential obstacles. Due to coulombic repulsion, at the corners of the cell, there are always two free electrons positioned diagonally. [22]. A QCA with a four-dot cell with the number (site) of the quantum dot is shown in Figure 2(a). The polarization (P) of the cell is computed using equation 1 [23].

$$P = \frac{(\rho_1+\rho_3)-(\rho_2+\rho_4)}{\rho_1+\rho_2+\rho_3+\rho_4} \quad (1)$$

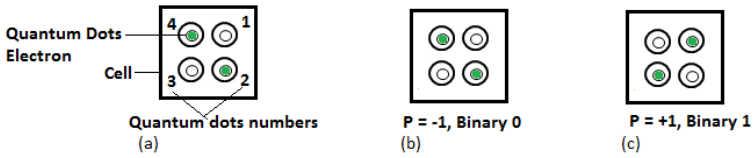

Fig. 1:QCA Cell (A) Schematic (B) with Polarization P = "-1" (C) with Polarization P = "+1". [22].

2. Methodology

A 3x3 logic circuit that can be used for reversible computing is the Toffoli gate. In the design of our 2:4 decoder, we utilized the Toffoli gate suggested in [24], which has 0.014μm² of area, a circuit complexity of 17, with a delay of 0.5 clock cycles. The relationship in Equation 2, describes the one-to-one mapping ofthe input and output. The suggested schematic logic diagram and QCA configuration for the reversible Toffoli gate are shown in Figures 2a and b, respectively. Table 1 presents a description of the Toffoli gate truth table.

$$P = A, Q = B, R = AB \oplus C \quad (2)$$

Table 1: Truth Table of Toffoli Gate

INPUT			OUTPUT		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

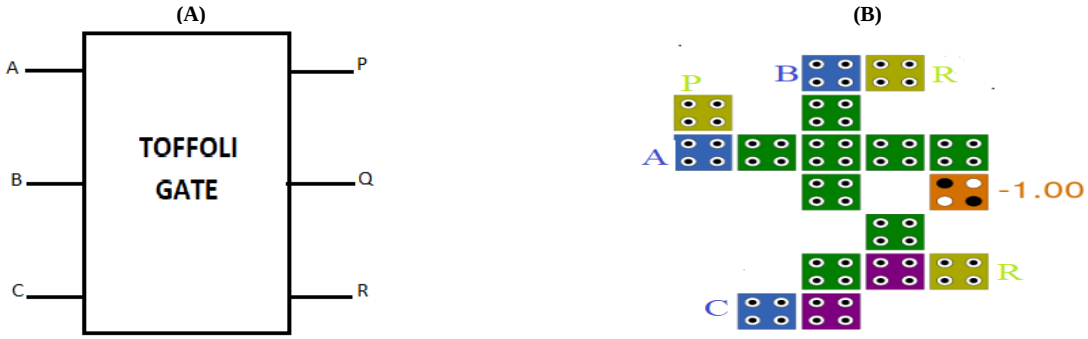

Fig. 2: (A) Proposed Toffoli Gate Logic Diagram (B) QCA Layout.

2.1. Design of 2:4 decoder

The suggested Toffoli gate cascades into a 2:4 reversible decoder, resulting in a 0.138μm² area, a circuit complexity of 112, and a 2.0 clock cycle latency. The schematic logic design and QCA layout shown in Figures 3a and b, are used to decode two-bit data. In order to detect the presence of a particular output level, this system has two input values, A and B, which are used for data transmission. Only one layer is used in the design of the entire circuit.

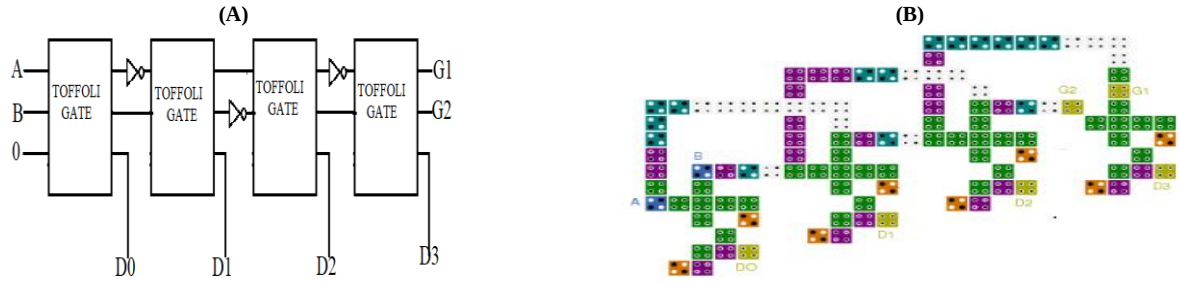

Fig. 3: (A) Proposed 2:4 Decoder Logic Diagram (B) QCA Layout.

3. Results and discussion

QCADesigner 2.0.3 was used to simulate the suggested designs, using default values for all simulation conditions and parameters as shown in Table 2.

Table 2: Applied "Bistable Approximation" Engine's Parameters within Our Simulation

Parameters	Values
Number of samples	12800
Convergence tolerance	0.00100
Radius of effect (nm)	65.000000
Relative permittivity	12.900000
Clock high	9.800000e–022
Clock low	3.800000e–023
Clock shift	0.00000e+ 000
Clock amplitude factor	2.000000
Layer separation	11.500000
Maximum iteration per sample	100
Cell width	18.0nm
Cell height	18.0nm
Dot diameter	5.0000

3.1. Simulation result of the proposed reversible toffoli gate

The simulation results of the suggested Toffoli gate are shown in Figure 4. The simulation results show that for A = 0 and B = 0, the corresponding outputs are P = 0 and Q = 0. For different values of the input data, these results are consistent with the theoretical values indicated in Table 1. Similarly, if the inputs are A= 0 and B =1, the output becomes P= 0 and Q = 1, and the process continues.

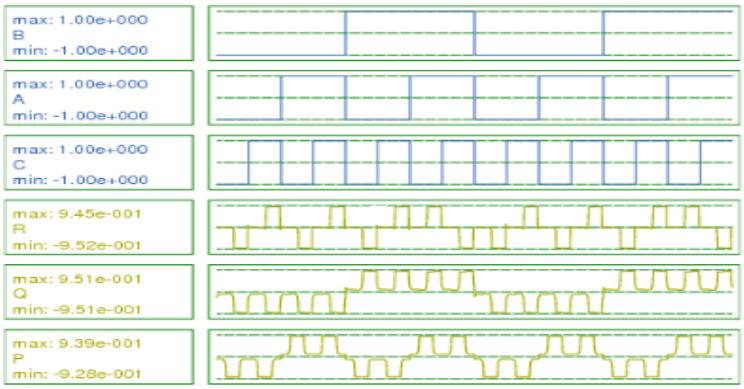

Fig. 4: Simulation Result of Toffoli Gate.

3.2. Simulation result of the proposed reversible 2:4 decoder

The proposed 2-to-4 decoder's simulated output is presented in Figure 5. All four of the input combinations A and B are accurately used in the depicted circuit to generate four outputs, D0, D1, D2, and D3 according to the truth table shown in Table 3.The simulation results demonstrate that the proposed decoder is functionally valid since only one output of the decoder has a value of one in each clock, while the other outputs are zero.

Table 3: Truth Table for 2:4 Decoder

INPUT		OUTPUT			
A	B	D0	D1	D2	D3
0	0	0	0	0	1
0	1	0	1	0	0
1	0	0	0	1	0
1	1	1	0	0	0

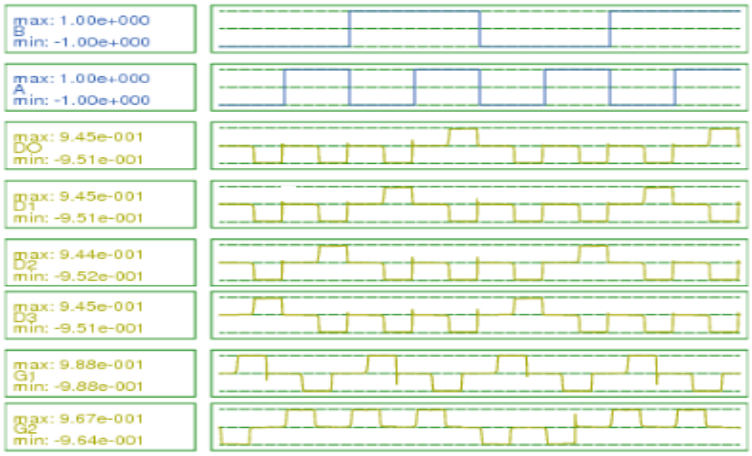

Fig. 5: Simulation Result of Reversible 2:4 Decoder.

3.3. Comparison of results

This section compares the suggested structures to the designs that are currently in use. Testing with QCADesigner version 2.0.3 confirms the proposed designs' correctness. A selection of the best-performing preceding circuits has been identified and compared to facilitate comparability. Cell count, latency, and occupied area are among the important performance metrics that are considered. A comparison of the decoder proposed in this work with decoders that have been previously introduced is shown in Table 4. Factors including the type of crossover, number of majority gates, number of cells, occupied area, and fault tolerance are all compared.

Table 4: Comparison of This Work and Related Works

Design	Number of Cell	Area(μm^2)	Layers	Reversibility
[6]	212	0.25	Single	-
[1]	137	0.05	Single	-
[8]	50	0.02	Multi-layer	-
Proposed	112	0.13	Single	✓

As can be seen, the works introduced in [1] and [6] use more cells and more area than our proposed decoder; in contrast, the work of [8] uses less cells and less area efficiently than our work because it uses multilayer designs, which raise fabrication costs. Actually, the only other concept based on a reversible gate employing a single layer is our proposed design, which has benefits for efficiency and fabrication complexity.

4. Conclusion

In conclusion, this work introduced a highly efficient 2-to-4 decoder design in QCA based on the Reversible Toffoli gate. The research addressed the growing challenges in CMOS technology, offering a viable alternative with reduced power dissipation, a smaller footprint, and faster switching characteristics. The simulation results validated the effectiveness of the proposed decoder, showcasing its superiority over previous designs. Future research directions could explore further optimizations in terms of latency, energy consumption, and fault tolerance to enhance the practicality and scalability of QCA-based circuits for advanced computing applications.

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