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Research paper

Adaptive low-power CMOS LNA in internet of things based wireless sensor networks

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Abstract

With the increasing need for the Internet of things (IoT), wireless communication has become a popular technology for the network. This explosion of IoT wireless applications makes the power consumption a key metric in the design of wireless sensor nodes. The major constraint of the wireless sensors nodes is battery energy, which is the mainly challenging problem in designing IoT network. these constraints have imposed new yet stringent specs to the design of RF front-ends. The design of adaptive radio-frequency circuits, in order to reduce power consumption, is of interest. In a RF receiver chain, the Low Noise Amplifier (LNA) stand as critical elements on the power consumption.
To address this purpose, this paper proposes a design strategy for an adaptive Low Noise Amplifier as the first element of the receiver chain. Hence the proposed LNA achieves the correct QoS for various scenario of communications. Using the proposed LNA, a significant trade-off between a conversion gain, noise figure and energy consumption is presented.

Keywords: *Internet of Things; Low Noise Amplifier; Energy Consumption.*

1. Introduction

Recently, the internet of things (IoT) is attracting lot of interest among researchers, since it can be expected to be widely used in a vast variety of applications, as illustrated in Fig.1. Using the evolution of wireless communications, traditional homes and workplaces can be transformed to smart homes or smart workplaces. Intelligence can be broadened to a whole city becoming a smart city. In the medical domain the IoT is also providing solutions to reduce medical errors [1].
The massive IoT applications need wireless sensor nodes with small form factor for an easy distribution in the environment, reduced power consumption for an extended lifetime and limited impact on the environment. This strategy of the IoT produces major challenges in the design of autonomous WSNs. The principal characteristic of such networks is nodes with limited resources and sensor nodes are typically battery powered. Under such an energy restraint condition, sensor nodes can only transmit a finite number of packages in their lifetime. Consequently, the power consumption is always considered in internet of things applications.

Fig. 1: Application Domains of the Internet of Things (Iot).

The power consumption of a sensor node is shared between the radio communication part for wireless data communication, the Micro-Controller Unit (MCU) and sensing unit which contains of one or more sensors and analog-to-digital converters (ADCs) for data acquisition [2]. For IoT applications, the radio part is one of the critical blocks in wireless sensor nodes and consumes the majority of battery

energy as depicted in Fig.2. By optimizing power consumption of this block, performance and energy requirements of the entire RF unit can be significantly improved.

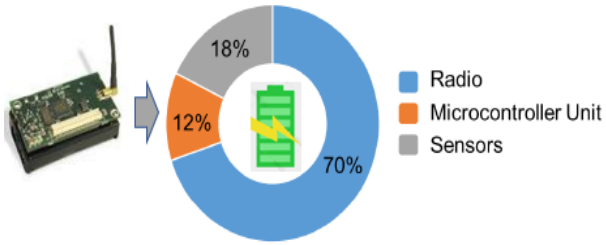

Fig. 2: Repartition of the Power Consumption in A Wireless Sensor Node.

Since, the low noise amplifier (LNA) has an important role as the first active element of the RF receiver. In this paper, we will describe the design and implementation of low-power CMOS RF LNA for 2.4- GHz-band IEEE 802.15.4 standard. There are several topologies for narrow band single ended LNA design; an appropriate topology should be selected for low power and low voltage optimized LNA design.
This paper is structured as follows: In the next two sections we summarize related work and describes the proposed LNA. Experimental results and discussions are shown in Section 4. Performances evaluation of the modified LNA is proposed in Section 5. Finally, Section 6 concludes this work.

2. Related work

In the receiver chain, the RF signal received is often very small and surrounded by interferers so the Signal to Noise Ratio is easily degraded impacting negatively in the receiver performance. Hence, the first block of an RF receiver should amplify the received weak signal with minimal noise added to the system in order to increase the sensitivity of the receiver. Therefore, the Low noise amplifier (LNA) is a part of the most important building blocks for displaying receiver chain. In the literature, a lot of effort has been focused on low power consumption LNAs design. Some researches combine the LNA and the mixer, supplied by the same DC current, to save power consumption [3], [4].
LNAs are key components in the front-end receiver system, which amplify the received Radio Frequency (RF) signal from antenna. LNAs are used in diverse applications, such as, Global Positioning System (GPS) receivers, wireless data systems, satellite communication, cellular handsets and radio systems. In [5], a significant tradeoff between gain, noise figure (NF), stability, linearity, input impedance matching and power consumption has presented. In the receive chain, the noise is reduced by the gain of the LNA. Therefore, the function is primarily to boost the signal power while adding minimum noise and distortion to the signal [6]. LNAs can adopt various design topologies and structures, but the input and output impedance must be matched [7].
In [8], the authors have proposed an adaptive LNA for intelligent IoT sensor node applications. The proposed LNA is based on reconfigurability methods that use power supply, bias current, bias voltage and passive bank adjustments. Authors in [9] introduced the nonlinear prediction model using successive learning process based on MARS algorithm and Monte-Carlo samples.
In this paper, to achieve the low power consumption it uses a CS-LNA architecture which consists on connecting MOSFETs M1 and M2 by a Linear Resistor then a Non-Linear Resistor, to reduce the voltage of M1 and M2, with an input and output impedance matching of 50 Ω. In this study, we aim to optimize our LNA design in two directions. One is for low NF and low power, and the other is for high gain.

3. The proposed LNA

In this paper, the CS-LNA in 0.18µm technology is presented as shown in Fig.3. MOSFETs M1 and M2 represent the core of the proposed LNA [10]. Capacitance C1 is connected to terminals of M1 in edict to reduce value of input matching inductor. The highest value of transconductance (gm) is divided by a drain current (id) in the MOSFETs M2 [11]. In the architecture, the basic topology of NMOS transistors is used. The proposed LNA provides an input matching and output matching to be matched with 50 Ω impedance. This LNA uses a resistive load. The optimum value of the quality factor Q, of the LNA is defined by:

$$Q(w_0) = \frac{w_0 W(w_0)}{P(w_0)} \tag{1}$$

Where, w_0 is the resonance pulse, $W(w_0)$ is the electromagnetic energy and $P(w_0)$ is the dissipated power.
The theoretical value of Q would be 4. To keep the value of Q, and additional capacitor is used. Therefore, the capacitor C1 is part of input matching. The input impedance of the proposed LNA is given by:

$$Z_{in} = \frac{V_{in}}{i_{in}} = \frac{(R_3 i_g + v_c + jwL_3 I_3)}{i_{in}}; V_c = \frac{i_g}{jwc_t}, i_3 = i_g + g_m v_c \text{and} c_t = (c_1 + c_{gs}) \tag{2}$$

$$\Rightarrow Z_{in} = R_3 + \frac{1}{jwc_t} + jwL_3 + \frac{g_m L_3}{c_t} \Rightarrow Z_{in} = R_3 + \frac{1}{jw(c_{gs}+c_1)} + jwL_3 + \frac{g_m L_3}{(c_{gs}+c_1)}$$

Where, Cgs is a gate-source capacitor of the MOSFET M2.
If the input impedance Zin of the LNA is not matched to the antenna, or antenna filter, the signal may bounce back to the antenna to be reradiated. Impedance matching is characterized by the S-parameter $S11$ expressed in Equation (3).

$$S11 = \frac{Zin - Z0}{Zin + Z0} \tag{3}$$

Where $Z0$ is the impedance of the source delivering the signal, typically 50 Ω. The $S11$ parameter is directly related to the input signal power and the power
absorbed by the LNA as detailed in Equation (4).

$$1\text{-}S11^2 = \frac{\text{Input power of the LNA}}{\text{Available power from the source}} \quad (4)$$

A $S11$ < -10 dB corresponds to a signal absorption of more than 90 %.
As shown in Fig.2, the proposed CS-LNA is based on Linear Resistors. The adopted topology is called Linear Resistors Common Source LNA (LRCS-LNA).

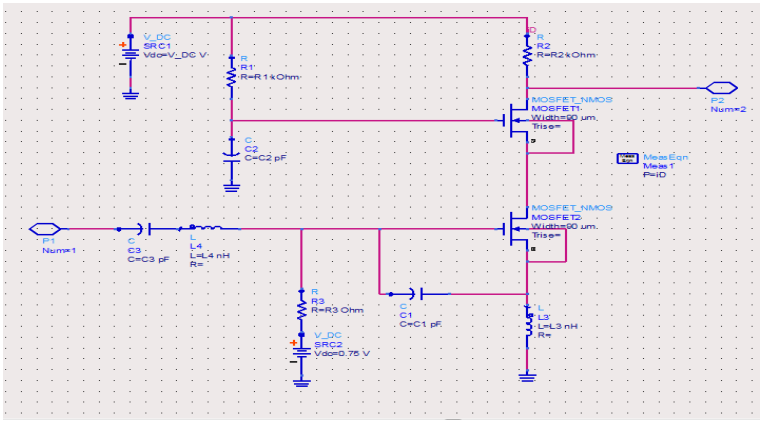

Fig. 3: The LRCS-LNA architecture.

4. Results and discussion

The proposed circuit is simulated with ADS simulation tools in 0.18-µm CMOS. The circuit is designed for 2.4- GHz ISM frequency band using the 2.4-2.48 GHz bandwidth. The proposed LNA dissipates 7.2-mA from a 1.8-V supply. The S-parameters simulation results are shown in Fig.3. The input return loss (S11) is -20 dB and output return loss (S22) is -5 dB at 2.4 GHz. Using the proposed LNA an gain (S21) of 10.2 dB is obtained.

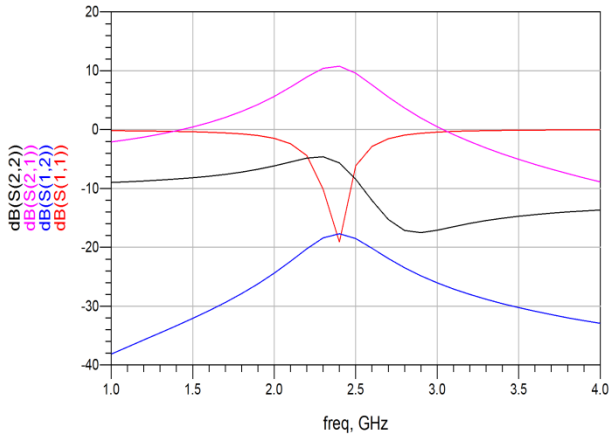

Fig. 4: S-Parameters of the LRCS-LNA.

From Fig.4, it can be seen that the isolation is well acceptable in the entire band. This gain meets the specifications of the Zigbee standard. The matching at the input ensures an NFmin is about 1.4 dB at operating frequency of 2.4 GHz as illustrated in Fig. 5.

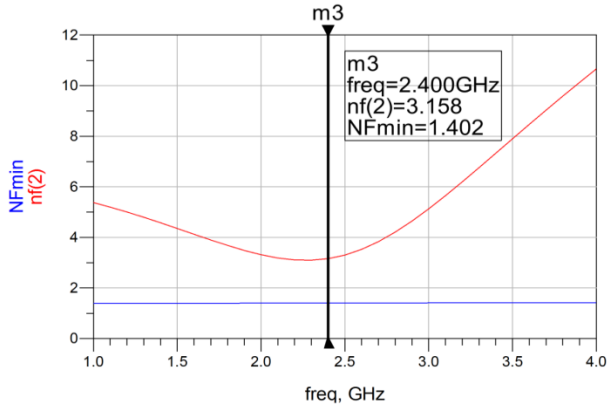

Fig. 5: Noise Figure Simulation Result.

When designing an LNA, we should consider many factors. First of all, the added noise must be minimized, then we should have acceptable gain with input adaptation. The first aspect is very important in order to avoid that part of the incoming signal is reflected back to the antenna and so reducing the signal gain. To address the above-mentioned concerns, the proposed LNA manipulates transistor construction. Therefore, R2 and R4 which are used as the LNA output load are replaced by a MOSFET, who's the grid is connected to the drain, as depicted in Fig. 6. The proposed method is called Non-Linear Resistors CS-LNA (NLRCS-LNA). Replacing R2 and R4 nonlinear improves isolation and increases the gain and as a consequence Noise Figure and linearity get deteriorated.

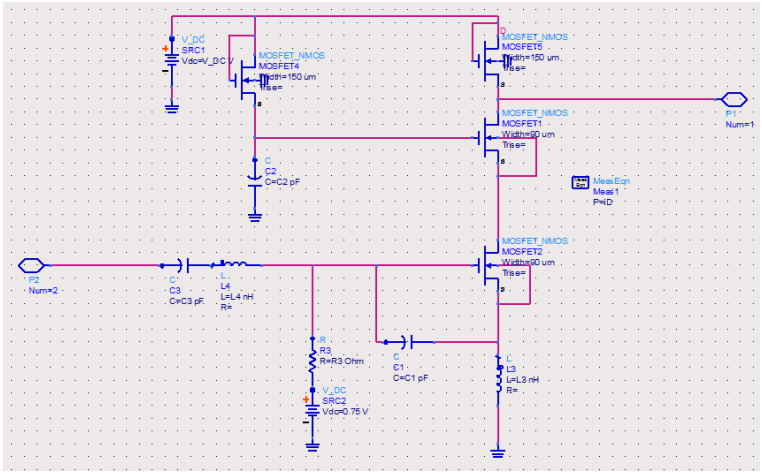

Fig. 6: The NLRCS-LNA Architecture.

5. Performances evaluation of the NLRCS-LNA

In our LNA design, noise and power matching is the most preferred technique to evaluate the radio performance of communication system. The performances of the NLRCS-LNA architecture have been depicted in Fig. 7 and Fig. 8. Fig. 7 depicts a minimum value of S11 of -24dB. From this figure, we can see that the input and output impedance of the proposed LNA are well adopted at 2.4-GHz which is a goal in the study. The good matching ensures a maximum power gain of 8 dB. The modified LNA dissipates 4.8-mA from a 1.8-V supply.

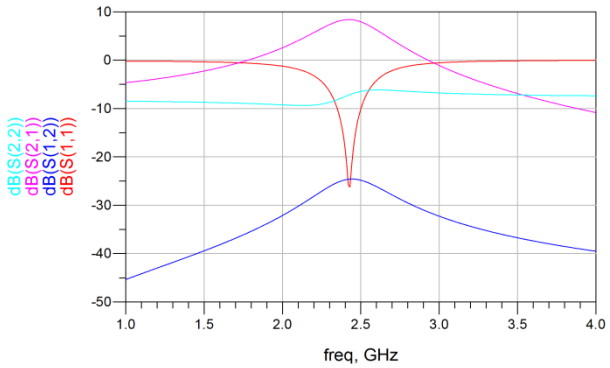

Fig. 7: S-Parameters of the NLRCS-LNA Topology.

Noise figure (NF2) and minimum noise figure (NFmin) have been shown in Fig. 8. This figure shows that at the center frequency NF has the smallest difference from minimum noise figure. Note that NFmin is achieved if the optimum noise matching is satisfied in the input, that is contradictory with power matching and hence scarify the gain.

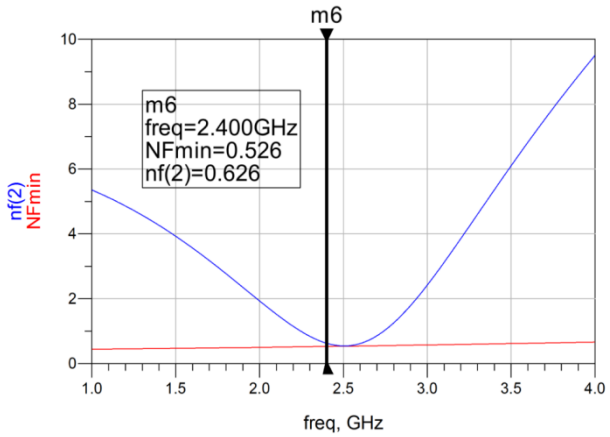

Fig. 8: Noise Figure of the NLRCS-LNA Topology.

In this paper, the common-source LNA (CS-LNA) is presented. Two architectures of the proposed LNA are considered. The first is based on Linear Resistors (LRCS-LNA) whereas the second uses Non-Linear Resistors (NLRCS-LNA). For the both architectures, the CS-LNA achieves high gain, low noise figure and low power consumption which are critical LNA performance parameters. The proposed architectures involve tradeoffs among input matching, power dissipation, gain, and noise. The CS-LNA architecture achieves a lower noise figure and consumes less DC power with good matching at the input. Furthermore, The NLRCS-LNA architecture achieves a good gain. Despite the NLRCS-LNA architecture exhibits superior performance, the LRCS-LNA topology is currently popular in LNA design for the wireless sensor network applications.
The performance of the CS-LNAs are summarized and compared with the state of the art LNAs in Table 1. As can be seen in table 1, the NLRCS-LNA architecture achieves a very low power and a low noise consumption with comparable state of the art LNAs performance.

Table 1: Performances Comparison

	[12]	[13]	[142]	[15]	[16]	[17]	This work LRCS-LNA	NLRCS-LNA
Technology (nm)	130	130	180	130	130	180	180	
Freq (Ghz)	3	5.1	2.4					
Power dissipation [mW]	0.4	1.03	1.13	5.6	17	7.2	7.2	4.8
Gain (dB)	9.1	10.3	21.4	13	10	17	10.2	8
NF (max) (dB)	4.7	5.3	5.2	3.6	3.7	0.01	3.1	0.6
S11 (dB)	-17	-17.7	-19	-14	-25	-15	-20	-24
VDD (V)	0.6	0.4	1.8	1.2	1.2	1.8	1.8	

6. Conclusion

The power, gain and low noise figure are the major constraints in designing a receiver unit for WSN. Therefore, choosing an ultra-power energy-efficient receiver is a challenging process. Since a low-noise amplifier is the first active stage of a CMOS RF receiver, an adaptive Low-Power CMOS LNA seems necessary. The CS-LNA is currently popular because it achieves high gain and low noise figure for the wireless applications. In this paper, a 2.4 GHz common-source LNA was designed in a standard 0.18 µm CMOS technology.
In this paper, the NLRCS-LNA and the LRCS-LNA architectures have been proposed. The NLRCS-LNA architecture can be used effectively using IoT as the protocol delivers a better result for homogeneous networks in comparison to LRCS-LNA architecture. Simulation result shows improved network performance for metrics such as power dissipation, gain and Noise figure.

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