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Research paper

Analysis of a three phase capacitor voltage balanced hybrid multi-level inverter with a three phase RL-load

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Abstract

This paper outlined the basic concepts of two selected types of hybrid multi-level inverters that were capacitor voltage-source dependent. A natural capacitor voltage balancing involving hysteresis with redundant switching states was analyzed in this paper. Simulations using MATLAB 7.14 were carried out for an unbalanced and a well-balanced capacitor voltage supply under 0V, 100V and 200V pre-charged capacitor voltage conditions. A comparative analysis of the two types of hybrid multi-level inverters (Type A and Type B) with pertinent to %THD values of [35.77% and 23.79%] for Type A and [92.10% and 84.94%] for type B during fault occurrence were evaluated in this work. These harmonic values can lead to thermal run away and total malfunction of the semi-conductor switches. An experimental validation of Type A hybrid multi-level inverter with a three level flying capacitor input stage and H-bridge output stage using a three phase RL-Load of 15Ω and 45mH was accomplished in the laboratory with results compared with the simulations for experimental verification.

Keywords: *Capacitor Voltage Balancing; Hybrid Multi-Level Converters; Hysteresis; Redundant Switching States; Simulations; %THD, RL-Load Design and Experimental Set Up.*

1. Introduction

Capacitor voltage balancing is one of the major challenges for modular multilevel converters (MMC's). To generate a precise five voltage levels for a capacitor fed voltage source inverter, it is important to keep the voltage of the D.C capacitors balanced. The flying capacitor voltage can be balanced by appropriate selection of the redundant switching states. To balance the D.C link capacitor voltages, many dc capacitor voltage balancing techniques have been proposed in literature. Reference [1] presented a voltage balancing method for a novel diode clamped modular multilevel converter, but it requires an external energy feedback circuit and high switching frequency which led to lots of losses. A model predictive control strategy was presented in [2] to carry out the capacitor voltage balancing of the modular multilevel converters with reduced switching frequency. Reference [3] introduced a voltage balancing control for modular multilevel converters at fundamental switching frequency where the pulse-widths were the same but the phase angles were different in each fundamental frequency period. In this reference, voltage balancing was realized by shifting the pulses in sequence in each fundamental frequency period. This however needs a several number of periods for capacitor voltage balancing. The technique of zero-sequence voltage injection was used to balance the dc-link capacitor voltages and was reported in [4]. In this reference, the zero sequence voltage did not influence the output line voltage and current but it led to different pulse pattern and different neutral-point current. The main problem with this method was that the calculation and selection of zero sequence voltage was very complex and the switching frequency was not always constant with phase disposition pulse width modulation. A control strategy based on Selective-Harmonic Elimination (SHE) PWM was proposed in [5]. The voltage across the flying capacitor clamped was balanced by swapping the switching patterns. The swapping of the switching patterns depended on the polarity of the output current and the polarity of the flying capacitor voltage. The dc-link capacitor voltage was regulated by adding or subtracting a relatively small pulse to the switching pulse signals. That method was very suitable for high power and low switching frequency applications. However, the voltage regulation ability was not strong due to the low switching frequency and high capacitor voltage ripple. The space vector modulation (SVM) was proposed in [6]. The SVM was used to generate five-level output voltage and to balance the voltages of the dc-link capacitors and flying capacitor (FC). For a five level SVM method, there are 125 space vectors in total for the output voltage synthesis. Each space vector represented one possibility of switch combination, and each space vector has different impact on dc capacitor and FC voltage variation. the field distribution of the stator. As a result, the singly excited induction machine is capable of producing torque at any speed below synchronous speed. For this reason, induction machines are placed in the class of asynchronous machines.

The SVM method was divided into different categories of triangles. Each category has its own principles to choose the vector sequence and compute the vector durations based on the dc capacitor voltage difference. The key problem of this method was the complicated calculation process. Similar to the zero sequence voltage injection method, the SVM balancing technique can only be used in three phase

applications. A dc link capacitor voltage balancing technique based on phase disposition pulse width modulation for single phase application was proposed in [7]. The basic idea is changing the flying capacitor reference voltage to change the dc capacitor voltages. The problem of this method was that the flying capacitor voltage will have double of the line frequency ripple in steady state which will increase the output current THD. In addition, the dynamic response of regulating the dc link capacitor voltages is not always desirable. In [8], a capacitor voltage balancing method for the modular multilevel converter with the switching frequency as grid frequency was proposed. In this reference, the low switching frequency can effectively reduce excess switching loss though the drive pulses have different pulse-widths but the same phase angle in each switching period. Based on the reviewed literature, it was observed that the existing dc balancing techniques were only suitable for three phase applications; while for single phase applications, the existing technologies have many problems such as high flying capacitor voltage ripple, slow dynamic response. This paper, thus applied the concept of hysteresis voltage band for capacitor voltage balance for a single phase and a three phase topology with a phase disposition modulation at a reduced capacitor voltage ripples. The hysteresis voltage band ΔV was usually set to a very small percentage of the actual capacitor voltage V_{F1}. The upper band applied in this work was denoted by $V_{h1} = V_{F1}\left(1 + \frac{\Delta V}{2}\right)$ while the lower band is denoted by $V_{n1} = V_{F1}\left(1 - \frac{\Delta V}{2}\right)$.

2. Capacitor voltage balancing for type a hybrid multi-level inverter

Many hybrid multi-level inverters have been proposed in reputable literatures. A considerable number of hybrid multi-level inverters were derived from the combinations of one or more conventional multi-level inverters [9]-[12]. The two capacitor voltage balanced hybrid multi-level inverters considered in this paper were classified as Type (A) and Type (B). Type (A) consists of Five-Level Inverter formed from three level flying capacitor as an input and H-bridge as an output while Type (B) is a Five-Level actively neutral point clamped inverter with one flying capacitor as an output. Type (A) hybrid multilevel inverter was shown in Figures 1 and 2. An important feature of this inverter topology was the ability to operate with one source of dc voltage supply. A more prominent feature when compared with other topologies was the ability to operate in three-level mode at full power rating when one of the devices in the H-bridge fails. At this condition, the H-bridge was bypassed through a fast bypass switch or by routing the current through the devices in the complementary path. This feature of the inverter improved the reliability of the whole system thus ensuring continuity in operation and fault-tolerant at all conditions. The modulation scheme was simple and did not need a complex modulation control strategy for the capacitor voltage balancing. The control strategy was based on a multicarrier level shifted in-phase disposition pulse width modulation and a hysteresis capacitor voltage band that regulated the level of capacitor voltage deviation. The three-level flying capacitor was set to a reference voltage value of $V_{c1r} = \frac{V_{dc}}{2}$ while the H-bridge capacitor reference voltage was set to $V_{c2r} = \frac{V_{dc}}{4}$. Table 1 shows the sixteen switch states, inverter output voltage levels with the charging and discharging condition of the capacitor for the Type A hybrid inverter. In Table 1, the capacitor voltage balancing was achieved with different redundant switch states. Three redundant switch states (5,9,14) at $\frac{V_{dc}}{4}$ voltage level, three redundant switch states (1,6,10) at $\frac{-V_{dc}}{4}$ voltage level and five redundant switch states (0,4,7,8,11) at zero voltage level were considered. When current flowed from the positive terminal of capacitor C_1 or C_2 to the negative terminal, it charged the capacitor but when it flowed from the negative terminal to the positive terminal it discharged the capacitor as illustrated in Table 1. The algorithm for the capacitor voltage balance was achieved by considering the positive and negative load current directions. Two major steps were chosen for full capacitor voltage balance when $V_0 = \frac{V_{dc}}{4}$.

Step One: For Positive Load Current ($i_a > 0$) and $V_0 = \frac{V_{dc}}{4}$,

i). Switch state 14 was chosen if capacitor C_2 was undercharged by $V_{c2} \leq (V_{c2r} - dV)$ and needed to be charged to its acceptable voltage range of $(V_{c2r} - dV) < V_{c2} < (V_{c2r} + dV)$ where dV was the permissible voltage deviation from the flying capacitor reference voltage.

ii). Else switch state 9 was chosen if capacitor C2 was overcharged by $V_{c2} \geq (V_{c2r} + dV)$ and needed to be discharged to its permissible voltage range and capacitor C1 was undercharged by $V_{c1} \leq (V_{c1r} - dV)$ and needed to be charged to its permissible voltage range of $(V_{c1r} - dV) < V_{c1} < (V_{c1r} + dV)$

iii). Else switch state 5 was chosen if capacitor C2 was overcharged by $V_{c2} \geq (V_{c2r} + dV)$ and needed to be discharged to its permissible voltage range and capacitor C1 was overcharged by $V_{c1} \geq (V_{c2r} + dV)$ and needed to be discharged to its permissible voltage range.

Step Two: For Negative Load Current ($i_a < 0$) and $V_0 = \frac{V_{dc}}{4}$,

i). Switch state 14 was chosen if capacitor C_2 was overcharged by $V_{c2} \geq (V_{c2r} + dV)$ and needed to be discharged to its permissible voltage range.

ii). Else switch state 9 was chosen if capacitor C_2 was undercharged by $V_{c2} \leq (V_{c2r} - dV)$ and needed to be charged to its permissible voltage range of $(V_{c2r} - dV) < V_{c2} < (V_{c2r} + dV)$ and capacitor C_1 was overcharged by $V_{c1} \geq (V_{c1r} + dV)$ and needed to be discharged to its permissible voltage range.

iii). Else switch state 5 is chosen if capacitor C_2 is undercharged by $V_{c2} \leq (V_{c2r} - dV)$ and needs to be charged to its permissible voltage range of $(V_{c2r} - dV) < V_{c2} < (V_{c2r} + dV)$ and capacitor C_1 is undercharged by $V_{c1} \leq (V_{c1r} - dV)$ and needs to be charged to its permissible voltage range.

The same control procedure for positive and negative load current direction for $V_0 = \frac{V_{dc}}{4}$, was applied when $V_0 = 0$, and $V_0 = -\frac{V_{dc}}{4}$ for efficient capacitor voltage balance control algorithm.

In Figure 1, when a fault occurred at the H-bridge, the five level inverter operated normally by producing a full three level voltage at maximum power. This action was usually achieved by bypassing the H-bridge to ensure continuity as shown in Figure 2. This unique characteristic differentiates it from other topologies.

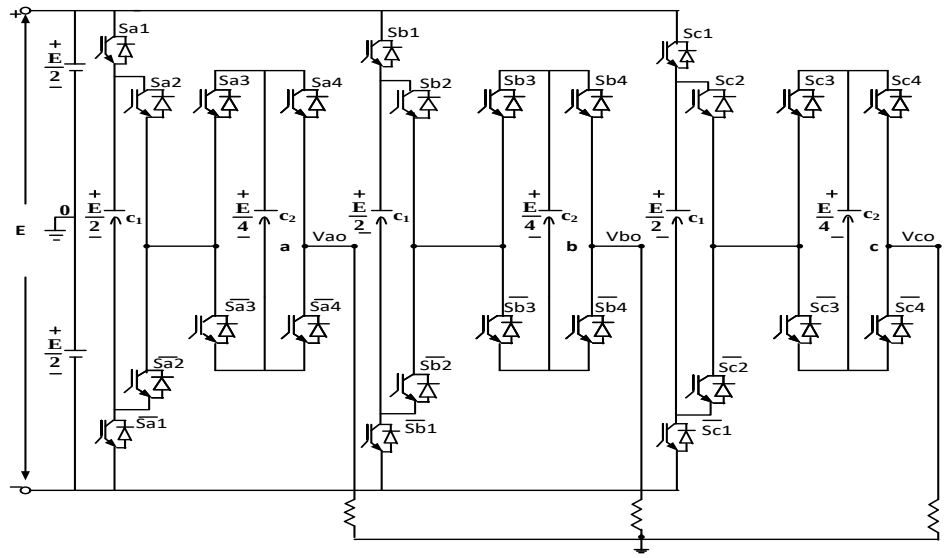


Fig. 1: Diagram of Type A Hybrid Five-Level Inverter with An Un-Bypassed H-Bridge.

Table 1: Switching Sequence and Output Voltages of the Hybrid Five-Level Inverter.

Switching State No.	s_{a1}	s_{a2}	s_{a3}	s_{a4}	$\overline{S_{a1}}$	$\overline{S_{a2}}$	$\overline{S_{a3}}$	$\overline{S_{a4}}$	V_{an}	C_1 ia>0	C_1 ia<0	C_2 ia>0	C_2 ia<0
0	0	0	0	0	1	1	1	1	-Vdc/2	*	*	*	*
1	0	0	0	1	1	1	1	0	-Vdc/4	*	*	-	+
2	0	0	1	0	1	1	0	1	-3Vdc/4	*	*	+	-
3	0	0	1	1	1	1	0	0	-Vdc/2	*	*	*	*
4	0	1	0	0	1	0	1	1	0	-	+	*	*
5	0	1	0	1	1	0	1	0	Vdc/4	-	+	-	+
6	0	1	1	0	1	0	0	1	-Vdc/4	-	+	+	-
7	0	1	1	1	1	0	0	0	0	-	+	*	*
8	1	0	0	0	0	1	1	1	0	+	-	*	*
9	1	0	0	1	0	1	1	0	Vdc/4	+	-	-	+
10	1	0	1	0	0	1	0	1	-Vdc/4	+	-	+	-
11	1	0	1	1	0	1	0	0	0	+	-	*	*
12	1	1	0	0	0	0	1	1	Vdc/2	*	*	*	*
13	1	1	0	1	0	0	1	0	3Vdc/4	*	*	-	+
14	1	1	1	0	0	0	0	1	Vdc/4	*	*	+	-
15	1	1	1	1	0	0	0	0	Vdc/2	*	*	*	*

Notations: * implies no effect on capacitor, + implies capacitor charging, - implies capacitor discharging.

In Table 1, out of the fifteen output voltage states, -3Vdc/4 and 3Vdc/4 were not applied since they do not have redundant switching states to balance the capacitor voltage.

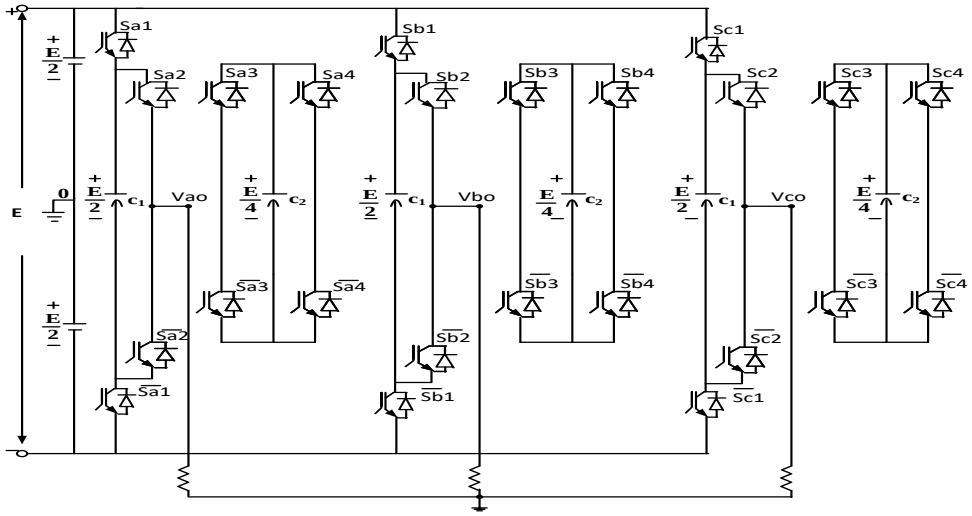


Fig. 2: Diagram of Type A Hybrid Five-Level Inverter with A Bypassed H-Bridge.

For an unbalanced capacitor voltage condition, the five level voltage waveform tends to change in symmetry after a given cycle. Figure 3 shows two capacitors and an inverter output voltages under an unbalanced capacitor voltage control for per cycle switch state sequence ($s_{a1}, s_{a2}, s_{a3}, s_{a4}$) of $1111 \rightarrow 1110 \rightarrow 1000 \rightarrow 0001 \rightarrow 0011$ (switching state number $15 \rightarrow 14 \rightarrow 08 \rightarrow 01 \rightarrow 03$ of Table 1). In Figure 3, it was observed that the capacitor C_2 voltage rised to a higher value than its reference value of $V_{c2r} = \frac{V_{dc}}{4}$. The same goes for C_1 with a

reference value of $V_{c1r} = \frac{V_{dc}}{2}$ for $V_{dc} = 200V$. That made the inverter output voltage highly distorted and far from being the desired five level output.

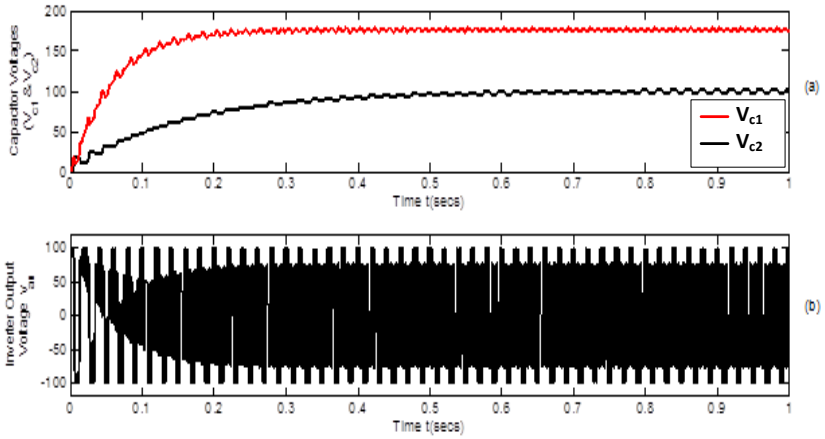


Fig. 3: (A) Capacitor Voltages V_{c1} and V_{c2}. (B) Inverter Output Voltage (V_{an}) for An Unbalanced Condition of Type A Hybrid Five-Level Inverter V_{dc} = 200 V, F_C = 5 kHz, F_s = 50 Hz, M = 0.8.

For a balanced capacitor voltage condition, the five-level voltage waveform tends to trace the shape of the reference voltage and maintain a given symmetry after a given cycle. Figure 4 shows that capacitors C_1 and C_2 voltages (V_{c1} and V_{c2}), in relatively fast response time becomes balanced and essentially equal to their respective reference voltages of $V_{c1} \approx V_{c1r} = \frac{V_{dc}}{2} = 100$ V and $V_{c2} \approx V_{c2r} = \frac{V_{dc}}{4} = 50$ V for $V_{dc} = 200$ Volts. If V_{dc} is extended to 400Volts with a zero precharged voltage or with precharged voltages of 100 V and 200 V, the waveforms in Figures 5 and 6 were realized and capacitors C_1 and C_2 voltages (V_{c1} and V_{c2}) were balanced and also equal to their respective reference voltages of $V_{c1} \approx V_{c1r} = \frac{V_{dc}}{2} = 200$ V and $V_{c2} \approx V_{c2r} = \frac{V_{dc}}{4} = 100$ V. For $V_{dc} = 400$ Volts.

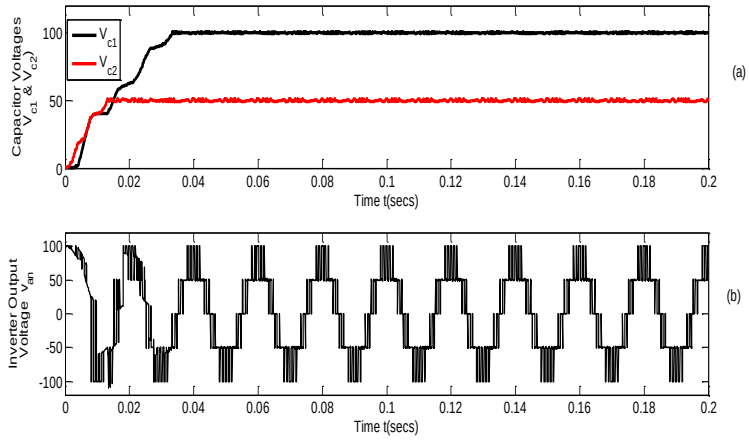


Fig. 4: (A) Capacitor Voltages V_{c1} and V_{c2}. (B) Inverter Output Voltage (V_{an}) for a balanced Condition of Type A hybrid five-level inverter, F_C = 5 kHz, F_s = 50 Hz, M = 0.8.

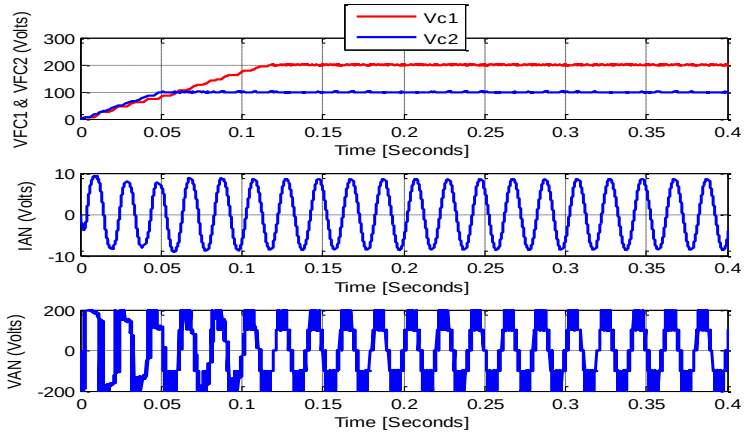


Fig. 5: (A) Capacitor voltages V_{c1} and V_{c2}. (B) Inverter output current (I_{an}); (C) Inverter output Voltage (V_{an}) under a balanced capacitor voltage control for Type A hybrid five-level inverter V_{dc} = 400 V, F_C = 5 kHz, F_s = 50 Hz, M = 0.8, with zero pre-charged capacitor voltage.

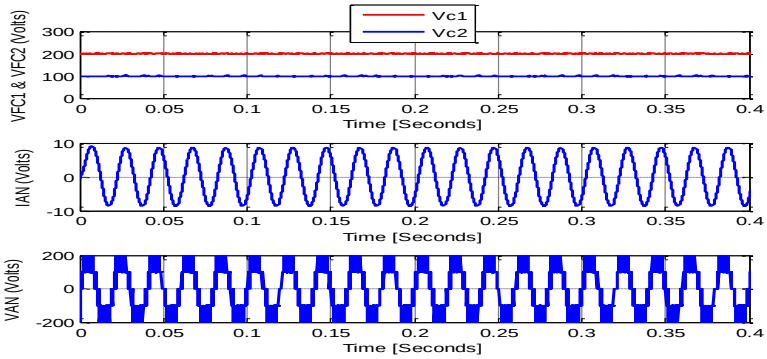


Fig. 6: (A) Capacitor Voltages V_{c1} and V_{c2}. (B) Inverter Output Current (I_{an}). (C) Inverter Output Voltage (V_{an}) Under A Balanced Capacitor Voltage Control For Type A Hybrid Five-Level Inverter V_{dc} = 400 V, F_C = 5 kHz, F_s = 50 Hz, M = 0.8, with 100 V And 200 V Pre-Charged Capacitor Voltage.

The per phase voltage for the three phase voltages and the line to line voltages with their spectral display for a balanced hybrid five level inverter topology of Figure 1 were presented in Figures 7 to 12.

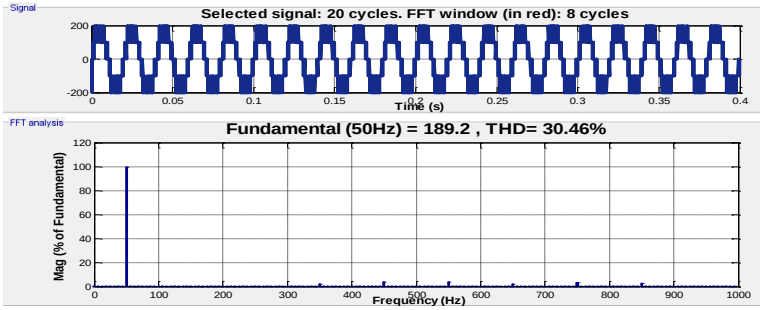


Fig. 7: Phase A Output Voltage (V_{an}) with A Balanced Capacitor Voltage for Type A Hybrid Multi-Level Inverter of Figure 1. V_{dc} = 400 V, F_C = 5 kHz, F_s = 50 Hz, M = 0.8, Z_L = (8+6j) Ω.

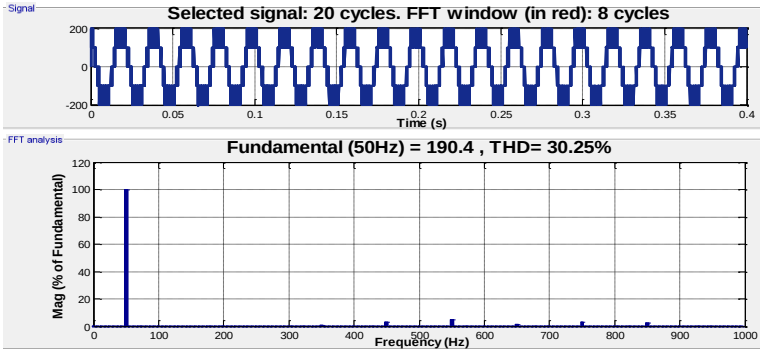


Fig. 8: Phase B Output Voltage (V_{bn}) with A Balanced Capacitor Voltage for Type A Hybrid Multi-Level Inverter of Figure 1. V_{dc} = 400 V F_C = 5 kHz, F_s = 50 Hz, M = 0.8, Z_L = (8+6j) Ω.

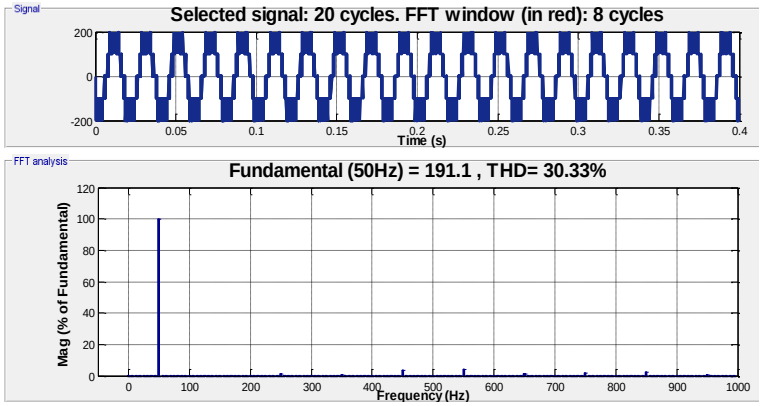


Fig. 9: Phase C Output Voltage (V_{cn}) with a balanced capacitor voltage for Type A hybrid multi-level inverter of Figure 1. V_{dc} = 400 V, F_C = 5 kHz, Fs = 50 Hz, M = 0.8, Z_L = (8+6j) Ω

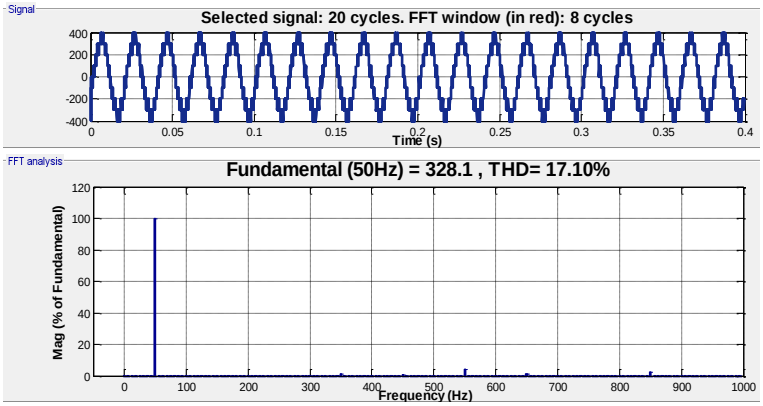


Fig. 10: Lines AB output Voltage (V_{AB}) with a balanced capacitor voltage for Type A hybrid multi-level inverter of Figure 1. V_{dc} = 400 V, F_C = 5 kHz, Fs = 50 Hz, M = 0.8, Z_L = (8+6j) Ω

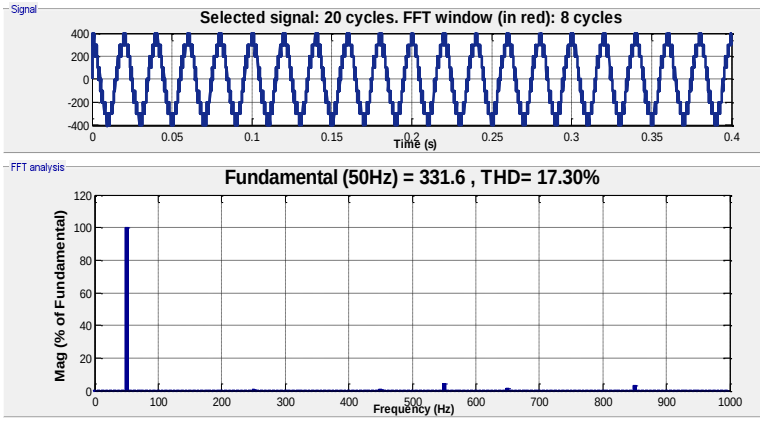


Fig. 11: Lines BC output Voltage (V_{BC}) with a balanced capacitor voltage for Type A hybrid multi-level inverter of Figure 1. V_{dc} = 400 V, F_C = 5 kHz, F_s = 50 Hz, M = 0.8, Z_L = (8+6j) Ω

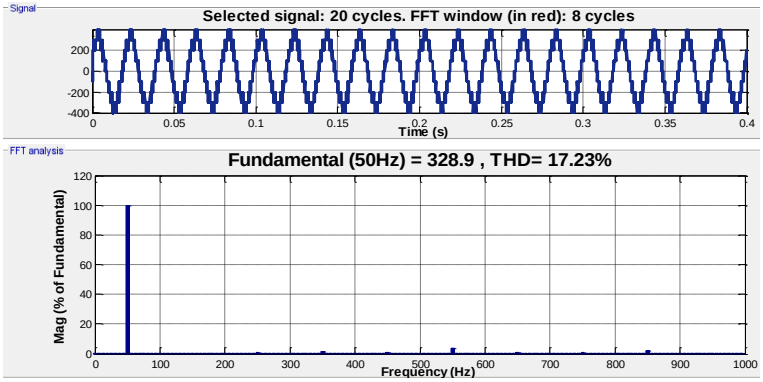
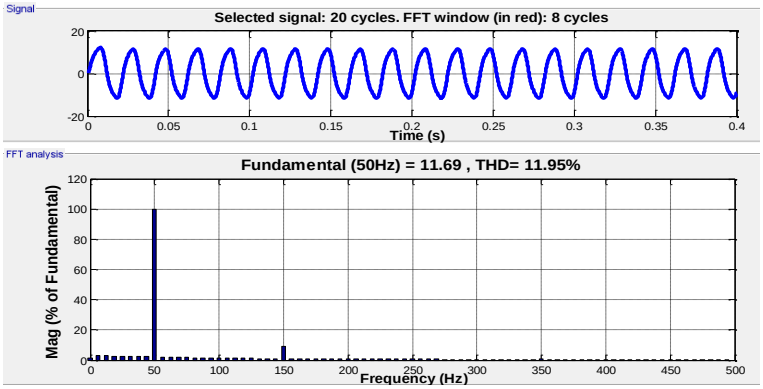


Fig. 12: Lines CA output Voltage (V_{CA}) with a balanced capacitor voltage for Type A hybrid multi-level inverter of Figure 1. V_{dc} = 400 V, F_C = 5 kHz, F_s = 50 Hz, M = 0.8, Z_L = (8+6j) Ω

When a fault occurs at the H-bridge as earlier presented in Figure 2, the H-bridge is bypassed and the inverter operates in three-level mode producing the same full voltage magnitude and full power output which was equivalent to the ratings of the five-level operation. The results shown in Figures 13-15 confirm this concept.



Fig, 13: Three Level Phase Current (Ian) With A Bypassed H-Bridge And Full Power.

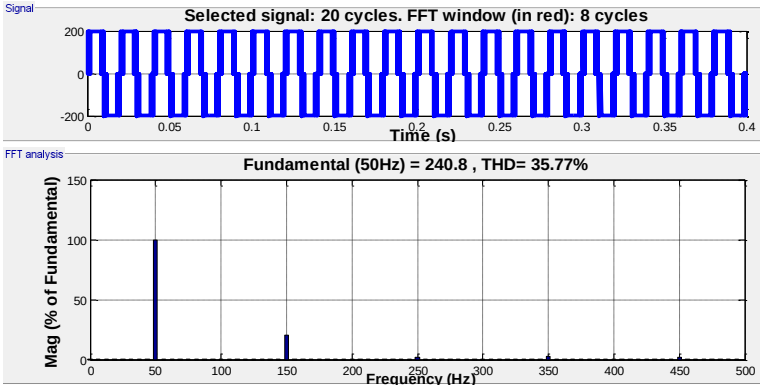


Fig. 14: Three Level Phase Voltage (Van) With A Bypassed H-Bridge And Full Power.

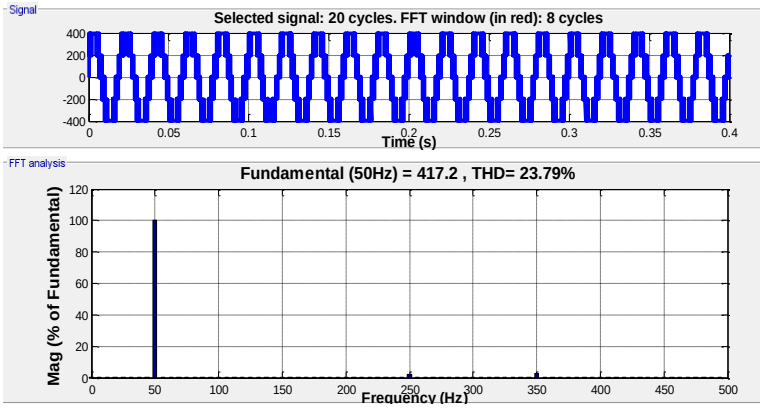


Fig. 15: Three Level Line-Line Voltage (V_{AB}) With A Bypassed H-Bridge And Full Power.

3. Capacitor voltage balancing for type b hybrid multi-level inverter

Type (B) hybrid multilevel inverter was shown in Figures 16 and 17. The circuit diagram presented in Figure 16 depicts the single phase five-level active neutral point clamped (5L-ANPC) hybrid inverter topology. This converter was an arrangement of two level inverters connected in parallel with the d.c-link capacitors. The first sub-circuit was made up of bidirectional switches S_5, S_6, S_9, S_{10}, with a capacitor C_2. The second sub-circuit was made up of bidirectional switches S_7, S_8, S_{11}, S_{12}, with a capacitor C_3 while the third sub-circuit was made up of bidirectional switches S_1, S_2, S_3, S_4, with a capacitor C_1 which was used to connect the converter to the output phase. It was worth mentioning that the switches S_5, S_7 and S_6, S_8 were operated in phase. S_5 and S_7 were complementary to S_6 and S_8. A similar sequence was applied to S_9, S_{10}, S_{11} and S_{12}.The three floating capacitors shown in Figure 16 add more cost to the overall system and require more space for accommodating the entire volume of the inverter structure. For this reason, it was expedient to reduce the number of floating capacitors in terms of component count. This was achieved by removing C_2 and C_3 from Figure 16 to form a more reduced circuit as shown in Figure 17 which was a simplified diagram for three phase 5Level-ANPC. The possible switching states for the discussed 5Level-ANPC was presented in Table 2 with capacitors C_1, C_2 and C_3 charged to a voltage level of $\frac{V_{dc}}{2}$.

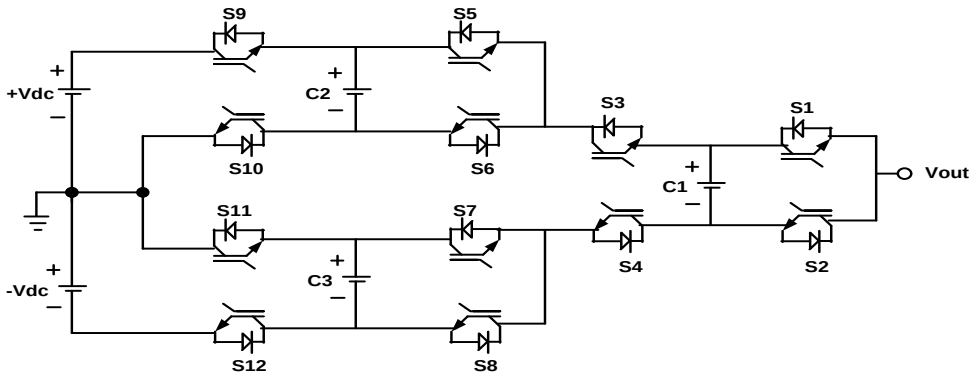


Fig. 16: Circuit Diagram of Five-Level ANPC.

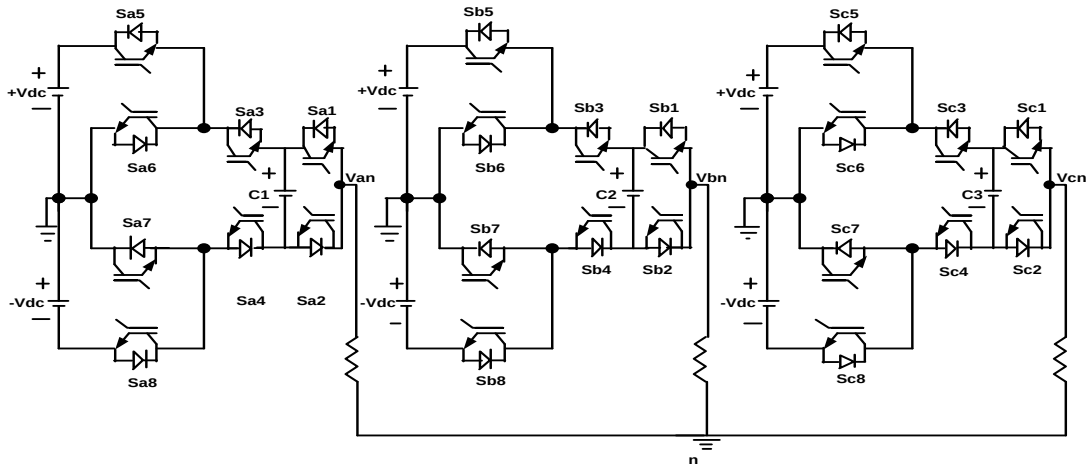


Fig. 17: Modified Circuit Diagram of Five-Level ANPC.

The five-level ANPC inverter has one capacitor. A capacitor voltage band of Vh_1 = 101.5 V and Vn_1 = 99.5 V was set up to track the expected output voltage. This reduced the control complexity in the capacitor voltage balance [13]- [14]. The output voltage can easily be synthesized with the sequence reported in [15]- [20].

The following steps were considered for the switching combinations for the Type (B) hybrid multi-level inverter under a balanced capacitor voltage technique.

Step 1: For $V_{AO} = +\frac{V_{dc}}{2}$. Switches $S_{a5,}S_{a3,}$ and S_{a1} were turned on. The output current i_a under positive and negative mode has no effect on C_1.

Step 2: For the Positive Load Current $i_a > 0$ and $V_0 = \frac{V_{dc}}{4}$,

i). If switches S_{a5}, S_{a3} and S_{a2} were turned on, capacitor C_1 was undercharged by $V_{c1} \leq (V_{c1r} - dV)$ and will be charged to its allowable voltage range of $(V_{c1r} - dV) < V_{c1} < (V_{c1r} + dV)$. Where dV was the maximum allowable voltage deviation from the flying capacitor reference voltage.

ii). Else, switches S_{a7}, S_{a4} and S_{a1} were turned on with capacitor C_1 overcharged by $V_{c1} \geq (V_{c1r} + dV)$ and will be discharged to its allowable voltage range of $V_{c1} \leq (V_{c1r} + dV)$. Where dV was the permissible voltage deviation from the flying capacitor reference voltage.

Step 3: For Negative Load Current $i_a < 0$ and $V_0 = \frac{V_{dc}}{4}$,

i). If switches S_{a5}, S_{a3} and S_{a2} were turned on, capacitor C_1 was overcharged by $V_{c1} \geq (V_{c1r} + dV)$ and will be charged to its allowable voltage range of $V_{c1} \leq (V_{c1r} + dV)$.

ii). Else, S_{a7}, S_{a4} and S_{a1} were turned on with capacitor C_1 undercharged by $V_{c1} \leq (V_{c1r} - dV)$ and will be charged to its allowable voltage range of $(V_{c1r} - dV) < V_{c1} < (V_{c1r} + dV)$.

Step 4: For the Positive Load Current $i_a > 0$ and $V_0 = 0$,

When switches S_{a6}, S_{a3} and S_{a1} or S_{a7}, S_{a4} and S_{a2} were on, capacitor C_1 was unaffected by i_a.

Step 5: For the Negative Load Current $i_a < 0$ and $V_0 = 0$,

When switches S_{a6}, S_{a3} and S_{a1} or S_{a7}, S_{a4} and S_{a2} were on, capacitor C_1 was unaffected by i_a.

Step 6: For the Positive Load Current $i_a > 0$ and $V_0 = -\frac{V_{dc}}{4}$,

i). If switches S_{a6}, S_{a3} and S_{a2} were turned on, capacitor C_1 was undercharged by $V_{c1} \leq (V_{c1r} - dV)$ and will be charged to its allowable voltage range of $(V_{c1r} - dV) < V_{c1} < (V_{c1r} + dV)$.

ii). Else, switches S_{a8}, S_{a4} and S_{a1} were turned on with capacitor C_1 overcharged by $V_{c1} \geq (V_{c1r} + dV)$ and will be discharged to its allowable voltage range of $V_{c1} \leq (V_{c1r} + dV)$.

Step 7: For Negative Load Current $i_a < 0$ and $V_0 = -\frac{V_{dc}}{4}$,

i). If switches S_{a6}, S_{a3} and S_{a2} were turned on, capacitor C_1 was overcharged by $V_{c1} \geq (V_{c1r} + dV)$ and will be discharged to its allowable voltage range of $V_{c1} \leq (V_{c1r} + dV)$.

ii). Else, S_{a8}, S_{a4} and S_{a1} were turned on with capacitor C_1 undercharged by $V_{c1} \leq (V_{c1r} - dV)$ and will be charged to its allowable voltage range of $(V_{c1r} - dV) < V_{c1} < (V_{c1r} + dV)$.

Step 8: For $V_{AO} = \frac{-V_{dc}}{2}$, $S_{a8,}$ $S_{a4,}$ and S_{a2} were turned on. The current output i_a has no effect on the capacitor (C_1). The pairs of redundant switching states were used to balance the capacitor voltage. Thus proper selection of the redundant switching states balances the flying capacitor (FC) voltage. This implied that the 5L-ANPC combined the robustness of the NPC with the flexibility of the flying capacitor.

Table 2: Switching Sequence of Figure 4.17 for 5Level-ANPC

Switching State No.	s_{a8}	s_{a7}	s_{a6}	s_{a5}	s_{a4}	s_{a3}	s_{a2}	s_{a1}	V_{an}	C_1 ia > 0	C_1 ia < 0
1	0	0	0	1	0	1	0	1	$\frac{+V_{dc}}{2}$	*	*
2	0	0	0	1	0	1	1	0	$\frac{+V_{dc}}{4}$	+	-
3	0	1	0	0	1	0	0	1	$\frac{+V_{dc}}{4}$	-	+
4	0	0	1	0	0	1	0	1	0	*	*
5	0	1	0	0	1	0	1	0	0	*	*
6	0	0	1	0	0	1	1	0	$\frac{-V_{dc}}{4}$	+	-
7	1	0	0	0	1	0	0	1	$\frac{-V_{dc}}{4}$	-	+
8	1	0	0	0	1	0	1	0	$\frac{-V_{dc}}{2}$	*	*

For the Five-Level ANPC, it was observed that two redundant switch states (2 and 3) exist for $V_0 = +\frac{V_{dc}}{4}$. The same applies to $V_0 = -\frac{V_{dc}}{4}$ with two redundant switch states (6 and 7). These two combinations provided self-controlled capacitor voltage balancing. The self-balancing implied that the natural balancing control algorithm was not applied. This can be achieved if either the per cycle switch state sequence of $1 \rightarrow 2 \rightarrow 4$ or $5 \rightarrow 6 \rightarrow 8$ and $1 \rightarrow 3 \rightarrow 4$ or $5 \rightarrow 7 \rightarrow 8$ in Table 2 were applied on the inverter switches. For self-balancing (with no balancing control) operation, the circuit dynamic response becomes relatively slow because of the relatively large value of capacitor C_1 of 7500µF needed to maintain the steady state capacitor voltage ripple to an appreciable low level. The waveforms for the capacitor voltage (V_{cf}) and the inverter output voltage (V_{an}) under self-capacitor voltage balancing operation without a balancing control algorithm was shown in Figures 18-19.

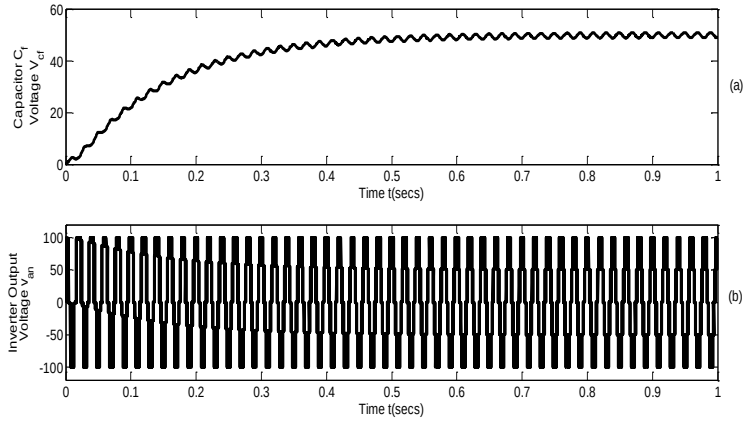


Fig. 18: (A) Capacitor voltage V_{cf} (B) Output load voltage V_{an} under self-capacitor voltage balance for the Type B hybrid multi-level inverter of Figure 17 with per cycle switch state sequence of $1 \rightarrow 2 \rightarrow 4 || 5 \rightarrow 6 \rightarrow 8$ & C_f = 7500 µF, V_{dc} = 200 V, F_C =1.05 kHz, F = 50 Hz, M = 0.8, Z_L = (5+20j) Ω.

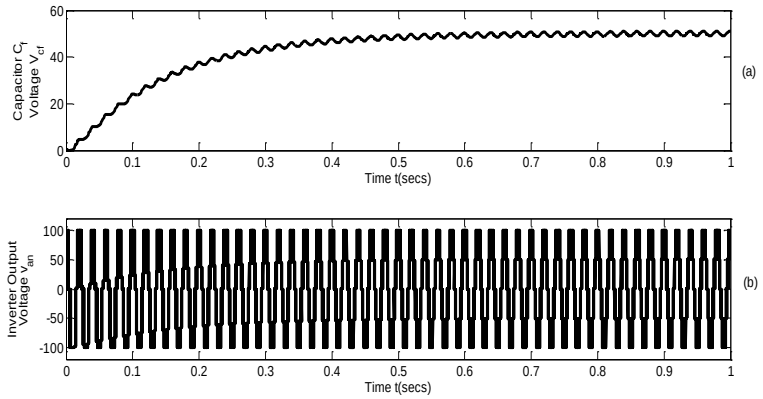


Fig. 19: (A) Capacitor voltage V_{cf} (B) Output load voltage V_{an} under self-capacitor voltage balance for the Type B hybrid multi-level inverter of Figure 17 with per cycle switch state sequence of $1 \rightarrow 3 \rightarrow 4 || 5 \rightarrow 7 \rightarrow 8$ & C_f = 7500 µF, V_{dc} = 200 V, F_C =1.05 kHz, F = 50 Hz, M = 0.8, Z_L = (5+20j) Ω.

When capacitor voltage balancing control as earlier discussed was applied to the Five-level ANPC circuit diagram of Figure 17, the capacitor voltage becomes balanced. The circuit dynamic response becomes relatively fast in response time due to the relatively small value of capacitor C_1 of 1500µF needed to maintain the steady state capacitor voltage ripple to an appreciable low level. The capacitor voltage was then made equal to its reference voltage value of $V_{cf} \approx V_{cfr} = \frac{V_{dc}}{4} = 50$ V for $V_{dc} = 200$ V as shown in Figure 20 for V_{cf} and V_{an}.

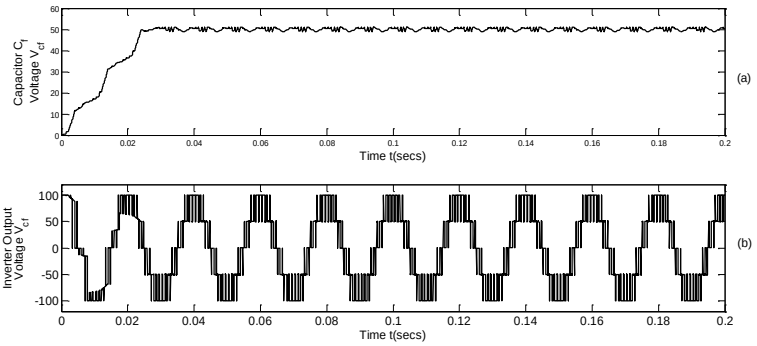


Fig. 20: (A) Capacitor Voltage V_{Cf} (B) Output Load Voltage V_{an} Under Natural Capacitor Voltage Balance for the Type B Hybrid Multi-Level Inverter of Figure 17 with Per Cycle Switch State Sequence Of $1 \rightarrow 2 \rightarrow 3 \rightarrow 4 \rightarrow 5 \rightarrow 6 \rightarrow 7 \rightarrow 8$ And C_f = 1500 µf, V_{dc} = 200 V, F_C =1.05 Khz, F = 50Hz, M = 0.8, Z_L = (8+6j) Ω.

Similarly, when a pre-charged capacitor voltage values of 0 V and 100 V with a V_{dc} of 400 V were applied for a natural capacitor voltage balance control the results presented in Figures 19 - 22 were realized.

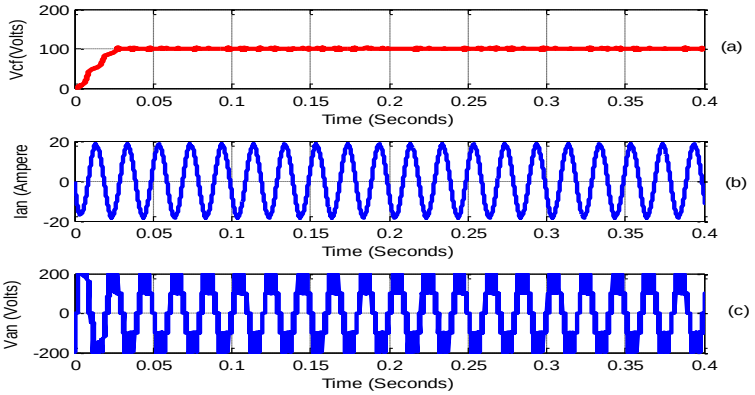


Fig. 21: (A) Capacitor voltage V_{cf} (B) Output Phase Current I_{an} (C) Output Phase Voltage V_{an} under natural capacitor voltage balancing operation for the five level ANPC inverter of Figure 17 with per cycle switch state sequence of $1 \rightarrow 2 \rightarrow 3 \rightarrow 4 \rightarrow 5 \rightarrow 6 \rightarrow 7 \rightarrow 8$ and C_f = 1500µF, V_{dc} = 400 V, F_C = 5 kHz, F = 50 Hz, M = 0.8, Z_L = (8+6j) Ω with zero pre-charged capacitor voltage.

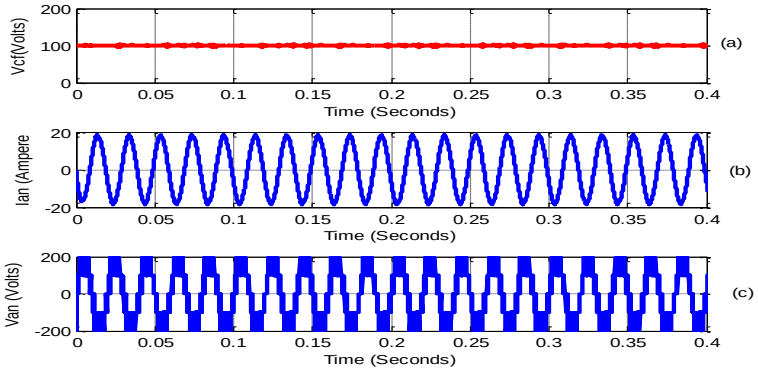


Fig. 22: (A) Capacitor voltage V_{cf} (C) Output Phase Current I_{an} (C) Output Phase Voltage V_{an} under natural capacitor voltage balancing operation for the Type B hybrid multi-level inverter of Figure 17 with per cycle switch state sequence of $1 \rightarrow 2 \rightarrow 3 \rightarrow 4 \rightarrow 5 \rightarrow 6 \rightarrow 7 \rightarrow 8$ and C_f = 1500 µF, V_{dc} = 400 V, F_C = 5 kHz, F = 50 Hz, M = 0.8, Z_L = (8+6j) Ω with 100 V pre-charged capacitor voltage.

The phase and line to line voltages with spectral display for a balanced hybrid actively neutral point clamped five level inverter of Figure 17 are shown in Figures 23 and 24.

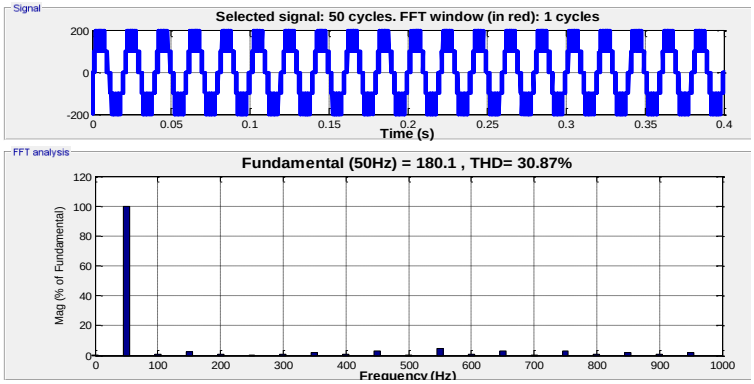


Fig. 23: Phase Voltage V_{an} of five-level ANPC inverter of Figure 17 under natural capacitor voltage balancing operation. V_{dc} = 400V, F_C = 5 kHz, F = 50 Hz, M = 0.8, Z_L = (8+6j) Ω.

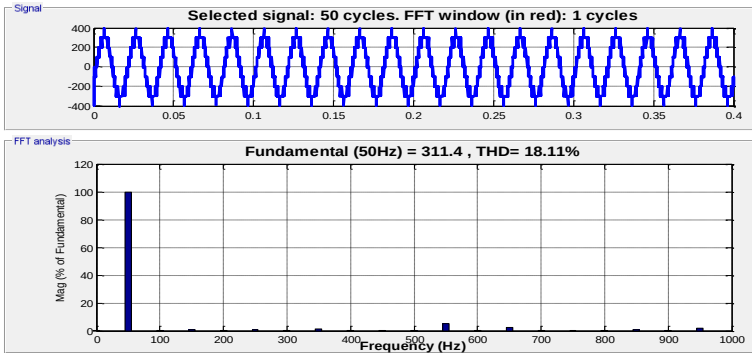


Fig. 24: Lines AB Voltage V_{AB} of five-level ANPC inverter of Figure 17 under natural capacitor voltage balancing operation. V_{dc} = 400V, F_C = 5 kHz, F = 50Hz, M = 0.8, Z_L = (8+6j) Ω.

In line with the fault tolerant condition, when the ANPC capacitor was shorted, the inverter produced a highly distorted and unsymmetrical waveforms. Though maximum power was produced which is similar to the type A hybrid topology, that was less efficient due to distortions and high harmonics (%THD of 92.10 and 84.94) as shown in Figures 25-26.

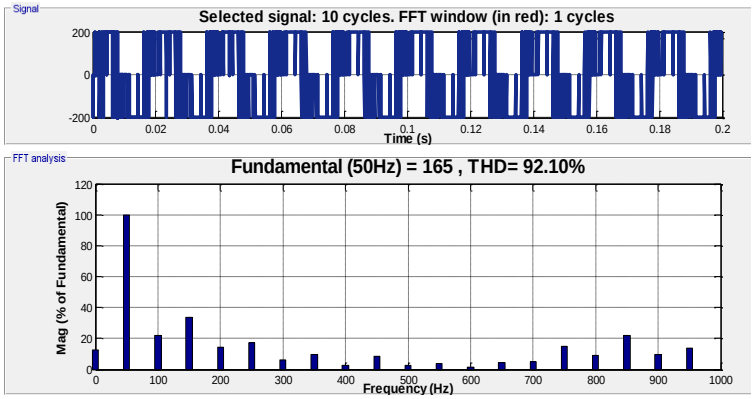


Fig. 25: Phase Voltage V_{an} of five-level ANPC inverter of Figure 17 with A Shorted Capacitor V_{dc} = 400V, F_C = 5 kHz, F = 50Hz, M = 0.8, Z_L = (8+6j) Ω.

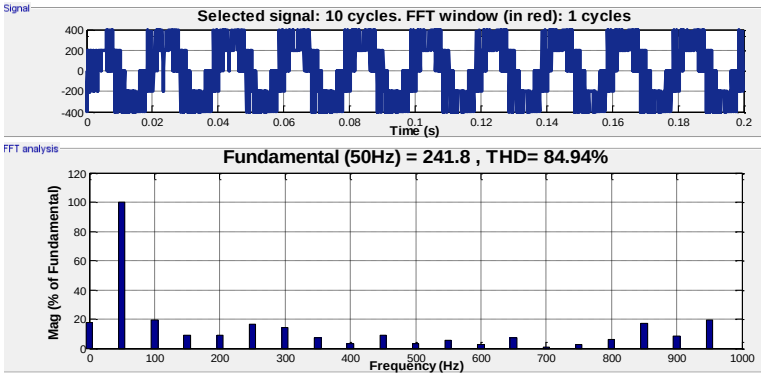


Fig. 26: Lines AB Voltage V_{AB} of five-level ANPC inverter of Figure 17 with A Shorted Capacitor. V_{dc} = 400V, F_C = 5 kHz, F = 50Hz, M = 0.8, Z_L = (8+6j) Ω.

4. Experimental set up for type a hybrid multi-level inverter

The experemental set up was shown in Figure 27. This is made up of four stages. The first stage was the d.c power supply which consists of a coiled 1.5 kVA, 220/200 Volts transformer, nine 100 Amps full bridge diode rectifiers and 2200 µF, 200 Volts capacitor filters. The second stage consists of the firing pulses or gate signal generator using EZDSPTMF28335 digital signal processor (dsp). The pulses generated from the dsp were processed using the dc-dc converter (VAS D1-S12-D12) which amplifies the generated signals that drives the power switches. The third stage was the dead band (1milisecond) or the isolation circuit which was achieved with a variable resistor of 10 kΩ and a capacitor value of 0.1µF. The fourth stage was the RL-load design calculation which involves a 1000 Watts power output, a 45^0 power factor angle and a 200 Vrms. A power triangle was applied to determine the values of R = 15 Ω, L = 45 mH and Z = 20 Ω. The block diagram in Figure 27 depicts the inverter d.c power supply unit.

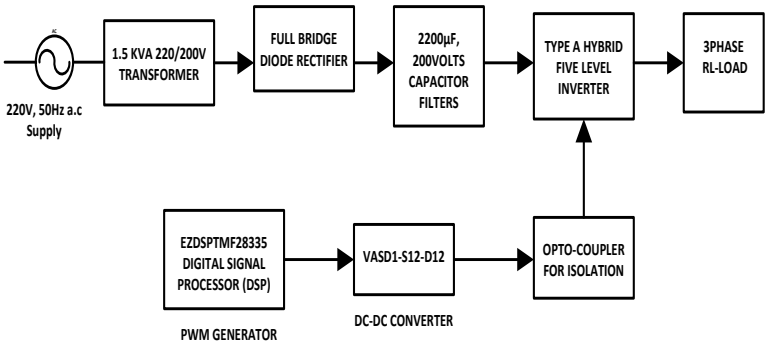


Fig. 27: Block Diagram of the Dc Power Supply Stage.

5. Simulation results and discussion

The capacitor voltages and inverter output voltage for an unbalanced capacitor state of Type A Hybrid multi-level inverter with $V_{dc} = 200V$ was presented in Figure 3. It was observed that the capacitor voltages (V_{c1} and V_{c2}) raised to a higher value than the reference value of $V_{c1r} = \frac{V_{dc}}{2}$ and $V_{c2r} = \frac{V_{dc}}{4}$. This exponential rise in the capacitor voltage made the inverter output highly distorted and above the desired five level inverter output voltage. Figure 4 showed a well-balanced capacitor voltage. It was obvious that the capacitor voltages (V_{c1} and V_{c2})

in Figure 4 were equal to the reference value of $V_{c1r} = \frac{V_{dc}}{2} = 100V$ and $V_{c2r} = \frac{V_{dc}}{4} = 50$ V for $V_{dc} = 200$ V. In Figure 5, when $V_{dc} = 400V$, the capacitor voltages V_{c1} and V_{c2} were balanced at a value of $V_{c1} = 200$ V and $V_{c2} = 100$ V. The transient period of 0 - 0.1second indicated the charging period of the capacitor when the pre-charged capacitor voltage was set at zero as shown in the inverter output current and voltage. Figure 6 represents a balanced capacitor voltage waveform when a pre-charged capacitor voltage values of 100 V and 200 V were impressed on the capacitors. It was observed that the transience was diminished and the inverter output current and voltage maintained a stable state from 0 - 0.4second. In Figures 7-12, the per phase voltage and the line-line voltages were represented with a corresponding %THD for pre-charged voltage values of 100 V and 200 V. A close observation indicated that a stable voltage was maintained all through the simulation period with close %THD values. In Figures 13- 15, it was proven that the H-bridge was bypassed during a fault occurrence on the H-bridge. The inverter operated in three-level mode producing the same full voltage magnitude of 200 V for the phase voltage and 400 V for the line voltage which was equivalent to the voltage ratings of the full five-level inverter in Figures 7 and 10. In Figures 18 and 19, the unbalanced capacitor voltage states for type B Hybrid multi-level inverter with $V_{dc} = 200$ V were presented. It was observed that the dynamic response was relatively slow due to the large value of capacitor (7500µF) needed to maintain the steady state capacitor voltage ripple to an appreciable low level. The capacitor voltage under this condition was not equal to the reference voltage value $V_{cf} \neq V_{cfr} \neq \frac{V_{dc}}{4}$. In Figure 20, the capacitor voltage was balanced for type B Hybrid Multi-Level Inverter. The dynamic response in Figure 20 was relatively fast in response time due to the small value of capacitor (1500µF) needed to maintain the steady state capacitor voltage ripple to a low level. At this condition, $V_{cf} \approx V_{cfr} = \frac{V_{dc}}{4} = 50$ V for $V_{dc} = 200$ V. In Figure 21, the capacitor voltage V_{cf} for $V_{dc} = 400$ V was made to track the reference voltage $V_{cf} \approx V_{cfr} = \frac{V_{dc}}{4} = 100$ V for $V_{dc} = 400$ V. A transient period existed from 0 - 0.025 second due to a zero pre-charged capacitor voltage. In Figure 22, a stable voltage state was obtained when the pre-charged capacitor voltage was set to 100 V. The capacitor voltage $V_{cf} \approx V_{cfr} = \frac{V_{dc}}{4} = 100$ V for $V_{dc} = 400$ V without a transient period. Figures 23 and 24 represented the phase and line-line voltages of a well-balanced capacitor voltage of the five-level ANPC with a pre-charged capacitor voltage value of 100 V devoid of a transient state. Figures 25 and 26 depicted the phase voltage and the line-line voltage when a short-circuit faults occurred on the capacitor output terminal of the five-level ANPC. It was observed in these two Figures that high %THD values of 92.10% and 84.94% were obtained which was far above the %THD values of 35.77% and 23.79% obtained in Figures 14 and 15 for type A five-level inverter under a fault occurrence on the H-bridge.

6. Experimental results and discussion

The stiff dc voltage from the 2200µF, 200 V capacitor was presented in Figure 28. The five-level output phase voltages were presented in Figures 29 and 30 at modulation indices of 1.2 and 0.8 respectively. The five-level line voltages at a modulation index of 0.8 were presented in Figures 31 and 32. The three phase current was presented in Figure 33. As earlier stated in the simulation results of Figures 14 and 15, when an H-bridge was bypassed, a three-level voltage was produced. The waveform generated from the laboratory result when an H-bridge was bypassed was shown in Figure 34 at a modulation index of 1.2. The three-level line voltages were presented in Figures 35 and 36. The current (A) lagging characteristics on voltage (V) at an angle of 45^0 was presented in Figure 37. The waveforms obtained showed that a close similarity exists between the simulation results and the laboratory results as indicated in Figures 14, 15 and 34, 35.

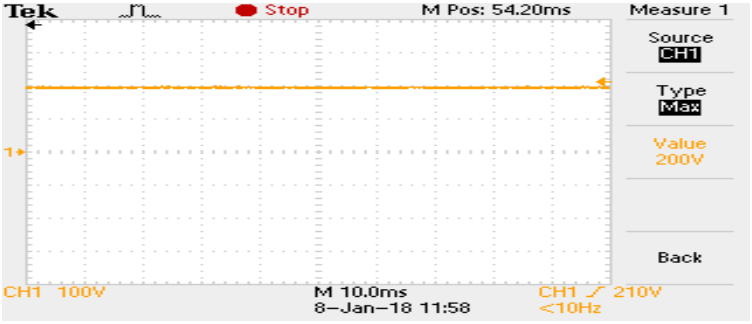


Fig. 28: A 200Volt Dc Stiff Voltage Supply to the Power Circuit.

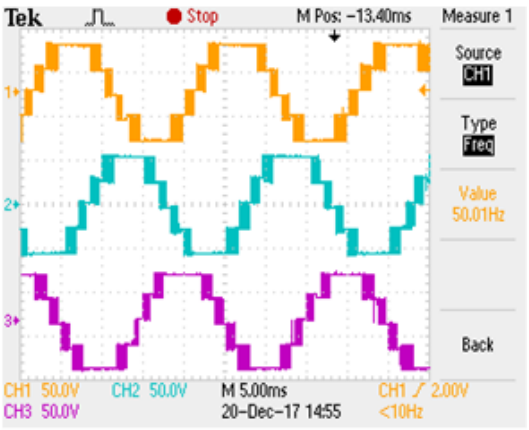


Fig. 29: Five Level Phase Voltage at 1.2 MI.

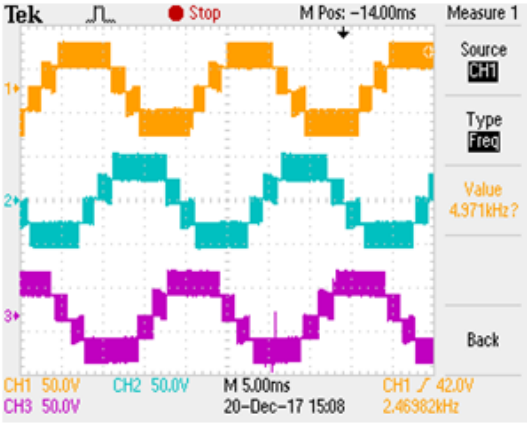


Fig. 30: Five Level Phase Voltage at 0.8 MI.

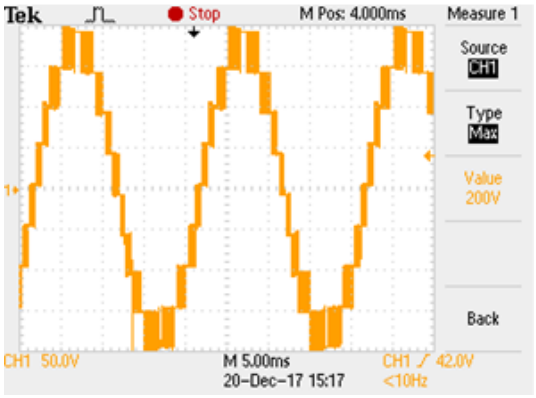


Fig. 31: 5 - Level Line Voltage at 0.8 MI.

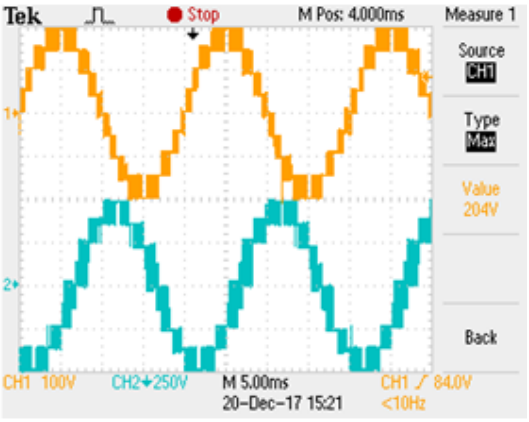


Fig. 32: 5 - Level Line - Line Voltage at 0.8 MI.

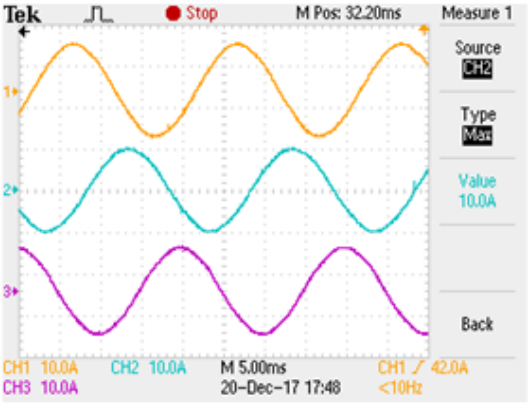


Fig. 33: 5 - Level Phase Currents at 0.8 MI.

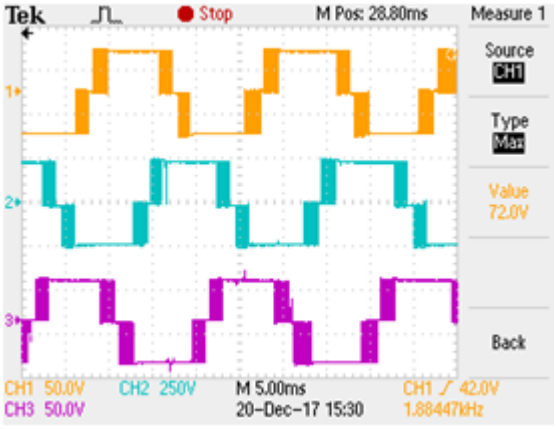


Fig. 34: 3 - Level Phase Voltage at 1.2 MI.

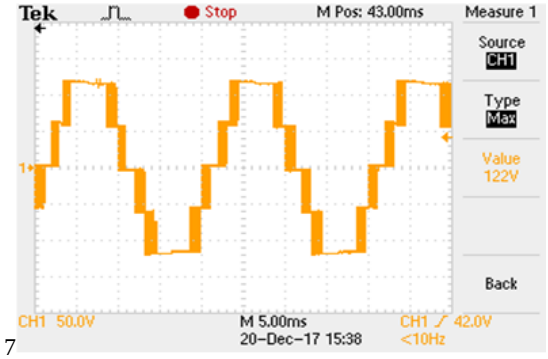


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Fig. 35: 3 - Level Line - Line Voltage at 1.2 MI.

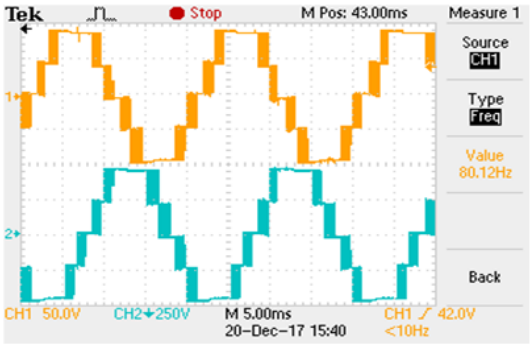

Fig. 36: 3 - Level Line - Line Voltage at 1.2 MI.

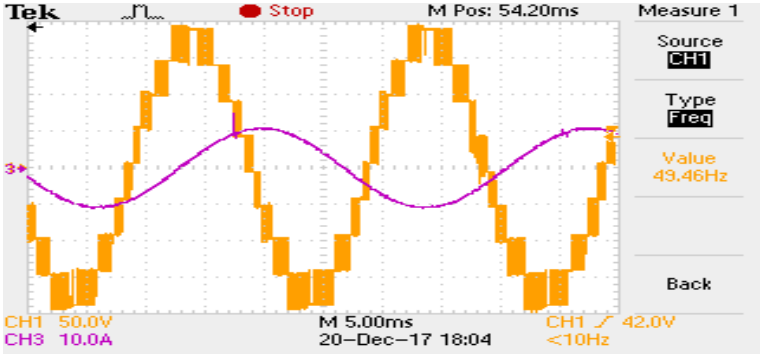

Fig. 37: An Interfaced Five Level Line Voltage and Current at 0.8 MI.

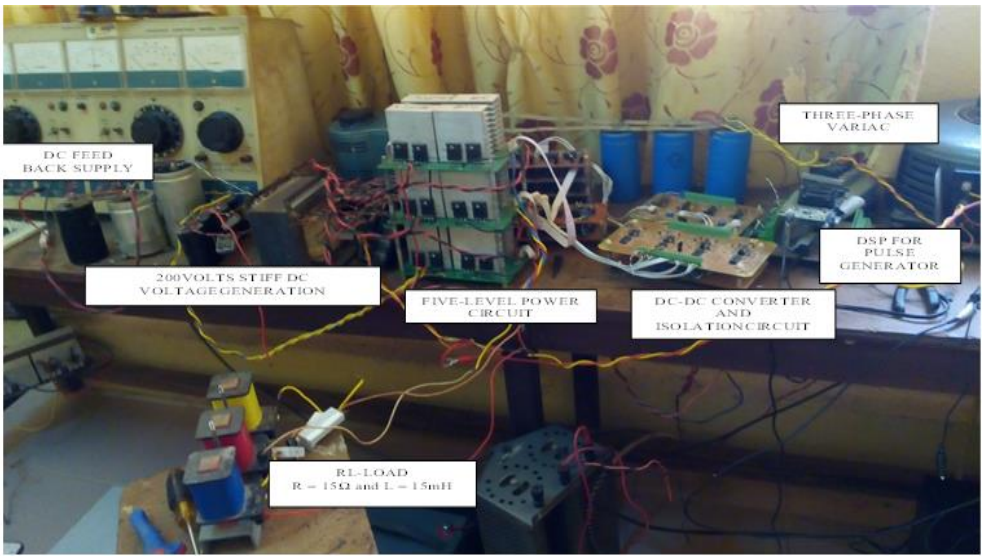

Fig. 38: Laboratory Set Up of the RL-Load with the Power Circuit and DSP.

7. Conclusion

Hybrid multi-level inverters (Types A and B) were analyzed under an unbalanced and a well-balanced capacitor voltage condition. The rate of rise in the capacitor voltage deviation from the reference voltage value was investigated for 0V, 100V and 200V pre-charged capacitor voltage values. The transient response of the capacitor voltage with pertinent to the above pre-charged condition was also analyzed. The dynamic response of the capacitor voltage in relative speed to changes in the capacitor values from 7500 µF to 1500 µF was discussed. The effects of faults occurrence on the two types of the hybrid multilevel inverters were underscored. The fault analysis indicated that type B five-level ANPC inverter albeit producing a three-level inverter waveforms of the same voltage magnitude and power rating of a five-level generates more harmonic values of 92.10% and 84.94%. These harmonic values can lead to thermal run away and total malfunction of the semi-conductor switches. Similarly, type A hybrid inverter under fault occurrence on the H-bridge produced a three-level inverter waveforms of the same voltage magnitude and power rating of a five-level but generates less harmonic values of 35.77% and 23.79%. The experimental results carried out and presented in Figures 34, 35 and 36 under a bypassed H-bridge showed that a close similarity exist between the simulated results presented in Figures 14 and 15 which validates the research paper.

Acknowledgement

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