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Research paper

Design of Dual Stage 180nm CMOS High Gain Low Noise Amplifier for 5G Applications

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Abstract

Low noise amplifier (LNA) is an important block in receiver front-end as it is used to amplify the weak signals from the antenna. This paper presents a design of low noise amplifier for 5G applications based on 180nm CMOS technology. LNA is designed to operate at 26 GHz in the K-band. The proposed circuit is a two stage LNA composing of a common-source followed by a Cascode stage. To minimize the noise figure (NF), the common-source (CS) structure along with the noise cancellation technique is employed in the first stage. The Cascode structure is used in the second stage to enhance the power gain and provide better reverse isolation. The measurement result depicts that a gain of 17.105 dB and noise figure of 1.016 dB at 26 GHz is obtained. The input and output impedance matching have been performed to achieve S_{11} of -19.185 dB and S_{22} of -38.884 dB. The circuit is designed and simulated using Advanced design system (ADS) software.

***Keywords*:** *ADS, CMOS, Low noise amplifier, Noise canceling, 5G*

1. Introduction

Low noise amplifier is the first important component in the Radio Frequency (RF) front-end; it has significant effect on the performance of the whole system. LNA amplifies the weak signal which is in the order of -100dBm or μV to 1/2V or 1V. Low noise amplifiers are widely used in a variety of applications like ISM radios, wireless LANs, GPS receivers, and satellite communications. LNA plays an active role in the receiver system since the noise performance is greatly determined by it. By using the Friis equation, it is significant to reduce the noise figure and increase the gain of the amplifier for better performance.

The 5G wireless communication has rapidly increased the requirements to the performance of transceiver. The millimeter wave wireless systems however have some major technical challenges like less data rate, limited coverage and high power consumption, less reliability, etc. In the later years, III-V compound semiconductor technologies including GaAs were employed for mm-wave communications. But currently, the CMOS technology is developed in the nanometer range, it is sufficient to use CMOS because of its low cost and high integration.
A highly linear LNA has been designed for K-band applications using 180nm CMOS technology. An additional post linearization technique has been adopted to improve the linearity; hence there is high noise figure and reduction in gain [1]. A K-band LNA using 180nm CMOS is designed [3], which consists of three common-source stage for suppressing the noise of the amplifier. A LNA is designed for Ka-band applications using the 180nm CMOS consisting of two cascade amplifier with inductive load and an output buffer [4]. Various other technologies like SiGe:C BiCMOS, GaAs, pHEMT, etc., are being used for designing the LNA. SiGe HBT Low Noise Amplifier for K-band is designed in which a capacitor has been added in the base-collector notch filter to enhance the gain and improve the input match [5].

This paper presents an LNA with an LC circuit given as the positive feedback to the input of the common-source transistor to suppress the noise of the overall circuit. To increase the power gain and improve reverse isolation a Cascode configuration is used at the second stage.

The paper is demonstrated as follows. In section 2, the design of the proposed 5G LNA is described and the circuit parameters needed to design the LNA is tabulated. Section 3 depicts the simulation result of the gain, noise figure, stability, reflection coefficient and reverse isolation in the entire band. The performance comparison of the proposed LNA with existing LNA in the K-band is tabulated. Finally, the conclusion is carried out in Section 4.

2. Proposed 5G LNA

The schematic diagram of the proposed LNA for 5G applications is shown in fig.1. The circuit of the proposed LNA consists of a common-source with noise cancellation circuit in the first stage and cascade topology in the second stage. The input and output matching

circuits are employed to achieve perfect impedance matching. The supply voltage is 1.8V and biasing voltages are given to M_1 of the common-source stage and M_3 of the cascade stage. L_6 is the source degenerated inductor, L_{12} is used as the coupling component between two stages.

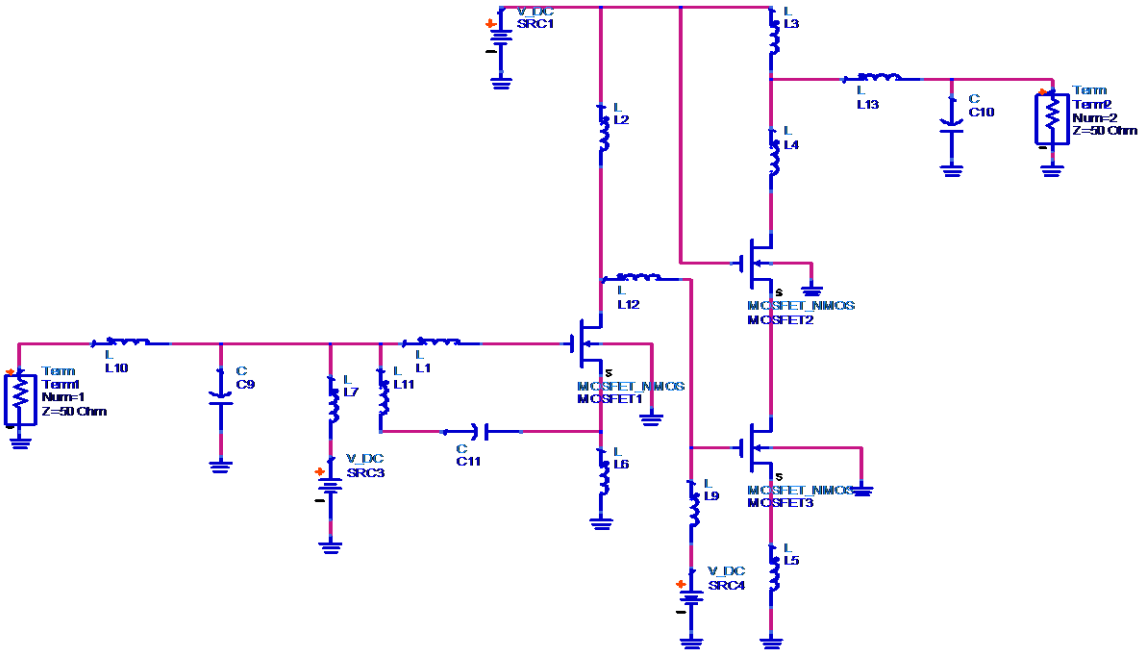

Fig.1: Schematic of the proposed 5G LNA

Table 1: Circuit parameters of proposed LNA

Parameters	Design values
MOSFET1	80µm/0.18µm
MOSFET2	209µm/0.18µm
MOSFET3	85µm/0.18µm
L_1	0.6nH
L_2	0.5698nH
C_{11}	1pF

The design methodology of the LNA is as follows.

2.1 Impedance Matching circuit

Although the common-source topology has high gain and less noise performance, the input matching of this configuration is very poor, hence an input matching circuit is used at the input stage of the amplifier to minimize the input return loss (S_{11}). The input matching circuit composes of L_{10} and C_9. The circuit of the input matching network is shown in fig 2.

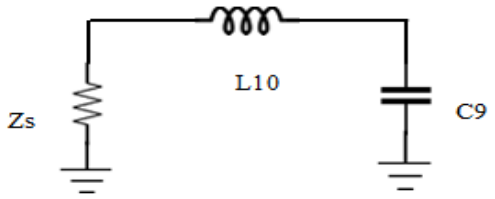

Fig.2: Circuit of input matching network

The proposed circuit has input impedance (Z_{in}) which is derived as follows.

$$Z_{in} = j\omega L \,//\, 1/j\omega C \quad (1)$$

$$Z_{in} = j\omega L*1/j\omega C/(j\omega L+1/j\omega C) \quad (2)$$

$$Z_{in} = j\omega L/(-\omega^2 LC+1) \quad (3)$$

The next step in designing LNA includes the output matching. To maximize the power transfer to the load and minimize the reflections the input and output impedance matching is required. The impedance matching is performed using the Smith chart.

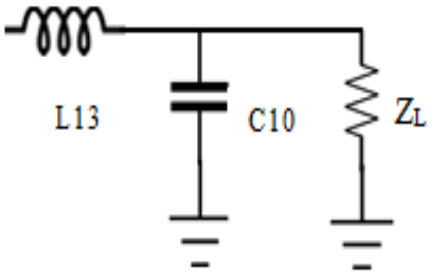

Fig.3: Output matching circuit

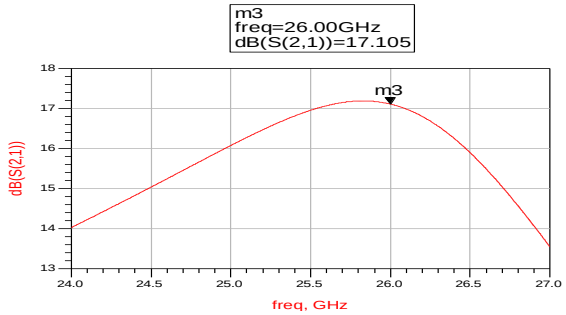

Fig.4: Gain vs frequency graph of the proposed LNA

The output impedance (Z_{out}) is derived as follows.

$Z_{out} = j\omega L+1/j\omega C$ (4)

$Z_{out} = (-\omega^2 LC+1)/j\omega C$ (5)

2.2 Noise Canceling Principle

The noise figure is one of the important parameter which should be considered while designing a low noise amplifier. The minimum noise figure is dependent on the size of the transistor and the bias condition. The proposed circuit uses a positive feedback network consisting of LC components which act as the noise canceling circuit. The common-source configuration is used at the first stage to suppress the noise. But using this configuration doesn't reduce the noise figure greatly; hence an additional noise canceling technique should be used to reduce the noise figure to a great extent. The noise canceling circuit consists of L_{11} and C_{11}. By using the positive feedback the gain of the stage is enhanced such that the contribution of noise of the subsequent stages can be suppressed greatly.

3. Simulation Results

The proposed LNA is designed using 180 nm CMOS technology at 26 GHz with a supply voltage of 1.8V. The circuit is designed for 5G applications which operate in the frequency range from 24.25 to 27.5 GHz. The various performance parameters like the S-parameters, Gain, noise figure and stability were measured using Advanced Design System (ADS) software.

3.1 Gain, Return loss and Reverse isolation

The S-parameters of the proposed LNA is shown in fig.4. It can be viewed that the gain (S_{21}) achieved is above 10 dB for the entire frequency range. The input impedance obtained is approximately 50 Ω by using the input matching circuit. The Cascode configuration is used at the second stage to improve the power gain and the reverse isolation of the amplifier. The input reflection coefficient (S_{11}) is less than -10 dB at the operating frequency i.e., 26 GHz. The output impedance is exactly 50 Ω, hence S_{22} obtained is -38.884 dB at 26 GHz. The reverse isolation (S_{12}) obtained is below -27 dB over the entire range of frequency. This is due to the Cascode topology used at the second stage of the circuit.

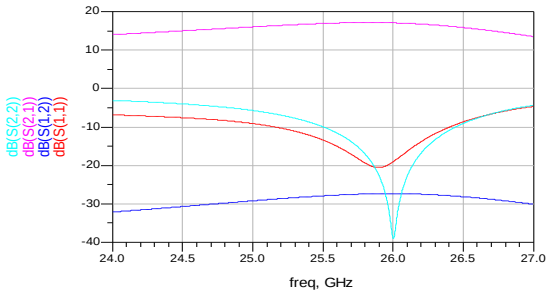

Fig.5: S-parameters of the proposed LNA

The return loss can be evaluated using the reflection coefficient with the equation given below:

$RL = -20\log(\Gamma)$ (6)

3.2 Stability factor

The widely used metric for the study of stability characteristics based on S-parameters involves the use of stability factor K, given in (7),

$K = (1+|\Delta|^2-|S_{11}|^2-|S_{22}|^2)/(2|S_{21}||S_{12}|)$ (7)

$\Delta = S_{11}S_{22} - S_{21}S_{12}$ (8)

For the amplifier to be unconditionally stable, K should be greater than 1 and Δ should be less than 1. The value of K obtained is 1.77 that is depicted in fig.6.

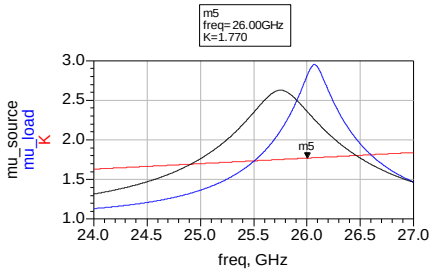

Fig.6. Graph of Stability factor

3.3 Noise figure

The plot for Noise figure (NF) of the proposed LNA is depicted in fig.6. The NF curve shows that the NF is below 2 dB over the entire frequency range. At the operating frequency 26 GHz the noise figure achieved is 1.016 dB. The minimum noise figure (NF_{min}) is 0.940 dB.

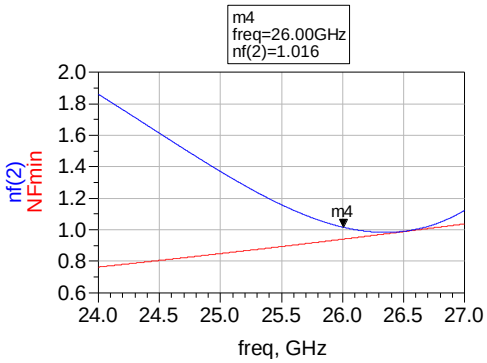

Fig.7. Plot of NF for the proposed LNA

4. Conclusion

A low noise amplifier for 5G application operating at 26 GHz using 180nm CMOS technology is presented in this paper. The proposed 5G LNA consists of a positive feedback in the first stage of the amplifier acting as the noise cancelling circuit. Tuning was also performed in the proposed circuit to achieve sufficient gain. At 26 GHz a gain of 17.105 dB, noise figure of 1.016 dB was achieved. The input and output matching circuits are added to achieve proper impedance matching. The input reflection coefficient (S_{11}) of -19.185 dB is achieved. The performance comparison between the proposed 5G LNA with previously proposed work is tabulated in table 2. In summary, the proposed amplifier attains high gain and low noise figure.

Table 2: Performance Comparison with Existing LNA's

Reference	Technology	S_{11} (dB)	S_{21}/A_v (dB)	NF (dB)	V_{dd} (V)
[1]	180nm CMOS	< -9	13.8	4.3	1.8
[3]	180nm CMOS	-	12.86	5.6	1.8
[4]	180nm CMOS	< -5.8	9.5	4.7	1.8
[11]	180nm CMOS	-15.9	16.5	7.4	1.8
This work	**180nm CMOS**	**-19.185**	**17.105**	**1.016**	**1.8**

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