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Research paper

Dynamic Threshold MOSFET for Low Power VLSI Circuit Design

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Abstract

In this abstract, we investigate a noble low power VLSI logic design technique by applied substrate bias to MOSFET & control threshold voltage (VTH) of MOSFET device i.e. dynamic threshold MOS (DTMOS) logic design for combinational digital logic gates. DTCMOS logic design has larger driving ability with low leakage current (i.e. low power dissipation) as compare to ratio-less static CMOS logic design. DTMOS approach that takes advantage of partially-depleted SOI technology, by providing an fitting substrate bias that varies according to gate voltage(VG), As we know that the VTH of the device is depending on its VG (i.e.by vary gate voltage we control the VTH of MOSFET). Under above circumstances, an improvement in delay while using less power than conventional transistors can be achieved. The behavioural comparison of DTMOS & CMOS logic design circuit are funded with respect to parameters such as Power dissipation, Propagation delay & Figure of merit evaluated through circuit simulator CAD tool HSPICE.

Keywords: *Dynamic threshold MOS; Silicon-on-Insulator; substrate bias; propagation delay; SPICE*

1. Introduction

Recent trend of the International Technology Roadmap for Semiconductors (ITRS), now a day highly scale microprocessors generates more heat dissipation due to dynamic & static power dissipation of miniature area of CMOS devices. The power dissipation in CMOS is directly depending upon supply voltage that can reduce for compensating it [9]. When we reduce power supply then ratio-less static CMOS device does not work properly and goes to standby mode in addition to dissipates static power dissipation. However the speedy spread of battery operated manageable systems robustly demands a reduction of both active power as well as standby power. We know that very high speedy devices operated with ultra-low-power will be dissipates static power in most of the VLSI applications. Traditional CMOS, does not meet all the requirements of high performance VLSI circuits in low power utilization [6].In the low power application its required scaling of the supply voltage, which cause the reduction of gate overdrive & small area of CMOS device also reduces threshold voltage, which leading to severe degradation of the circuit speed in terms of sub-threshold leakage current [6].According to dynamic power dissipation as shown in equation (1) CMOS digital circuits, required power is proportional to the square of power supply voltage.

$$P_D = C_{LOAD} * V_{DD}^2 * f \quad (1)$$

Where, C_{LOAD}=Load Capacitance, V_{DD}=Power Supply, f =Frequency. Thus, Dynamic threshold MOS is a promising accomplish high performance. The V_{TH} of Dynamic threshold MOS falls as the gate voltage is increased, subsequent in a higher current driving ability with low leakage current as match up to ratio-less CMOS logic for ultra-low power applications[5].

2. Device Structure

In this paper a device was proposed with common substrate and gate voltage, which reduce leakage current, which indicate that higher current driven than conventional CMOS for minimum power drive. At gate to source voltage is equivalent to 0V indicating lower value of threshold voltage, therefore the leakage current is low. The body of a dynamic threshold MOS is coupled to its gate, it can lead to an tremendously high trans-conductance under very low supply voltages. The V_{TH} of a DTMOS transistor is given as-

$$V_{TH} = V_{THO} - \gamma \times (2\Phi_f)^{1/2} + (2\Phi_f - V_{SB})^{1/2} - \eta \times V_{DS} \quad (2)$$

Where, V_{TH} is V_{TH} when source to body voltage(V_{SB}) is not zero, V_{THO} is threshold voltage at zero body bias & mainly depends on manufacturing process coefficients. Where γ is the body effect coefficient (typically equals to 0.4-0.5 V) & it depends on the gate oxide capacitance(C_{OX}), silicon permittivity(ε_r=3.9), doping level & other parameters like surface potential, which is equal to $2\Phi_f$ at threshold (typically $|-2\Phi_f|$ equals 0.6 V).The term $\eta \times V_{DS}$ represents the effect of Drain-Induced Barrier Lowering (DIBL), In which η is the DIBL coefficient (its range of

0.02–0.1)[5].Results concluded that the excellent DC characteristics down to V_{DD} = 0.3V to 0.2V for DTMOS [4].

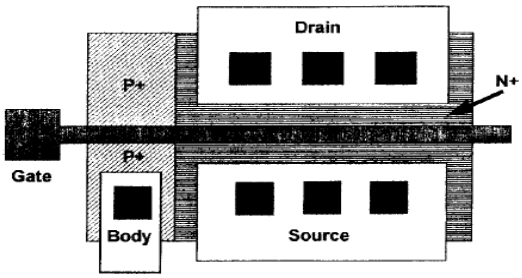

Fig. 1: Physical Representation of the body contact in SOI MOSFET device.

DTCMOS devices are basically used SOI based fabrication technique, which is suitable for low power VLSI application. The SOI devices modeling used in the research are constructed on SIMOX & BESOI substrates. A 4-terminal device structure was used to offer split SOURCE, DRAIN, GATE & body contact. Besides the 4-terminal electrode with limited gate-to-body connections were also made-up as shown in fig1. Above connection uses a whopping metal to high doping P type semiconductor contact window aligned over a "hole" in the poly gate [8]. The metal shorts the gate & P+ region. Thus, there is no considerable penalty in area [10,11].To operating the DTMOS, floating body & gate of a SOI CMOS are coupled collectively[10]. Hence, because of very small junction areas, drift current & capacitances are appreciably reduced. dynamic threshold MOS based circuits used principle of forward bias i.e. when input is high, the transistor will be ON, resulting in reduction of V_{TH} & higher driving capability & cross section schematic shown in fig.2 [10].

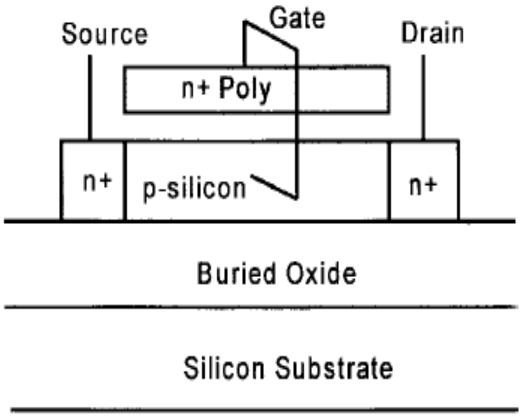

Fig. 2: Structural View of SOI NMOSFET with Shorted gate and substrate

3. MOSFET & DTMOS Configuration

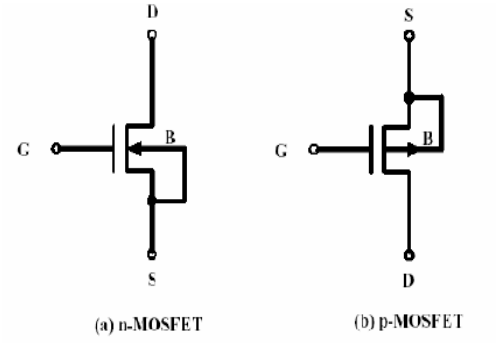

Fig. 3(a): MOSFET Structure

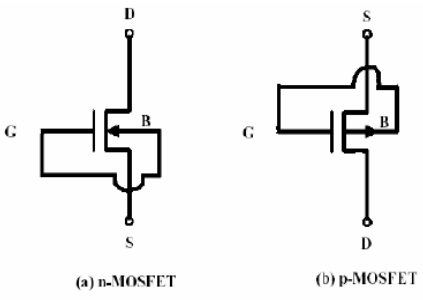

Fig. 3(b): DTMOS structure

Typical schematic configuration of CMOS & DTMOS are shown in fig 3(a) & 3(b), the substrate is always connected to source terminal of device, because source to substrate voltage always equal to zero (V_{SB}=0V) in conventional operation . Comparing above with DTMOS, the substrate & gate both are tied together & hence always with same potential. Thus, DTMOS device uses substrate bias behave as dual threshold logic gates, resulting in more efficient, minimizing power dissipation, decreasing leakage current ,increasing thre3shold voltage & decreasing propagation delay [1]. DTMOS with substrate bias is an excellent approach to offer ultra-low power VLSI circuits with improved speed but optimized figure of merit compared to conventional CMOS in the sub-threshold region.

3. Experimental Analysis

3.1. DTMOS Logic Gates

First introduces DTCMOS Inverter as shown in fig.4(a).The threshold voltages of the devices are 0.22V for N-MOS & -0.22V for P-MOS. W_N & W_P is selected as 200 nm & 400 nm, which are the respective widths of the transistors. For the simulation the supply voltage of devices is 5V,which is below the threshold voltages of both the devices.

The DC voltage V_{AP} is applied between substrate and gate for P-MOS, which bias the gate negative with respect to substrate. Similarly we applied V_{AN} for the N-MOS with opposite polarity, Due to these both of the transistors operate in the low current region. For simulation of DTMOS inverter, we can vary V_{AN} from 0 to 0.2V and V_{AP} from 0 to -0.2V. For Bias substrate V_{AN}=0 & corresponding V_{AP}=0.2, the performance of DTMOS inverter, DTMOS TWO-input NAND gate & DTMOS TWO-input NOR gate is analyzed in terms of propagation delay, power dissipation & FOM [1].

A.DTMOS Inverter

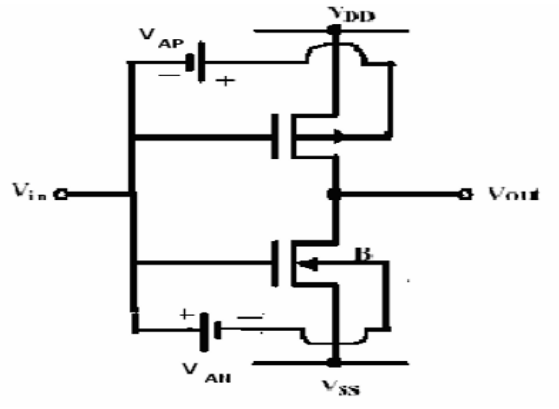

Fig. 4(a): DTMOS Inverter

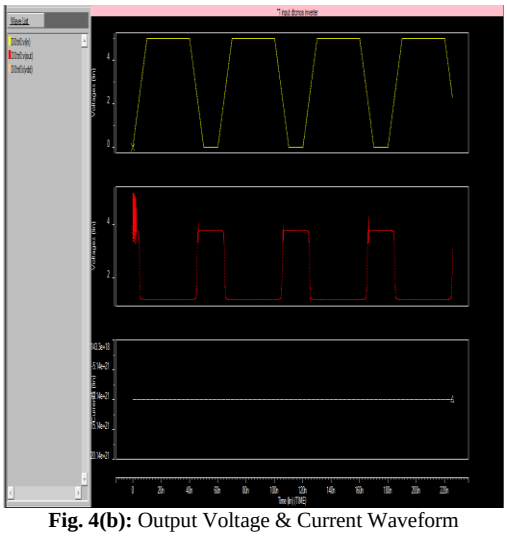

Fig. 4(b): Output Voltage & Current Waveform

B.DTCMOS NAND Gate:

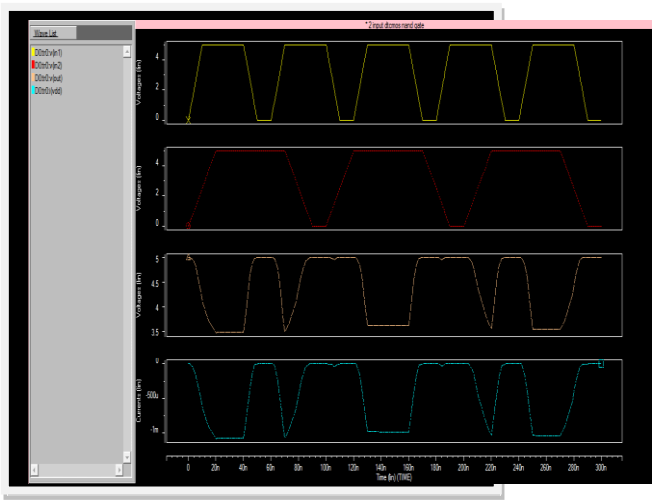

Fig. 5: Output Voltage & Current Waveform on HSPICE

C. **DTCMOS NOR GATE**

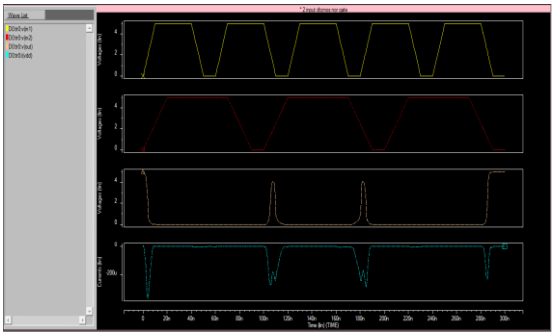

Fig. 6: Output Voltage & Current Waveform on HSPICE

4. Result Analysis:

In the following section we have described the calculative results based on the previous simulations.

4.1. Power Dissipation (P_D)

Also referred as the power consumed per gate. It is the major factor that we have tried to reduce to the maximum extent in the DTMOS circuits as compared to conventional CMOS. From experiential measure mentions in Table 1,the power dissipation just reduces approximately 40-50% in DTCMOS logic circuits as compare to CMOS logic circuits.

Table 1: Comparison of power dissipation

POWER DISSIPATION $P_D = V_{DD} * I$ *(n-Watt)*	CMOS Circuits	DTMOS Circuits
Inverter	0.30	0.15
NAND	0.35	0.20
NOR	0.35	0.20

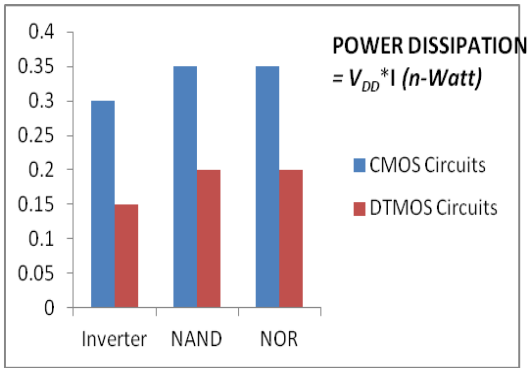

Fig. 7: Bar graph of CMOS and DTMOS circuits for power dissipation

4.2. Propagation Delay (P_D)

Propagation delay is defines as average of propagation delay from low to high (T_{LH}) & high to low (T_{HL}). It is the factor that lies at the marginal values in the DTMOS circuits as compared to the conventional CMOS. From experiential measure mention in Table 2,the propagation delay is approximately equal in both logic circuits.

Table 2: Comparison of propagation delay

PROPAGATION DELAY $T_P = (T_{PLH} + T_{PHL})/2$ *(n-sec)*	CMOS Circuits	DTMOS Circuits
INVERTER	15	16
NAND	18	20
NOR	18	20

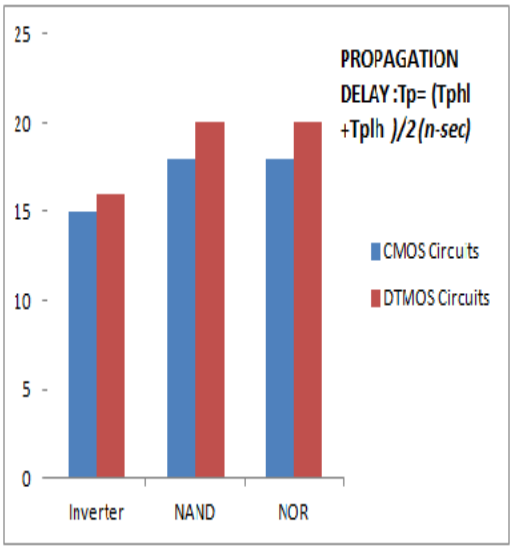

Fig. 8: Bar graph of CMOS and DTMOS circuits for propagation delay

4.3. Figure of Merit (FOM)

FOM is an important parameter for VLSI circuit, which is defined as product of power dissipation & propagation delay. From

experiential measure mentions in Table 3 ,the figure of merit are compare for both logic circuit.

Table 3: Comparison of FOM

FIGURE OF MERIT $P_D \times T_P \times (10^{-18})$ Watt-sec	CMOS Circuits	DTMOS Circuits
INVERTER	4.5	2.4
NAND	6.3	4.0
NOR	6.3	4.0

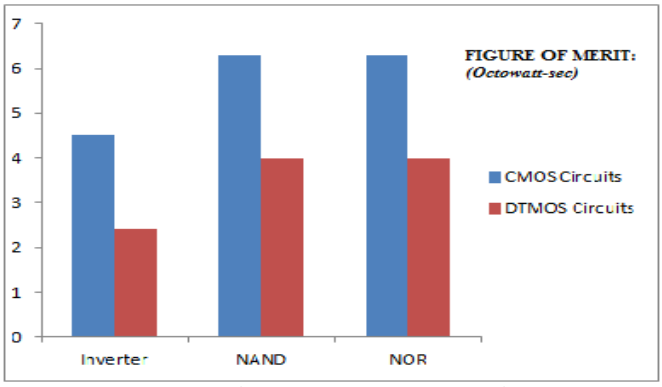

Fig. 9: Bar graph of CMOS and DTMOS circuits for FOM

5. Conclusion

In DTMOS logic design, we see from result analysis table and graphical analysis, DTCMOS logic design gives 50% less power dissipation as compare to CMOS for same design parameter technology as well as lesser power dissipation in case of NAND & NOR also. Figure of merit in case of DTCMOS is also optimized in cast of increasing propagation delay i.e. substrate biasing technique used in case low power VLSI applications, where mainly concentrate on lesser power dissipation.

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