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Performance of Potential Distribution of CSDG MOSFET Using Evanescent-Mode Analysis

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Abstract

In nanotechnology, to overcome the restriction on the scaling (sizing) of the MOSFET, a cylindrical structure of MOSFET is suitable. It increases the switching speed, current flow and packaging density. In this research work, analytical 2D model for potential distribution of Cylindrical Surrounding Double-Gate (CSDG) MOSFET has been derived, based on 2D Poisson solution using Evanescent-Mode analysis. The impact of Short Channel Effects (SCEs) on the channel potential has been evaluated which is based on the device parameters such as channel length, drain to source bias voltage, silicon thickness, and oxide thickness. Also, the derived closed-form expressions surface potential for both the inner and outer gate of the CSDG MOSFET produced a relatively the same results. The accuracy have been validated through the simulation analysis.

Keywords: CSDG MOSFET, 2D analysis, Potential distribution, Microelectronics, Nanotechnology, VLSI.

1. Introduction

For the last few decades, the downscale of MOSFETs devices has been the driving force of the semiconductor industry [1]. The main motive behind the transistor scaling is to increase functionality, speed, low operating power and packing density of the IC. However, the downscaling of the device has led to problems of Short Channel Effects (SCEs) such as threshold voltage roll-off and Drain Induced Barrier Lowering (DIBL) as the major effects [2-5]. *Srivastava et. al.* [6] have discussed that Double-Gate (DG) MOSFETs provides lower short channel effects, higher transconductance, and better scalability which is of greater roadmap for CMOS technology than typical MOSFETs. However, the fabrication of DG MOSFETs, especially the alignment of both gates to achieve better performance and the control of threshold voltage becomes major challenges [7].

It has been established that Multi-gate MOSFETs such as Double-Gate (DG) MOSFETs and Cylindrical Surrounding-Gate (CSG) MOSFETs has emerged as a better immune to SCEs [8-12]. Despite the fabrication problems of DG MOSFET, CSG MOSFETs poses a better immunity to SCEs as proposed by *Oh et. al.* [13] using Evanescent-Mode Analysis (EMA) [14]. Also, the CSG MOSFETs provides greater coupling of the gate around the silicon pillar, resulting to better controllability of the gate over the MOSFET channel and low leakage current. But in terms of current drive the CSG MOSFETs have lesser current compared with the DG MOSFET, hence its use becomes limited for high performance [15]. So, the need for the modification of the CSG MOSFET becomes a necessity to boost the current drive and improve the SCEs immunity since below 100nm gate length, SCEs becomes non-negligible.

The CSDG MOSFETs offer high packing density, greater controllability over channels and better immune to SCEs in cylindrical regime [16, 17]. As a result of this, it makes CSDG MOSFETs a promising structure in the recent 22 nm technology node [18]. *Srivastava et. al.* [19-21], presented an explicit model of CSDG MOSFT based on unified charge control model. The authors derived the channel current expression for the structure with the terminal charges, transconductance, trans-capacitance and drain conductance as a function of structural parameter and applied voltage. However, the authors did not consider the subthreshold characteristics in their model. In 2015, *Verma et. al.* [22] proposed a new CSDG structure with in which they provided a physics based analysis of CSDG MOSFETs at the subthreshold characteristics to investigate the threshold voltage and subthreshold behaviour. However, the authors assumed non-hollow concentric cylindrical structure in their analysis making which is different from *Srivastava et. al.* [21]. In 2017, *Hong et. al.* [23] presented a general 1D Poisson equation model for CSDG MOSFET, based on special variable transformation method. However, the authors did not consider the subthreshold characteristics in their model. Also, in 2017, *S. Bairagya and A. Chakraborty* [24] proposed a model for the electrical characteristics of CSDG MOSFET in strong inversion region. In their approach, they solved the 1D Poisson equation in CSG MOSFET, and then extend the result to

obtain the CSDG MOSFET model. However, they considered only the strong inversion region in their analysis.

The proposed CSDG MOSFETs has a hollow concentric cylindrical structure in which a simple analytical channel potential model has been derived at subthreshold regime, where the charge carriers are neglected. In the CSDG structure, the 2D Poisson equation is solved with the EMA as a boundary valued problem to obtain the minimum surface potential. Its performance is investigated with the device parameters. We assumed a minimum silicon body thickness of 5nm and this caused the quantum mechanical effects to be negligible [25]. This paper is organized as follows: The structure of CSDG MOSFET and EMA flowchart has been described in the Section 2. The Poisson equation of the proposed CSDG structure with the boundary condition and its analysis have been discussed in the Section 3. Finally, Section 4 concludes the work and recommends the future aspects.

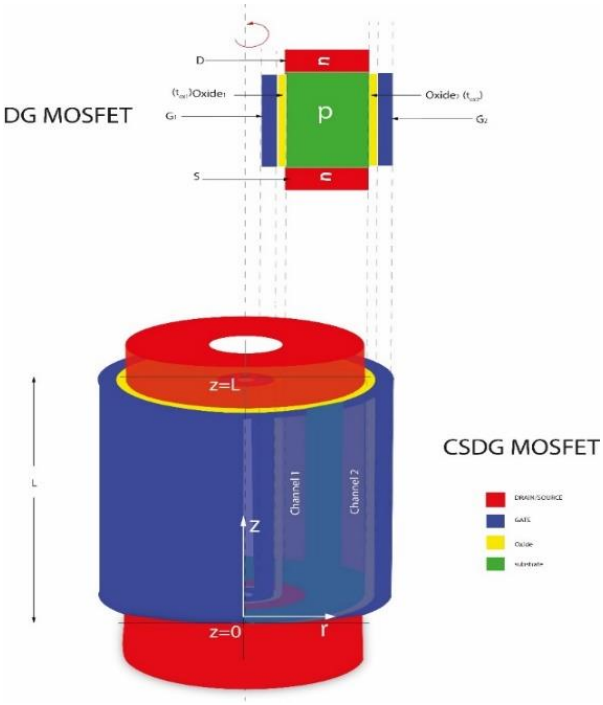

Fig. 1. 3D view of proposed CSDG MOSFET in cylindrical structure [26].

2. Structure of CSDG MOSFET and EMA Model

2.1. CSDG MOSFET Structure

The CSDG MOSFET is an extended rotatory version of DG MOSFET [26, 27] and an advanced version of CSG MOSFET which comprised of Drain, Source, Gate oxide, gate and silicon substrate. It belongs to GAA MOSFET family. The DG MOSFET has two gates (*Blue colour*), the oxides (*Yellow colour*), the drain/source (*Red colour*) and a silicon substrate (*P, Green colour*).

When this DG MOSFET is rotated with respect to the reference point, the first gate (G_1) forms the inner radius ($r = a$) with a circular thin oxide to immune the effect of SCEs. The second gate (G_2) forms the outer radius ($r = b$) with circular thin oxide, forming a hollow concentric cylinder [26, 27]. Between the oxides is the silicon substrate, while the extension forms the source and drain part of the cylinder as shown in the Fig. 1.

2.2. Evanescent-Mode Analysis

The best approach in solving the 2D Poisson equation is by considering the oxide and silicon regions as a two-dimensional analysis, to produce physically consistent results. This can be achieved if the 2D Poisson equation is split into 1D Poisson for both the oxide and silicon region and 2D Laplace for the drain/source SCEs in the channel potential. For this reason, the EMA is used as shown in the flowchart in Fig. 2. The EMA provides solution to the 2D Poisson equation and accurately predicts the potential in the entire device channel.

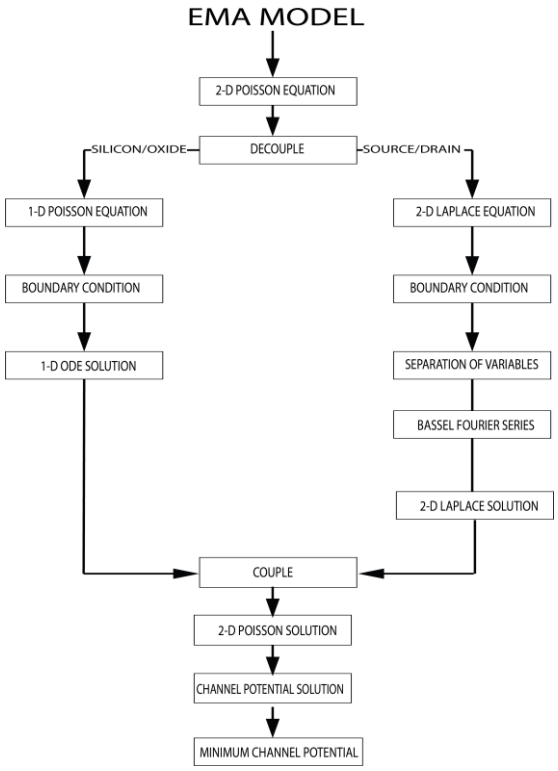

Fig. 2. EMA model flow chart [29].

3. Poisson Equation Modelling and Its Analysis

In the subthreshold (weak inversion) regime, the 2D channel potential region, $\psi(r, z)$ is determined from cylindrical Poisson's equation in the cylindrical coordinate system. Assuming uniform channel doping and the independency of the channel potential on the angle θ as highlighted by [28], the 2D Poisson equation is expressed as:

$$\frac{d^2\psi(r,z)}{dr^2}+\frac{1}{r}\frac{d^2\psi(r,z)}{dr^2}+\frac{d^2\psi(r,z)}{dz^2}=\frac{qN_A}{\varepsilon_{si}} \quad (1)$$

The solution to the Equation (1) to yield Equation (2) to Equation (5) is found in our previous publication [29]. The theoretical and numerical simulation results are presented here using Equation (4) and Equation (5). The list of parameters used for the CSDG MOSFETs are given in table 1.

$$\psi(r,z) = (V_{GS} - V_{FB}) - \psi_{1D}(0) + \frac{qN_A a^2}{4\varepsilon_{si}} - \frac{qN_A t^2_{si}}{16\varepsilon_{si}} - \frac{qN_A t_{si}{}^2 C_{si}}{4\varepsilon_{si} C_{ox-a}} + \left(A_0 e^{(z\lambda_0)} + B_0 e^{(-z\lambda_0)}\right) J_0(a\lambda_0) \quad (2)$$

$$\psi(r,z) = (V_{GS} - V_{FB}) - \psi_{1D}(0) + \frac{qN_A b^2}{4\varepsilon_{si}} - \frac{qN_A t^2_{si}}{16\varepsilon_{si}} - \frac{qN_A t_{si}{}^2 C_{si}}{4\varepsilon_{si} C_{ox-b}} + \left(A_1 e^{(z\lambda_{01})} + B_1 e^{(-z\lambda_{01})}\right) J_0(b\lambda_{01}) \quad (3)$$

$$\psi_S(z_{\min}) = (V_{GS} - V_{FB}) - \psi_{1D}(0) + \frac{qN_A a^2}{4\varepsilon_{si}} - \frac{qN_A t^2_{si}}{16\varepsilon_{si}} - \frac{qN_A t_{si}{}^2 C_{si}}{4\varepsilon_{si} C_{ox-a}} + \left(A_0 e^{(z_{\min}\lambda_0)} + B_0 e^{(-z_{\min}\lambda_0)}\right) J_0(a\lambda_0) \quad (4)$$

$$\psi_S(z_{\min}) = (V_{GS} - V_{FB}) - \psi_{1D}(0) + \frac{qN_A b^2}{4\varepsilon_{si}} - \frac{qN_A t^2_{si}}{16\varepsilon_{si}} - \frac{qN_A t_{si}{}^2 C_{si}}{4\varepsilon_{si} C_{ox-b}} + \left(A_0 e^{(z_{\min}\lambda_0)} + B_0 e^{(-z_{\min}\lambda_0)}\right) J_0(b\lambda_{01}) \quad (5)$$

The surface potential distribution at both silicon-oxide interfaces is shown in Fig. 3. It has been observed that at *0 V* and *0.5 V* drain to source bias voltage, the inner and the outer surface potential are approximately the identical. Also, as the drain voltage increases to *0.5 V*, both Potential increases towards the drain end which indicating mutual dependence on the threshold voltage. The model is verified with the numeric simulation.

Table 1 The device parameters for simulation

Parameters	Values
t_{ox1}, t_{ox2}	2 nm to 5 nm (each)
L	9 nm to 90 nm
a	3 nm - 6 nm
b	13 nm
$t_{si} = (b\text{-}a)$	10 nm
N_A	10^{17} cm^{-3}
Φ_{MS1}, Φ_{MS2}	4.8 eV
V_{DS}	0.1 V

The potential distribution for the radii difference between the outer and the inner radius of the CSDG MOSFET (silicon film thickness) is shown in Fig. 4. It has been observed that the radii difference is inversely proportional to the minimum surface potential. As the radii difference decreases, the minimum surface potential position increases. The controllability of the two gates (inner and outer) over the channel increases. Therefore, smaller radii difference enhances the device for better immunity to SCEs. The surface potential behaviour at various oxide thickness is shown in Fig. 5. The minimum surface potential position increases by pulling upward due to decrease in oxide thickness. This is because as the oxide thickness reduces, the more the penetration of the vertical electric field into the channel from the gates. Thereby increasing the gate control over the channel and the effect of threshold degradation is controlled. Hence, thin oxide is better preferred to suppress SCEs in CSDG MOSFET. The numerical simulation results obtained are in good agreement with our model.

The performance of the surface potential at different channel length is shown in Fig. 6. At channel length of *30 nm – 100 nm*, the minimum surface potential flattens. Showing better improvement of SCEs due to the coupling of the double surrounding gates.

However, at channel length of less than *30 nm*, the surface potential position rises upward gradually and loses its flatness due to minor drain and source impacts on the channel. The proposed model is in good agreement with numerical simulation.

The potential distribution with various gates to source voltage at constant zero drain to source voltage is shown in Fig. 7. As observed, there is an increase in the minimum surface potential as the gate to source voltage increases and flattens out at higher voltage showing the better immunity to SCEs. The numerical results obtained agree with the simulated results.

The surface potential result at various drain to source voltage values with zero gate bias is shown in Fig. 8. It is examined that as the source to drain voltage increases, the surface potential increases at the drain end; which indicating that the threshold voltage is inversely dependent on the drain bias. The numerical results obtained agree with the results simulated.

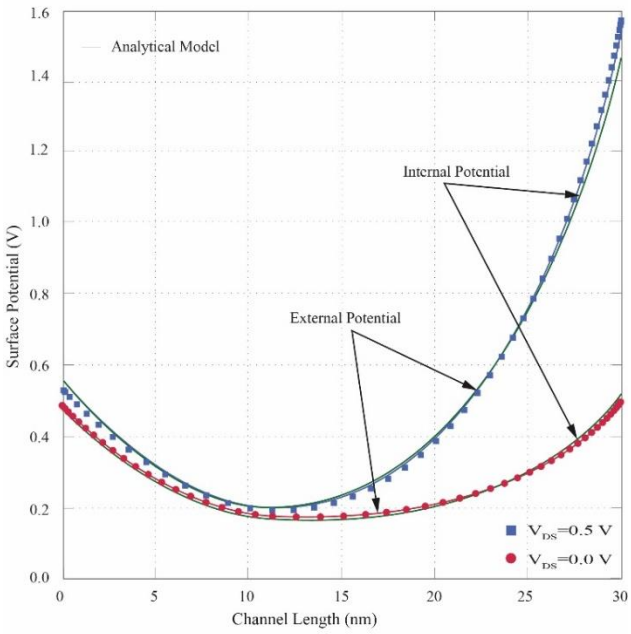

Fig. 3. Potential distribution of the inner and outer CSDG MOSFET by model and numerical simulation at *0 V* and *0.5 V* bias drain voltage.

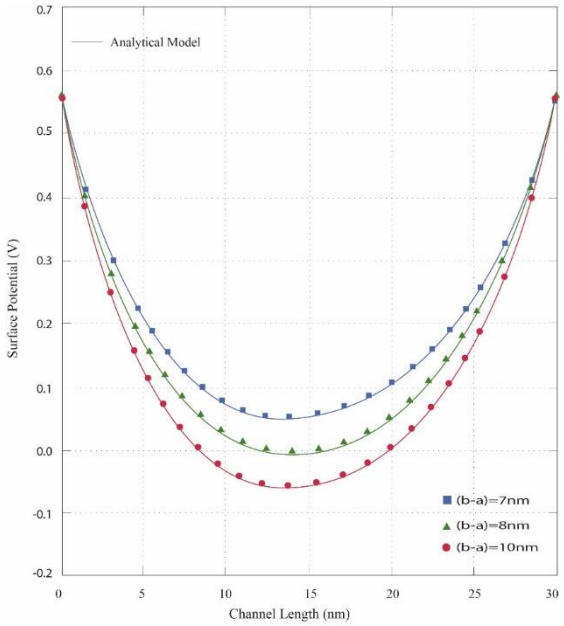

Fig. 4. Potential distribution for the radii difference between the external and internal radius of CSDG MOSFET at various Silicon thickness.

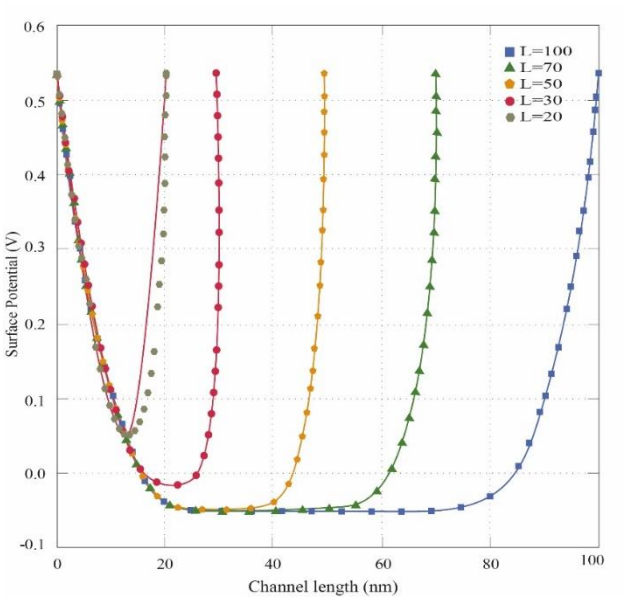

Fig. 6. Potential distribution of the external Surface of CSDG MOSFET along channel length.

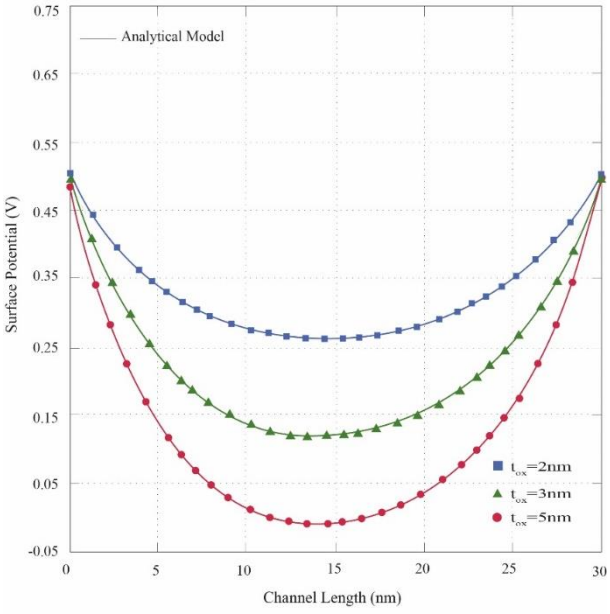

Fig. 5. Potential distribution of the external gate surface of CSDG MOSFET along the channel length.

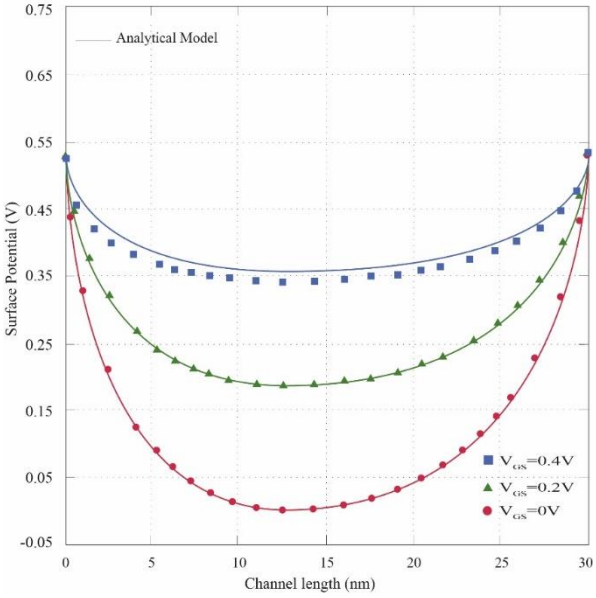

Fig. 7. Potential distribution of the external surface of CSDG MOSFET along channel length.

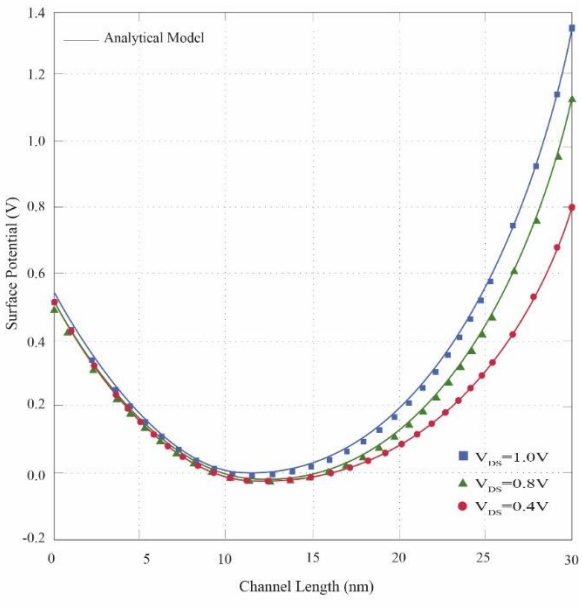

Fig. 8. Potential distribution of the external surface of CSDG MOSFET along channel length.

4. Conclusions and Future Recommendations

In this research work, a simple channel potential model for CSDG MOSFET has been obtained by solving the 2D Poisson equation using Evanescent-mode approach to improve the performance of the device. The channel potential has been verified with different parameters to show the performance of the device structure. It is found that as the channel length decreases up *30 nm*, the device is immune to SCEs due to flatness of the minimum channel potential. This makes our proposed structure a more promising device for Nanotechnology. Also, the surface potential increases with decrease in gate oxide, thereby enhancing the gates controllability over the channel. Furthermore, the smaller the radii difference, the better the gate control over the channel. Good agreement is observed with numerical simulation.

However, the close form expression of the model can be extended to model the threshold voltage and subthreshold swing behaviour of the proposed CSDG MOSFET structure. Also, future research work can be done by including the quantum mechanical effects.

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