International Journal of Engineering & Technology, 7 (4.38) (2018) 732-736

International Journal of Engineering & Technology

Website: www.sciencepubco.com/index.php/IJET

Research paper

Performance Analysis of a Universal Circuit for Reversible ALU using QCA & CMOS Technology

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Abstract

The reversible logic and gates are one of the promising and upcoming technologies which are capable of overcoming the limitations of the design and applications based on the CMOS technology. In this technology, the schematic arrangement of the device is implemented in such a way that every input terminal has been provided with individual output terminals. The author has used the technology which is based on quantum computations with a basic feature of loss of energy in small amount. It has many advantages like very high operating speed, low energy dissipation, and high device density. An adder/subtractor is heart of arithmetic units of processors i.e. acts as universal circuit for carrying out the mathematical computations in the quantum processors. The author has put forward a novel reversible adder/subtractor circuit using reversible logic & QCA. The QCA based circuit reported by the author has been compared and analyzed for the performance on the basis of number of gates, size, delay, power dissipation etc. The experimental work has been completed with the use of the most suitable and reliable software i.e. QCA and the performance of the proposed circuit has proven to be quite useful for this circuit to be used in some promising applications. These results are also compared with those obtained with the use of CMOS Technologies.

Keywords: *Reversible Logic, CMOS, Universal Circuit, ALU, Quantum Computing.*

1. Introduction

The concept of the reversible logic has developed a new era of the technology in support with another innovative concept based on the quantum i.e. the role of the photons in the performance of the systems. With this approach, it has become quite feasible to implement a device with low power dissipation, small size, less delay, high speed, etc. With this approach, one can easily eliminate the limitations which do exist by using irreversible logic approach i.e. the loss of information in terms of the heat dissipation. This logic basically performs a dual operation i.e. a device has an identical output terminals for each individual input terminals. With this technique of the design, it becomes quite feasible to process the given information with much faster rate i.e. less delay and also the loss of the information is also quite minimum [1]. In this paper, the author has come up with an innovative universal circuit using QCA tool which is capable of performing the most important computations for ALU of the quantum process. In this circuit, the prime focus has been put on the basic calculations of addition as well as subtraction with a single circuit. In addition to this, with this proposed circuit, emphasis has been made on reducing the no of cells i.e. high density in addition to other prime features. This manuscript flow has been started with an introduction to the topic with some literature survey on the reversible logic & QCA, basics of the mathematical computation of the ALU, discussion of the proposed circuit and then the last section delays with the performance analysis of the 3 bit universal circuit using reversible gate for the ALU of quantum processor.

2. Reversible Logic & Gates

The concept of reversible & irreversible logic is basically dependent on the capability of the system to hold or retain the previous bit of the information. On the basis of the comparison between these two approaches, it has been also found that in addition to retaining the previous bit of information, the reversible logic has also got dedicated output terminals for each input. Due to this behavior, the gates based on this logic negligible power loss in addition to small delay i.e. quite high speed and accurate to acceptable range. Due to all this, this has formed the basis for a new and upcoming technology i.e. QCA based various computations in the domain of quantum, DNA, Nano,

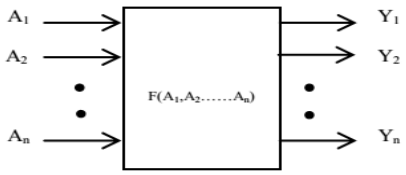

Fig. 1: Reversible Logic [1]"

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etc. The reversible gate is a basic cell of reversible circuit, which can be further extended to build large reversible circuits as shown in below Figure 1.

Table 1: Reversible Function"

Input		Output	
a b	Permutation	x y	Permutation
0 0	0	0 0	0
0 1	1	0 1	1
1 0	2	1 1	3
1 1	3	1 0	2

The various reversible gates discussed in the literature survey of the problem enunciation are the NOT (Feynman, 1985), CNOT (Feynman, 1985), Toffoli (Toffoli, 1980), Fredkin (Fredkin & Toffoli, 1982) and Peres (Peres, 1985) gates, which are demonstrated in Figure 2**,** with inputs a, b and c and their respective response x, y and z shown in Table 2 [2-3].

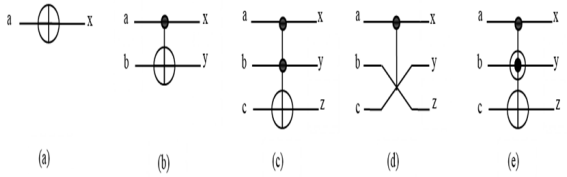


Fig. 2: Reversible gates (a) NOT, (b) CNOT, (c) Toffoli, (d) Fredkin and (e) Peres[2]"

Table 2: Responses of Reversible Gates"

	x	y	z
NOT	a'	-	-
C-NOT	a	ab	-
Toffoli	a	b	c=ab
Fredkin	a	a'b+ac	ab+a'c
Peres	a	ac+b	ab+c

3. QCA

In order to understand the behavior and performance of this technology, we can have a comparative analysis of the two technologies on the basis of the channel length i.e. microns and nano technology. It is well known that the microns technology normally depends upon the flow of the electrons as the majority charge carriers in the device as compared to the Quantum Dot Cellular Automata (QCA) in which the charge wells known as quadratic cells are the dominant parameter, placed in square nanometer as shown in below Figure 3 & 4. Based on this concept, we can design the quantum cells as per the need of the applications in addition to the supplementary modules such as various input, output and processing modules of the signal processing. The below given Fig. 4 shows a general arrangement of electrons in single QCA cell. The below shown Figure. 5(a), 5(b) and 5(c) & 6, a null polarized, positive polarized and negative polarized QCA cell respectively [3].

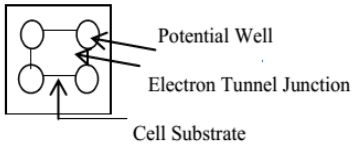


Fig. 3: Structure of QCA Cell".

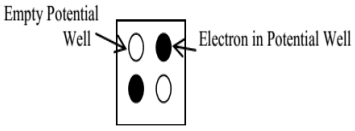


Fig. 4: Electron Arrangement in Potential Well."

The information flow or transfer of the data in a cell can be discussed nothing but swapping of the state of the charge carriers within the quantum cell. It can be also stated as the phenomenon of the tunneling of the majority charge carriers which acts quite fast so as to enhance the overall execution speed of the circuit. The below given Figure. 7 shows the schematic arrangement of the various devices designed using the basic QCA elementary gates [4].

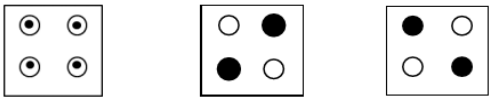


Fig.5: Polarization in QCA Cell"

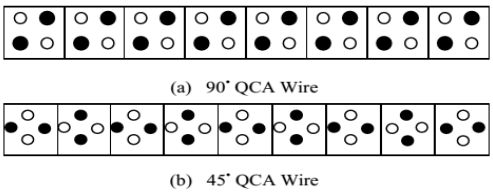
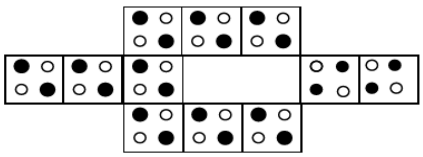
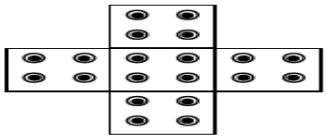


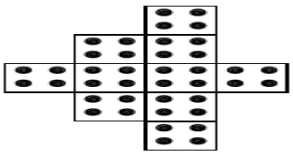
Fig. 6: QCA Wires"



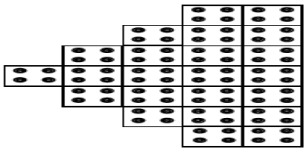
(a) QCA Inverter



(b) Three Input Majority Voter



(c) Five Input Majority Voter



(d) Seven Input Majority Voter

Fig. 7: Basics of QCA Gates [5]"

The following Figure 8 shows the clocking scheme and Figure 9 shows four different phases of the clock pulse applied to the device based on the concept of the nano technology which plays a dominant role in the proper functioning of the circuit [Chen, J., Zhang et. al

2008, Chua, S et. al 2014]. In addition to this, the below given fig. 10 shows the different phases for different clock pulses with reference to the time domain.

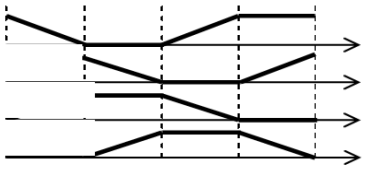


Fig. 8: Clocking scheme in QCA"

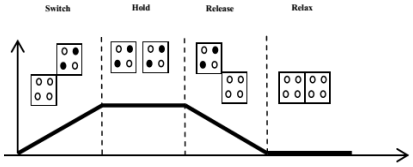


Fig.9: Phase description of a QCA clock"

Time

Clock 0	Switch	Hold	Release	Relax
Clock 1	Relax	Switch	Hold	Release
Clock 2	Release	Relax	Switch	Hold
Clock 3	Hold	Release	Relax	Switch

Fig.10: Phase in clock Zones"

3. Universal Computational Circuit (Adder cum Subtractor)

There are so many reversible adder and multiplier implementation methods [M. Haghparast et. al 2016]. Adders are widely used in data processing and computing circuits such as Arithmetic Logic Unit (ALU) of processors. The performance of modern processors is decided by the speed, area, and power consumption of adders and subtractor. Hence, the design of a robust universal circuit in QCA technology is basic necessity for a high performance ALU [6-7].

$$Sum = A \oplus B \oplus C_{in} \quad (1)$$

$$C_{out} = A.B + B.C_{in} + C_{in}.A \quad (2)$$

$$D = A \oplus B \oplus B_{in} \quad (3)$$

$$B_o = A'C + A'B + B_{in} \quad (4)$$

Table 3: Truth Table of 3 bit Full Adder"

A	B	C_{in}	S	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

The schematic arrangement of the universal circuit which carries out all the essential calculations for the ALU as shown in the below Figures 11 & 12. The Boolean performance of the proposed device can be easily analyzed with the help of the truth table given shown in below table 4 & 5. The generalized Boolean equations for the universal circuit as shown in above figures [8-12].

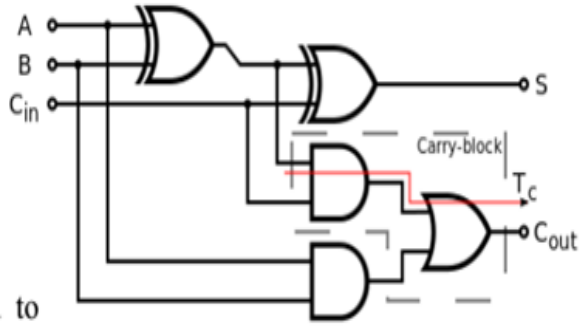


Fig.11: Circuit Diagram of Full Adder"

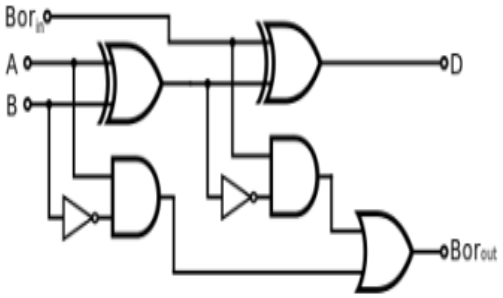


Fig. 12: Circuit Diagram of Full Subtractor"

Table 4: Truth Table of 3 bit Full Subtractor"

A	B	C_{in}	S	C_{out}
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	1	0
1	0	0	0	1
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

4. Proposed Reversible Universal Circuit of Computational Circuit (Adder cum Subtractor)

An exhaustive literature survey has been carried out by the author so as to choose the most efficient reversible gate in order to design and implement the proposed design of universal circuit for an ALU of the quantum processor. Based on this discussion, it has been found that with the use of the RQG gate the resultant circuit can provide the desired performance as shown in below Figure 13 (a). This reversible gate has got three inputs with dedicated outputs terminals. The Boolean expression for each out of this reversible gate is given below i.e.

$$Y_1 = Maj(X_1 X_2 X_3) = X_1.X_2 + X_2.X_3 + X_1.X_3 \quad (5)$$

$$Y_2 = Maj(X_1' X_2 X_3) = X_1'.X_2 + X_2.X_3 + X_1'.X_3 \quad (6)$$

$$Y_3 = X_1 \oplus X_3 = X_1.X_3' + X_1'.X_3 \quad (7)$$

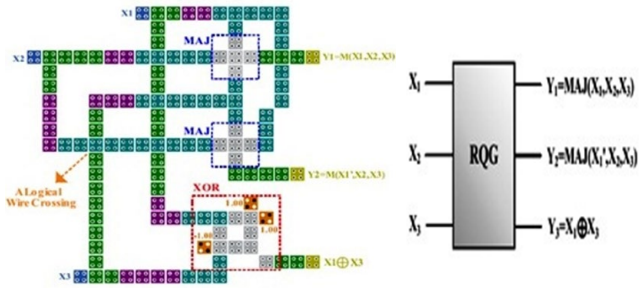


Fig. 13: Schematic Circuit using QCA (a) Block Diagram (b) QCA based Layout

The above figures 13 (a) & (b) represents the block diagram as well the lay out circuit of the most commonly used reversible gate i.e. RQG. It has been implemented with the use of the most commonly used software tool due to its distinct features and results.

Table 5: Operational Behavior of RQG Gate

X1	X2	X3	Y1	Y2	Y3
0	0	0	0	0	0
0	0	1	0	1	1
0	1	0	0	1	0
0	1	1	1	1	1
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	1	0	1
1	1	1	1	1	0

This above considered gate (i.e. RQG) is one of the most commonly and universally accepted one to design and implement the proposed circuit of the universal adder cum subtractor for the ALU of the quantum processor. The performance of this circuit can be easily evaluated simply by verifying the truth table of the gate using the standard Boolean expressions. These Boolean expressions are elaborated further with the help of the equations given from 08 to 10. The below given Figure 14 shows the schematic block diagram of the proposed circuit of the universal adder/subtractor. It has been observed that this circuit provides an output of x⊕y with the given input signals. In addition to this, here we have also used another reversible gate i.e. FG so as to obtain the final three input based output of the proposed circuit. The three main outputs of the circuit provides the resultant output as shown in below subsequent equations 8 , 9 & 10, where Sum and Diff are the sum and difference of the three inputs, respectively and C_{out} and B_{out} are the output carry and borrow, respectively. The truth table of the proposed reversible universal circuit is shown in Table 6, which indicates the completely one-to-one mapping between the inputs and outputs.

$$C_{out} = Maj(A, B, C) = A.B + B.C + A.C \quad (8)$$

$$B_{out} = Maj(A', B, C) = A'.B + B.C + A'.C \quad (9)$$

$$Sum = Diff = A \oplus B \oplus C = A.B.C + A'.B'.C + A'.B.C' + A.B'.C' \quad (10)$$

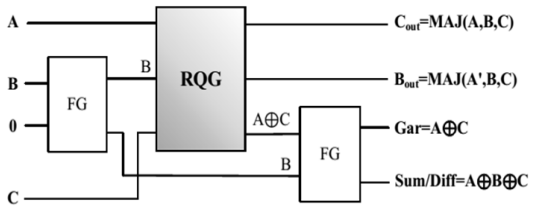


Fig. 14: Proposed Reversible Universal Circuit"

Table 6. Proposed Universal Circuit Behavior"

A	B	O	C	Cout	Bout	Sum/Diff	Gar
0	0	0	0	0	0	0	0
0	0	0	1	0	1	1	1
0	1	0	0	0	1	1	0
0	1	0	1	1	1	0	1
1	0	0	0	0	0	1	1
1	0	0	1	1	0	0	0
1	1	0	0	1	0	0	1
1	1	0	1	1	1	1	0

5. Performance Evaluation of the Proposed Circuit

The design and implementation of the universal circuit has been carried out by utilizing the QCA Designer tool. For this simulation work, the most desired parameters of the circuit has been set to the values with which one can get the best performance and as per the need of the quantum processor. The figure 16 given below presents the simulation results of the universal circuit that validates the functionality of the proposed circuit.

The Table 7 presents the comparative analysis of the proposed circuit with the existing model of the circuit on the basis of the modeling of the most important parameters which forms the basis of the performance of the universal circuit using reversible logic gates. From this above table 7, it has been observed that the circuit put forward by the author has only single garbage out as compared to the other models existing in the domain. In continuation to this comparison, it is also found that the resultant output of GO and CI is two which is smaller in values as compared to the other ones. Now on the basis of the clock zone parameter of the circuit, the latency of the proposed circuit has been found bit longer than other ones. Finally, on the basis of the above analysis, we can submit that the proposed circuit using reversible logic technique is very much capable of preforming the operation of the addition as well as subtraction i.e. an universal operator with fewer less number of cells and smaller area.

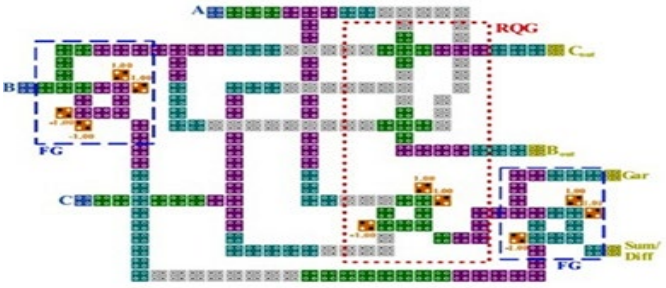


Fig.15: The QCA Implementation of the Proposed Circuit

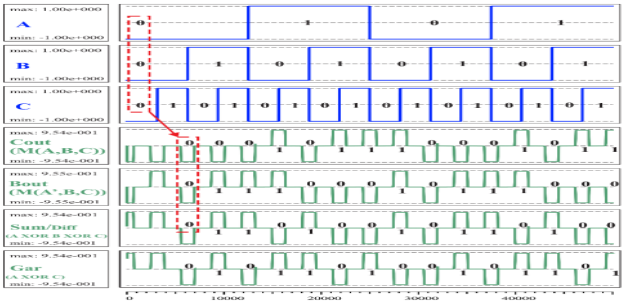


Fig. 16: Simulation Results of the Proposed Circuit"

Table 7: Comparative Analysis of Proposed Universal Circuit"

Designs	Cells	Rotated Cells	Layers	Area (μm2)	Latency (Clock Cycles)	Constant Inputs	Garbage Outputs
QCA1[1]	342	109	1	0.46	1.50	0	3
QCA2[1]	355	104	1	0.47	1.50	0	3
FG+RQCA[3]	516	154	1	0.78	3.25	1	2
RM[7]	611	176	1	0.96	4.00	3	3
[9]	352	0	2	0.41	1.50	0	3
Proposed	**227**	**0**	**1**	**0.27**	**1.74**	**1**	**1**

6. Conclusion & Result Analysis

Thus, with the help of the above comparative analysis & discussion of the performance of the proposed reversible universal circuit using QCA approach, we can submit that it is an innovative design which provides the basic computation of the arithmetic i.e. addition, subtraction, multiplication and division. With the help of the above Table 7, the author has submitted a n interesting and excellent parameters which in turn enhances the overall performance of the ALU of the quantum processor i.e. in terms of the cell count, latency, area, etc.

7. Acknowledgements

The author is thankful to Hon'ble C-VI (Additional President, RBEF and Chairman AUUP, Lucknow Campus), Maj. Gen. K. K. Ohri (AVSM, Retd.) Pro-VC Amity University, Uttar Pradesh Lucknow, Prof (Dr.) Ankur Gupta, Director, MIET Jammu, Wg. Cdr. Dr. Anil Kumar, Retd. (Guide & Director, ASET), Prof O. P. Singh (HOD, ECE.) and Prof. Preeta Sharan, Professor & Co-Guide, The Oxford College of Engineering, Banglore for their motivation, kind cooperation, and suggestions.

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Journal Article

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Conference Proceedings

[12] Rajinder Tiwari, Anil Kumar, Preeta Sharan "Design and Implementation of 4:1 Multiplexer for Reversible ALU using QCA" accepted for oral presentation in the 2nd International Conference on Micro-Electronics & Telecommunication Engineering (ICMETE 2018), a SCOPUS & IEEE Sponsored to be held on 20-21 September, 2018 at SRM University, Ghaziabad, India.

Authors Profile

Rajinder Tiwari has done M.Tech from Department of Applied Sciences, NIT, Kurukshetra in 2002. He has an experience 16+ years in research, industry & academics. Presently, he is associated with Dept. of ECE, MIET, Jammu. He has published about 25 research papers in various Journals of high repute. Mr Tiwari is a senior & lifetime member of IAEng, IETE, MRSI, & UACEEE. His areas of interest are Quantum Computing, Analog CMOS Circuits (VLSI) and Embedded System Design.