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Research paper

Design of CMOS High Linear Low Noise Amplifier for Small Satellite Ground Station

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Abstract:

Ground stations are established to provide communication with the satellite. The quality of communication depends on the performance of satellite ground station in addition to that of satellite. If the ground station is implemented in urban areas, intermodulation interferences affect the front end of the ground station. The non-linearity of low noise amplifier (LNA) is disturbed by these intermodulation products. In ground station, linearity is more important factor in the design of LNA. In this paper, LNA is designed at S band using CMOS technology. Modified derivative superposition (MDS) linearization technique is incorporated in LNA. The performance of high linear CMOS LNA is analyzed with the linearization techniques. This linear LNA is designed using 90 nm CMOS technology that provides good IIP3 value of 5 dBm, 17.7 dB gain, 1.1 dB NF and 5.79 mW power consumption.

Keywords: Satellite, ground station, low noise amplifier and CMOS

1. Introduction:

Now a day, small satellites are enabling technology in developing countries. According to variety of size and mass, small satellite can be divided into minisatellite, microsatellite, nanosatellite, picosatellite, femtosatellite. Ground station is used to establish the communication with the satellite. The important components of the ground station are antenna and its tracking system, transceivers, LNA and control computer. LNA is one of the main components in the ground station and first crucial component in receiver. The RF signal received from the antenna is severely affected by noise. The received signal in ground station is affected by intermodulation products. Careful attention must be given for designing the LNA.

Low noise amplifier (LNA) is a first crucial component in RF receiver design. The important role of LNA is to amplify the received signal with less noise. The linearity of LNA is improved by various linearization techniques such as feedforward, post-distortion, derivative superposition (DS) and modified derivative superposition [1]. The popular linearization technique is DS method. Mayank B. Thacker et al., designed the multistandard high linear LNA using derivative superposition mthod [2]. DS method used the auxiliary transistor which is biased in weak inversion region. In DS, weak inversion transistor is not operated at high frequency and cannot handle large signals. To overcome this drawback, modified

superposition method is approached. In this paper, MDS is used to improve the linearity of LNA.

2. Proposed LNA:

The proposed LNA with MDS technique is shown in Fig.1(a). Since, transistors M1 and M2 are connected in current reuse structure, M1 and M2 share the same bias current from the supply voltage. The current reuse LNA supports high gain and low power consumption. The capacitor C_d is used to reduce the gate induced noise. The ac signal is amplified by the main transistor M1 and is coupled to the gate of common source stage M2 by the capacitor C2. This two stage configuration increases the gain. The LNA is biased in strong inversion region. C1, L_g and L_s are the input matching network components. L_d and C4 are the output matching network components. C1 and C4 are the DC blocking capacitors. C3 is used to ground the ac signal. Inductor Lm is used to provide high impedance between two stages.

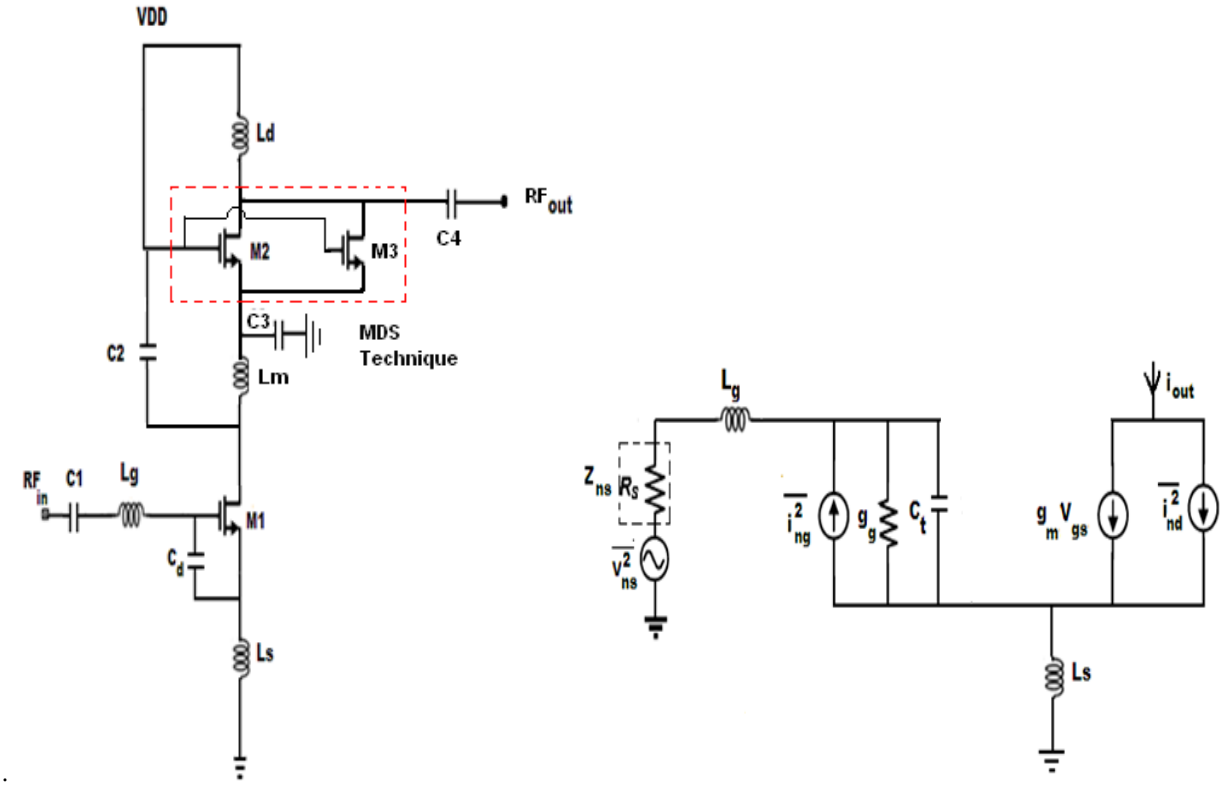

Fig.1(a) Schematic of Current Reuse LNA with MDS **(b)** Small Signal Equivalent Circuit of input stage

The small signal equivalent circuit of input stage is shown in Fig.1 (b). The input matching network is found using the input impedance of IDCLNA which is expressed in Eqn (1) [3],

$$Z_{in} = \frac{1}{j\omega_0 C_t} + j\omega_0 L_t + \left(\frac{g_m}{C_t}\right) L_s \quad (1)$$

where g_m is the transconductance of main transistor. ω_0 is the angular frequency at resonance. The total inductance is expressed as in Eqn (2),

$$L_t = L_g + L_s \quad (2)$$

L_g and L_s are the gate and source inductances. The total capacitance is given in Eqn (3),

$$C_t = C_{gs} + C_d \quad (3)$$

C_{gs} and C_d are the gate-to-source and additional capacitances. The gate to source capacitance C_{gs} is calculated by Eqn (4),

$$C_{gs} = \frac{2}{3} W_{opt1} L C_{ox} \quad (4)$$

The input impedance is to be matched to 50Ω and equating real and imaginary terms in Eqn (1) to find the values of source inductor L_s, gate inductor L_g and the capacitance C_d. The parameters L_s, L_g and C_d are adjusted to obtain the perfect input impedance matching. To improve the linearity of current reuse LNA, modified derivative superposition technique is used.

2.1 Modified Derivative Superposition (MDS) Technique

In MDS method, two transistors which are main transistor and auxiliary transistor are connected in parallel. The main transistor is usually operating in strong inversion region. The auxiliary transistor (AT) is chosen to operate in moderate inversion region instead of weak inversion region, resulting in the contribution of gate induced current noise to noise figure is reduced, and by tuning the sizes and bias conditions of the AT transistors the third-order nonlinear coefficient of current at the output port is closed to zero; thus, causing to extend the linear region. In this paper, the MDS technique is used in an output stage. The main transistor M2 is biased in strong inversion region while auxiliary transistor M3 is biased in moderate inversion region.

Linearity is improved by cancelling out the third order nonlinear current of main and auxiliary transistors so that the nonlinear transconductance (g_m'') is minimized. IIP3 of a nonlinear device is expressed as [4],

$$\text{IIP3} = \sqrt{\frac{4}{3}\left|\frac{g_m}{g_m''}\right|} \quad (5)$$

MDS technique is used to minimize the nonlinear transconductances (g_m'') of main and auxiliary transistors close to zero. IIP3 value of LNA is improved.

3. Results and Discussion:

The proposed LNA has been designed and simulated using Advanced Design System (ADS) software. The important performance metrics for design of low noise amplifier are return loss, gain, noise figure and linearity. The circuit has been designed in 90 nm CMOS technology. It is simulated using S-parameter simulation to measure gain and noise figure. S-parameters are shown in Fig.2. The gain of 17.7 dB and the return loss of -10.5 dB are obtained at a frequency of 2.4 GHz. The LNA has provided enough gain and good input impedance matching.

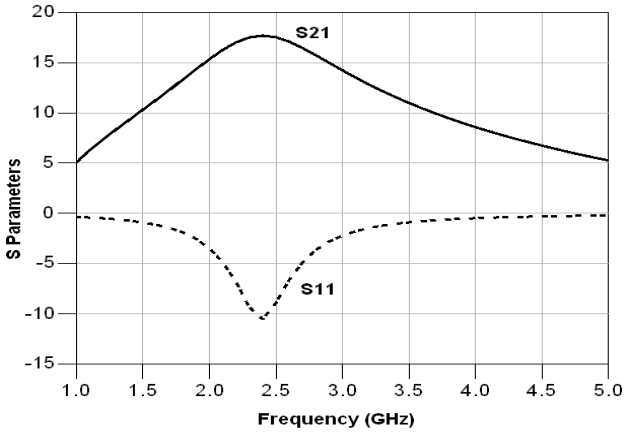

Fig.2 S - Parameters

The noise figure (NF) value of 1.1 dB is obtained as shown in Fig.3.

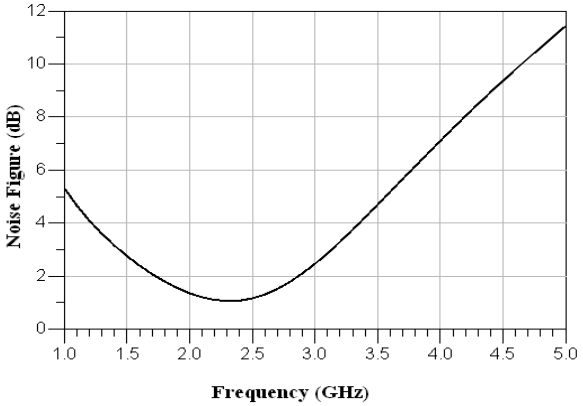

Fig.3 Noise Figure

The important linearity measure of LNA is input 1-dB compression point (P-1dB) and input third order intercept point (IIP3). P-1dB of -18 dBm is obtained as shown in Fig.4. To observe IIP3 value, the two-tone signals with 10 MHz spacing are applied with equal power levels to the LNA. The third order intercept point is the extrapolated intersection of desired output and third order intermodulation (IM) output as a function of input RF level. The obtained IIP3 value is +5 dBm .

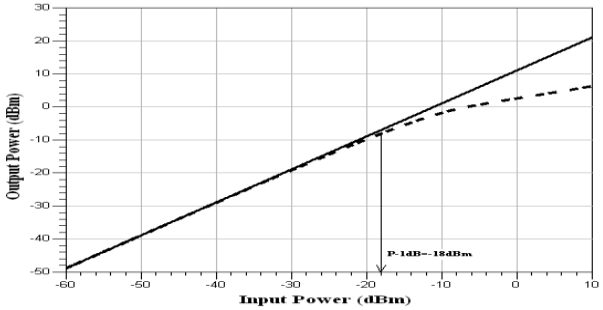

Fig.4 Input P-1 dB Compression Point

The current reuse LNA consumes 4.825 mA current at 1.2 V supply voltage

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4. Conclusion:

A 2.4 GHz current-reused topology LNA utilizing MDS technique is designed for satellite ground station using 90nm CMOS technology. The MDS technique is used to enhance the linearity performance. The simulation results show that the LNA achieves a 17.7 dB gain, -10.5 dB return loss, 1.1 dB NF, 5 dBm IIP3, and a -18 dBm of IP-1dB. The proposed LNA consumes 5.79 mW power at a supply voltage of 1.2 V.

5. References:

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