International Journal of Engineering & Technology, 7 (4.36) (2018) 258-260

International Journal of Engineering & Technology

Website: www.sciencepubco.com/index.php/IJET

Research paper

Design of an On-Chip Tracking ADC

Manju Mohan, N Seenu, Shyam R Nair, U P Vignesh

Centre for Automation & Robotics, Hindustan Institute of Technology & Science, Chennai, India
**Corresponding author E-mail: upvignesh@ hindustanuniv.ac.in*

Abstract

Data acquisition and conversion systems require analog signals to be converted into a digital form that can be used for further analysis. The analog signals are mostly output of sensors and transducers which transform the real-world signals into electrical signals. These electrical signals are modified to digital form by using Analog to Digital Converters (ADC). This conversion involves sampling followed by a quantization of the input signal thus will be converted to digital signal. The bandwidth of the ADC is restricted by the sampling rate and the quantization error should be kept as low as possible for better accuracy. This paper emphasis on the On-Chip design of a 12-bit Tracking ADC using PSoC which is highly reliable for digitizing the slowly varying signals. Complication encumbered in the logic that connects comparator and counter is replaced by using dual comparators, and an XOR gate. The proposed design has immense leverage in providing stable and constant data for instantaneous signal value. The major involvement is shown in making the design very simple, by efficiently using the available components, thus providing much accurate and stable digital data for further processing the slowly varying signal.

Keywords: *ADC, UART, PSoC, LabVIEW.*

1. Introduction

Data acquisition and conversion systems are mostly used for interfacing sensors and transducers. The output electrical signals of sensors are converted to digital form by using Analog to Digital Converters (ADC). Varieties of ADCs are parallel or flash, Counting converter, Tracking ADC, Successive approximation ADC etc. Flash ADC targets at high-speed applications but holds the disadvantage of incurring a large number of components for higher resolution. Successive approximation ADC transforms uses the technique of binary search of all quantization levels for converting the analog waveform into a digital output for each conversion. After each successful conversion, SAR logic sets its initial value to zero and then iterates N times to arrive at a final value, where N is the number of bits. Counting converter is basic and simplest type that employs a counter, a comparator and a Digital to Analog converter. The Comparator can be considered as the basic 1-bit ADC. Since if the voltage input is above voltage reference then the output is logic 1 and if voltage input is below the voltage reference then the output is logic 0 in case of non-inverting type. The output logic is vice versa of the above for inverting type comparator. Input is given to comparator and reference voltage is increased systematically to make comparator output to zero. Hence the current reference voltage can be taken as the required digital value equivalent to the input. In this type, simplicity has traded off with the speed which is very less since the counter has to start counting from zero for each conversion. In order to avoid this, the counter has to maintain the current output value corresponding to the previous analog value instead of going to zero. The analog value to be converted next (current value) may be more or less than the previous one hence the counter will start counting up or down from the previous value instead of zero. Tracking ADC makes use of an up/down counter instead of the normal counter to perform this operation.

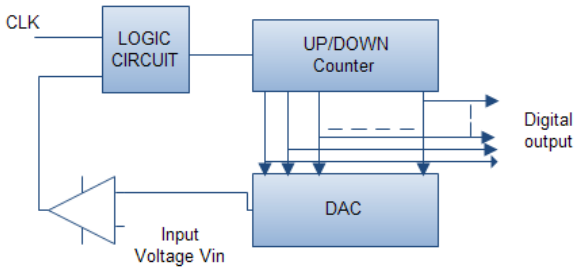


Figure 1: Tracking ADC

Figure 1 shows the basic circuit of tracking ADC consisting of comparator, logic circuit, N bit up/down counter, Digital to Analog Converter (DAC). On the arrival of the clock pulse, the counter starts counting and delivers a digital input to DAC. The corresponding analog output from the DAC is then applied to the op-amp circuit for comparison where it is compared with the input sampled value. Depending on the comparator output, the clock pulse will be sent to the counter so that the counter starts counting up for an input value higher than the DAC output or otherwise the counter starts decrementing on the arrival of the clock pulse. The counter usually increments for the first analog value and further, it may decrement to match with the required value. The digital output can be taken directly from the counter provided the DAC output equals the sampled value. Need for shift register to get the digital data. Since the output of the counter is proportional to the difference between the previous and next sampled value, it is also known as Derivative counter type ADC.

Here, we have proposed an on-chip tracking ADC circuit using Programmable System on Chip(PSoC). The design is made with the available resources in the PSoC board without any analog components hence reducing the noise. Cypress provides a flexible microcontroller, PSoC that can be easily configurable for the

specific work. The CY8C38xxx family built on the PSoC3 architecture is used for the present design.

2. Programmable System on Chip

Cypress provides a flexible microcontroller, PSoC that can be easily configurable for the proposed work. Analog, PLD-based programmable logic, memory and a microcontroller are integrated on a single chip in PSoC which makes it a programmable embedded system-on-chip. There are four microcontroller unit options that range from the cost-optimized 8-bit microcontroller to the high-performance ARM Cortex-M3 for 8-bit and 32-bit applications. The available categories of PSoC are PSoC 1, PSoC 3, PSoC 4, PSoC 5, PSoC 5LP, PSoC Software.
A complete design tool available for the CY8C38xxx family to configure the analog and digital resources within the device is the PSoC Creator. A code editor with a set of pre-built hardware and software components is provided to write the firmware and will be linked to the compiler. Each component has a Schematic symbol, Datasheet, Configuration dialog, API linked with it.

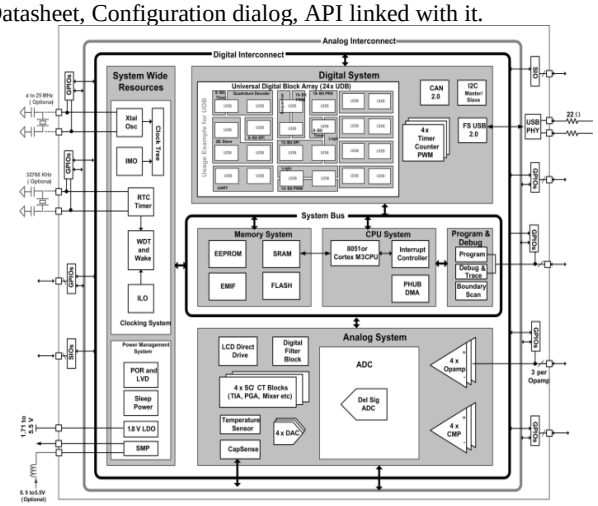


Figure 2: CY8C38 Device Family Block Diagram

The PSoC3 architecture has the accurate analog processing and digital flexibility. The user has the ability to choose the board from the available options for the desired performance as the architecture of the digital and analog peripherals is being the same. The analog and digital systems are integrated on the same chip hence mapping the designs into a lesser physical space. This also keeps the sensitive analog signals within the device itself which makes the design more immune to noise and better stability. The CY8C38xxx family has a single cycle 8051 CPU that runs upto 67MHz. The configurability is given by the Analog and Digital subsystem. Other subsystems that are integrated to its architecture are 8051 CPU subsystem, non-volatile subsystem, programming, debug, and test subsystem, Inputs and outputs, Clocking, Power.
The user can create a new project by selecting the Starter Design in the PSoC creator. The required components in the designed circuit are to be selected and dragged to the schematic design from the Component Catalogue. The parameters of the component are modified to achieve the desired behavior through the configuration dialog box. The required pins for input and output, clock signals, and other components can be added and configured in the same way in order to complete the design. The connections between the different components in the schematic design is made with the Wire tool. Once the design is completed, source code will be created using the Build Command.

3. PSoC Design of Tracking ADC

The Experimental setup is shown in figure 2 consists of the following components:
1. Counter 16 which is made to operate till the maximum count of (2^12) -1 since the word size of DAC is 12 bits.
2. Two comparators to capture the difference in actual input and reference signal exactly
3. 12-bit DAC, that converts, digital data available at the counter to analog data, in order to give a proper reference for comparators (feedback).
4. An XOR gate in order to find when exactly Vref = Vin.
5. A status register that controls the operation of the counter through software control.
6. 2 Clocks, Clock_1 decides basic operation speed of the entire circuit which is 32KHz and Clock_2 that decides the counting speed of the counter that is 500Hz.
7. LCD and Universal Asynchronous Receiver-Transmitter (UART) for displaying the result.

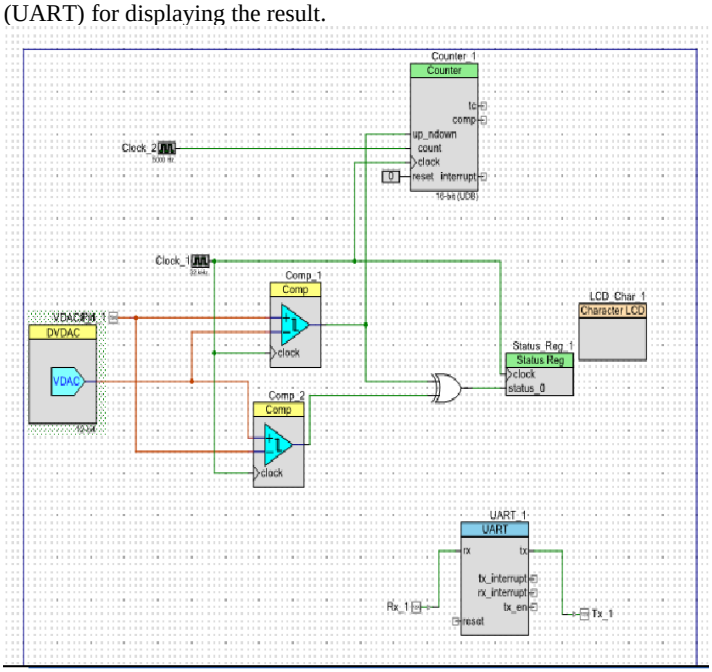


Figure 3: Implementation in PSoC3

Clock speed is decided based on constraints of DAC and Counter. The working of the design is summarized in Table 1.

Table 1: Comparator and XOR values

Relationship between Vref and Vin	Comparator 1 output (I/P to counter)	Comparator 2 output	XOR output and Action performed in the counter
Vref < Vin	1	0	XOR = 1 Counter performs up counting
Vref > Vin	0	1	XOR = 1 Counter Performs down counting
Vref = Vin	0	0	XOR = 0 Counter Stop by using Software control

Using PSoC eventually makes the ADC programmable. ADC can work in two different ranges (0 – 4.080) V and (0 – 0.020) V and number bits representing the sample can also be varied, and possible number of bits per sample is {9, 10, 11, 12}. The restriction is made by the DAC used internally. The speed of conversion and the frequency input to the ADC is also restricted by the DAC circuit involved.

4. Results & Discussion

ADC output when the range of DAC is chosen in as (0 – 4.080) V is given in Table 2 and ADC output when the range of DAC is chosen in as (0 – 1.020) V is given in Table 3.

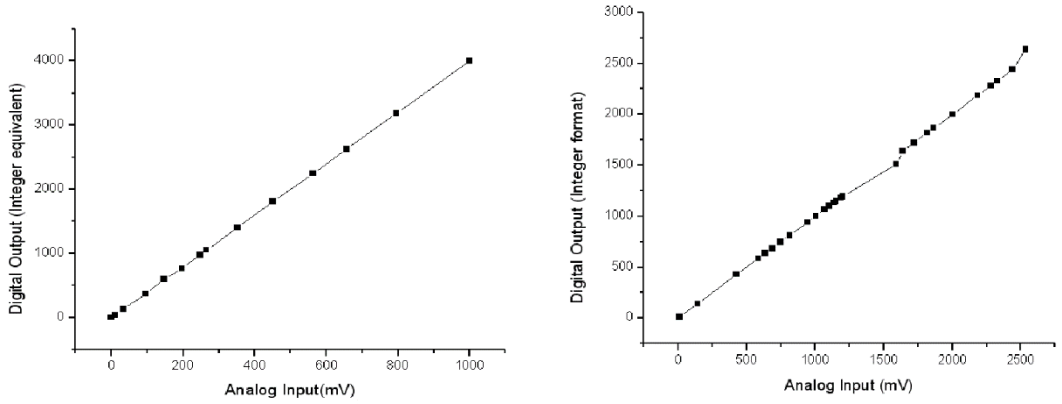
Table 2: ADC Output Readings for (0 – 4.080) V DAC range

Analog Voltage Input(mV)	Digital Count Output
10	10
141	140
586	588
635	637
747	747
812	812
1005	1001
1069	1065
1103	1099
1187	1183
1591	1513
1721	1721
1818	1817
1864	1865
2001	2000
2185	2185
2281	2280
2328	2329
2440	2441
2536	2637

Table 3: ADC Output Readings for (0 – 1.020) V DAC range

Analog Voltage Input(mV)	Digital Count Output
0.25	1
10	38
33.3	130
95.2	370
146.6	600
196.6	763
247.5	973
264.8	1052
352.8	1406
450.5	1804
562.7	2245
656.7	2624
794.6	3180
999	400

It can be clearly observed from the above table the minimum step size possible with the designed ADC is 250microvolt per bit, eventually, that becomes the sensitivity of the ADC designed.



(a) (b)

Figure 4: Analog output Vs Digital output for the DAC ranges (a) 0 – 1.020 V (b) 0 – 4.080 V

In case of ideal ADC step size, increment should be same for equally increasing input levels. It can be seen from the graph shown in Figure 3 that the ADC designed is almost ideal (in case of linearity) for the range (0 – 1.020) V. In case of (0 – 4.080) V it is linear till 1.75 mV, after that a constant linearity error occurs which is corrected using software by checking the range.

5. Conclusion

Digital conversion of natural signals for further analysis is made possible by the ADC. RTD signal had been read out using the designed ADC. The advantage of this design is to build the efficient ADC, and the further processing circuit and finally communicating the result to the end user through UART or USB-FS communication is possible using this On-chip design. A complete temperature monitoring system can be built just by interfacing PSoC with the LABVIEW. Furthermore, On-chip design has high noise immunity, thus providing better results than individual components in addition to the handy final module available.

References

[1] D.A. Rauth and V.T. Randal, "Analog-to-digital conversion", IEEE Instrumentation & Measurement Magazine, vol. 8, no. 4, pp. 44 –54, Oct. 2005
[2] PSoC Creator, version 2.2, www.cypress.com/?id=2494.
[3] PSoC Programmable System on Chip, Technical Reference Manual, Document No. 001
[4] Ross Fosler, "Getting started with PSoC3", Application Note-AN54181, Cypress Semiconductor Corporation.
[5] S. Rapuano, P. Daponte, E. Balestrieri, L. D. Vito, S. J. Tilden, S. Max, and J. Blair, "ADC Parameters and Characteristics", IEEE Instrumentation & Measurement Magazine 1094-6969/05, 2005
[6] Walter Allan Kester, "Data Conversion Handbook" Analog Devices Inc Engineeri, Analog Devices, inc. Engineering staff - 2005 - Computers