International Journal of Engineering &Technology, 7 (4.24) (2018) 103-107

International Journal of Engineering & Technology

Website: www.sciencepubco.com/index.php/IJET

Research paper

A Comparative Study on Total Harmonic Distortion of Interleave Boost Rectifier with the other Boost Derived Topologies

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Abstract

Boost rectifiers find their applications in the active power factor correction and have been subject to extensive research. Further, various topologies have been introduced, studied and applied in order to make boost rectifiers more and more efficient and better. Accordingly, Bridgeless configuration and Interleaved topology are most popular among others. In this paper, a comparative study between Basic boost rectifier, bridgeless boost rectifier, interleaved boost rectifier and bridgeless interleaved boost rectifier model has been carried out. The differences analyzed are summarized to learn about the best configuration and which can be implemented. Bridgeless configuration reduces conduction losses in the system by removing one diode from line conduction path while two parallel boost converters with anti-phase conduction in a 2-interleaved topology reduces the current ripple. BLIL combines the advantages of both the system in a single circuit.

Keywords:*Bridgeless converter, interleaved converter, bridgeless interleaved converter, BLIL,THD*

1. Introduction

If a simple rectifier circuit is to be considered with RC filter, it is found that power delivered at the load side is half of the power delivered by the input. consequently bringing down system efficiency to almost 50%. High harmonics are present in input current which results in higher Total Harmonic Distortions (THDs), reduced power factor and decreased system performance. This amount of loss can become huge and unacceptable at higher power levels. Any method which increases the system efficiency and reduces the power losses would considerably increase the scope of power management. Hence, arises the need to improve the efficiency of rectification circuits. Boost converters serve this purpose of increased system performance. The general goal of the boost PFC converter is to turn the switch off and on rapidly and with a varying duty cycle so that the input current (I_{ac}) in phase with sinusoidal input voltage. This reduces ripple in input line current thereby decreasing the THD of the system. Fig 1 gives the circuit diagram of boost converter.

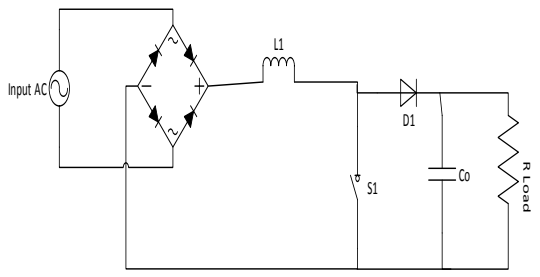

Fig1. Classic boost converter

Boost PFC can be implemented with various topologies and configurations. Among many, Bridgeless configuration and interleaved topology are most studied and applied.

The diode bridge which is present in classic boost converter as shown in Fig 1 will be eliminated in Bridgeless configuration[1][2], while still maintaining the advantages of classic boost converter.

An interleaved boost converter(IBC)[[3][4] is formed by connecting number of boost converters in parallel . The phase number of IBC is nothing but number of such boost converters in parallel. All the parallel connected boost converters will have the same switching frequency and phase shift. A two phase IBC topology is discussed in this paper.

Further in improvement of both the topologies mentioned above, Bridgeless Interleaved Boost Rectifier (BLIL)[5] is presented in this paper which combines the advantages of bridgeless as well as interleaved topologies. The elimination of input diode bridge rectifier reduces switching losses while still maintaining the classic IBC functionality.

2. Circuit configuration and operation principle

2.1 Bridgeless Boost Rectifier

The circuit operation can be described in two half cycles i.e. positive and negative half cycles. During the positive half cycle, current from source flows through inductor L_1, Switch S_1, internal diode of Switch S_2 and flows back into source through L_2 (V_{ac}-L_1-S_1-S_2 Diode-L_2-V_{ac}). During this period, inductor charges with

increase in inductor current linearly until the voltage across inductor equals source voltage. By the end of this period, inductor stores energy which depends on the duration for which the switch in ON.. During OFF period of switch, inductor discharges through diode D_1 and to the capacitor and load (V_{ac}–L_1-D_1-D_o-C_o-R_L -V_{ac}). During the negative half cycle, current direction reverses and now current follows the path (V_{ac}-L_2-S_2-S_1 Diode-L_1-V_{ac}) when switch (S_2) is conducting and charges the inductor L_2 . When the switch is off, inductor discharges through the path (V_{ac}–L_2-D_2-D_o-C_o-R_L -V_{ac}).

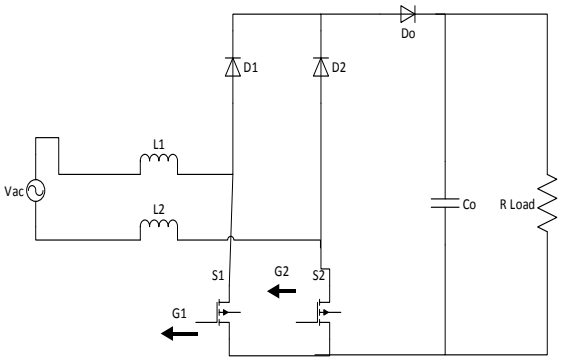

Fig. 2 Bridgeless Boost Rectifier

Unlike the classic boost converter shown in Fig 1, the inductor split and placed at the input side to perform the boost operation in case of Bridgeless boost rectifier as shown in Fig 2..
The two intrinsic body diodes in parallel with the two switches can solve the purpose of diode bridge.

2.2 Interleaved Boost Rectifier

During mode 1, both *S1* and *S2* are on at the same instant which makes the diodes *D1*and *D2* reverse biased. The equivalent circuit is shown in Figure 3(a). Inductors L_1 and L_2 are charged by input source. The voltage across inductors after charging depends on the time period of charging or the duty cycle.
During mode 2, the switch *S1* is in on condition and switch *S2* is turned off which makes D1 to be forward biased and D2 to be reverse biased. The equivalent circuit is shown in Figure 3(b)
In mode 3, *S1* is turned off and the switch *S2* is turned on which makes the diode D1 forward biased and D2 reverse biased. The equivalent circuit is shown in Figure 3(c).
During mode 4 both *S1* and *S2* are turned off which makes both the diodes *D1* and *D2* forward bias condition, and the corresponding equivalent circuit is shown in Figure 3(d)

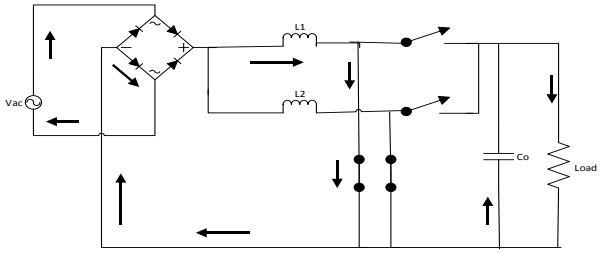

Fig. 3(a) Interleaved Boost Rectifier Mode 1 Operation

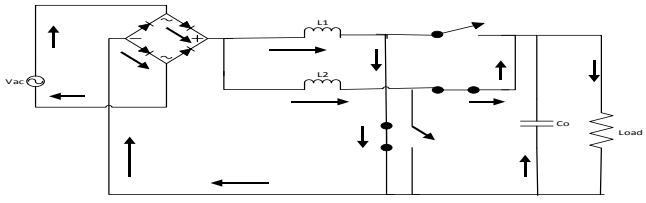

Fig. 3(b) Interleaved Boost Rectifier Mode 2 Operation

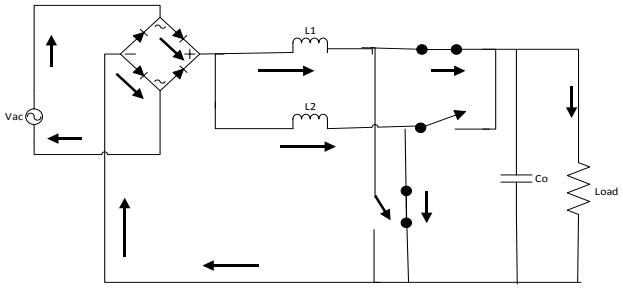

Fig. 3(c) Interleaved Boost Rectifier Mode 3 Operation

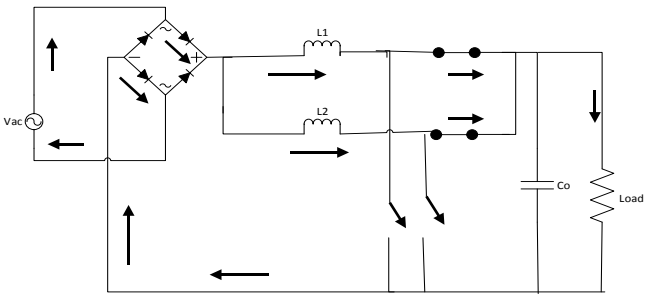

Fig. 3(d) Interleaved Boost Rectifier Mode 4 Operation

2.3Bridgeless Interleaved boost Rectifier

The operation can be divided in to two modes. In mode 1, S1 and S2 are turned on at the same instant during positive half cycle of supply voltage. the current flows through L1, S_1, $S_2$and L2 thereby storing energy in L1 and L2. When S_1 and S_2 are turned off, the energy stored in L1 and L2 are released as current through D1, load, body diode of S_2 and is fed back to the mains.
During mode 2, S3 and S4 are turned on at the same instant during negative half cycle of supply voltage which is 180˚ out of phase with respect to the instants of S_1 and S_2. S_3 and S_4 are turned ON and energy is stored in L3 and L4 via S_3 and S_4. During the negative half cycle, S_4 and S_2 are turned ON, energy gets stored in L2 and L1 for the first phase and L4 and L3 for the next phase and gets released as current which flows through D2 (D4), load, body diode of S_1 (S_3) and back to mains.

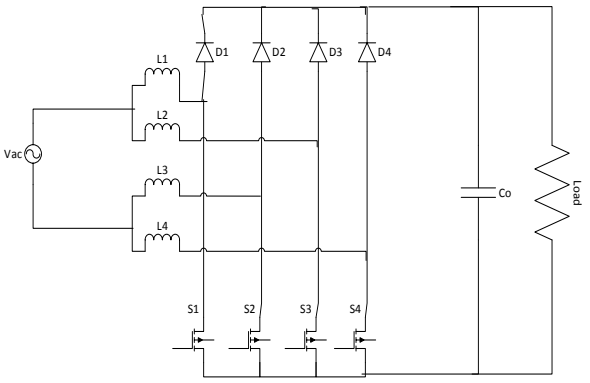

Fig. 4 Bridgeless Interleaved Boost Rectifier

3. Design procedure for BLIL

Each Bridgeless Boost Rectifier, IBC or BLIL involves boost converter in their design. Therefore, it is imperative that design equations of boost converter come to use here too.
It is generally found that IBC operates at maximum efficiency at a duty cycle of 50%. Also, boost converter needs to be operated at high frequencies for boosting operation. Switching frequency is taken to be 70 KHz. It is assumed that inductor ripple current and capacitor ripple voltage would be around 20-30 % of final current and voltage respectively.

Following calculations are made for a 100 W system.
Inductance value is calculated from:

$$L=\frac{Vin*(Vout-Vin)}{\Delta IL*fs*Vout} \quad (1)$$

From the inductance value we cn find out max current through switches by:

$$I_{s(max)}=\frac{\Delta IL}{2}+\frac{Io(max)}{2} \quad (2)$$

It is essential to find out max current through switch for the proper selection of switch with required rating.
Filter capacitance can then be found out by,

$$C_o=\frac{Io*D}{fs*\Delta Vout} \quad (3)$$

Table 1: gives the value of various parameters required and used.

Table1. Parameters Design Tabulation

S No	Parameter	Value
1.	Duty Cycle	50 %
2.	Switching Frequency	70 KHz
3.	Input Voltage	50 V
4.	Output Voltage	100 V
8.	L1, L2, L3, L4	200 µH
9.	Co	500 µF
15.	Efficiency	98 %

4. Simulation Analysis

4.1 Bridgeless Boost rectifier

Following fig 5(a) shows the MATLAB simulink model for bridgeless boost rectifier.

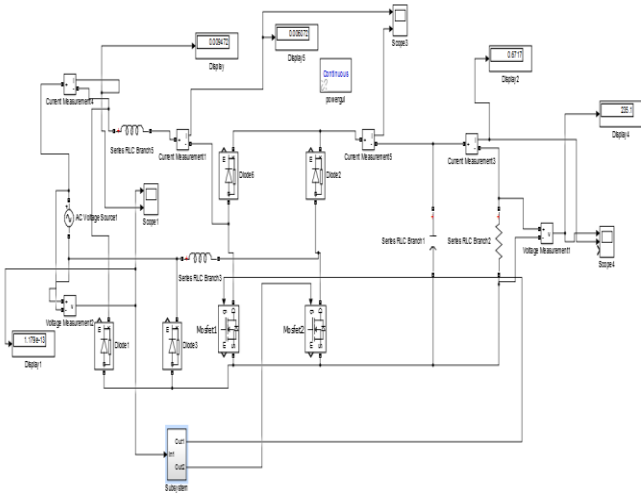

Fig. 5(a) Simulink model of Bridgeless boost rectifier
Simulation of the above model gives following results.

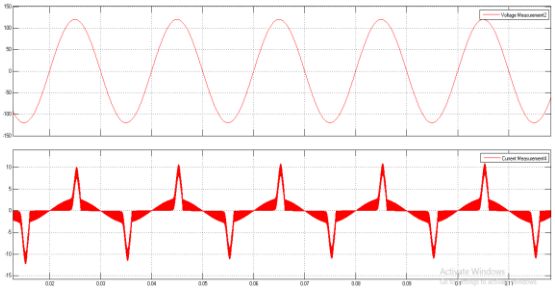

Fig. 5(b) Input Voltage and Input Current Waveforms

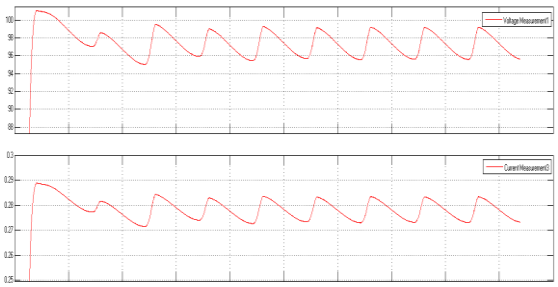

Fig. 5(c) Output Voltage and Output Current Waveforms

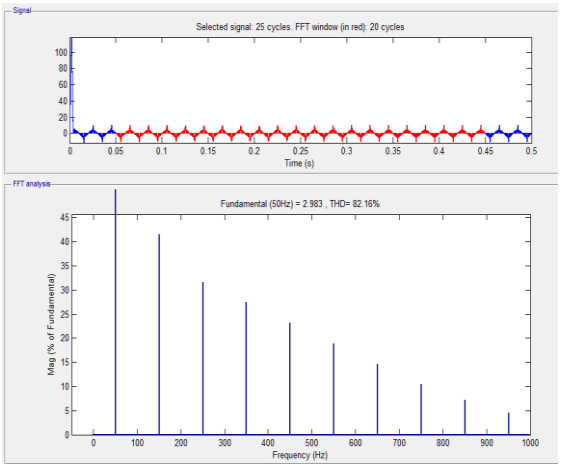

Fig. 5(d) THD Results of Bridgeless Boost Rectifier

Experimental results of bridgeless boost rectifier gives FFT analysis of the input current shows harmonic content of around 80%. This circuit, though being high in harmonic content exhibits various advantages like reduction in conduction losses, low dissipation of heat, increase in Power density etc.

4.2 Interleaved boost converter

Below fig 6(a) shows the MATLAB simulink model of IBC.

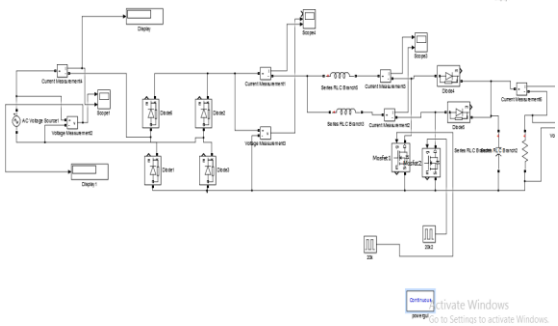

Fig. 6(a) Simulink model of interleaved boost rectifier

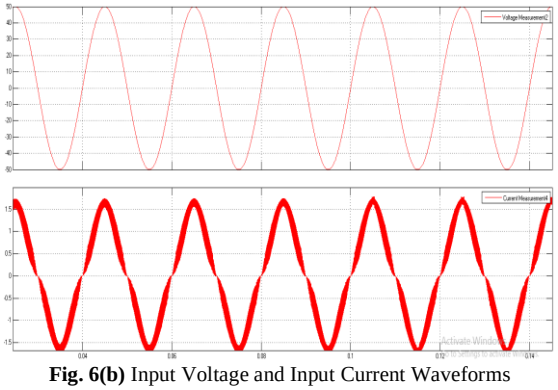

Fig. 6(b) Input Voltage and Input Current Waveforms

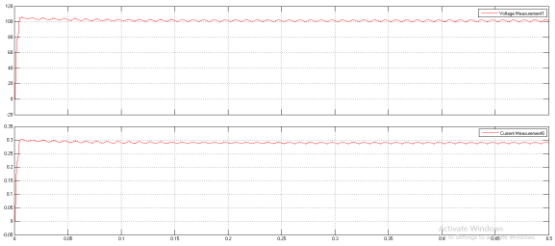

Fig. 6(c) Output Voltage and output current waveforms

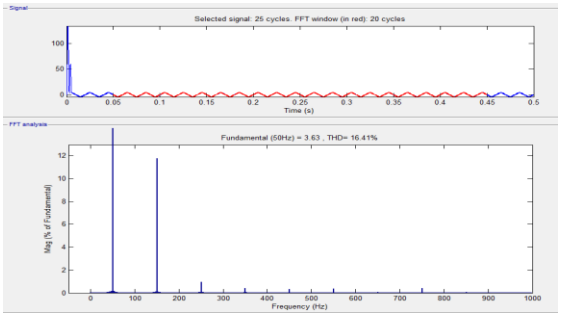

Fig. 6(d) THD results of Interleaved Boost Rectifier

Simulation results of IBC gives FFT analysis in which THD is around 12%. Input current also follows the input voltage. This is a significant improvement considering high THDs in the conventional boost rectifier circuit.

4.3 Bridgeless Interleaved Boost rectifier

Following fig 7(a) gives the simulink model of BLIL rectifier. The simulation results of BLIL rectifier shows us that the THD stands at only 9% with reduced conduction losses and improved system performance. Input current is almost sinusoidal and follows the sinusoid of voltage.

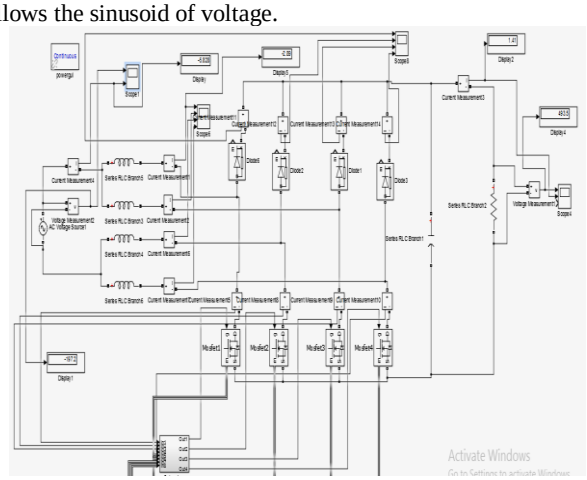

Fig. 7(a) Simulink Model of Bridgeless Interleaved Boost Rectifier

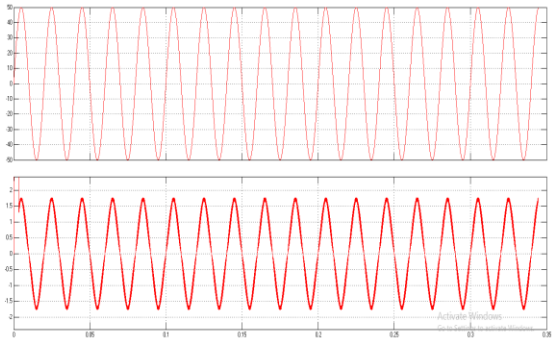

Fig. 7(b) Input Voltage and Input Current Waveforms

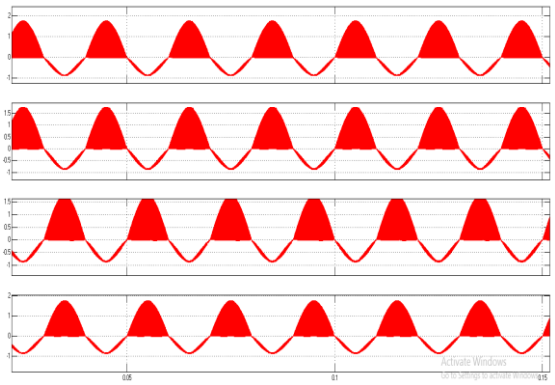

Fig. 7(c) Inductor Current Waveforms

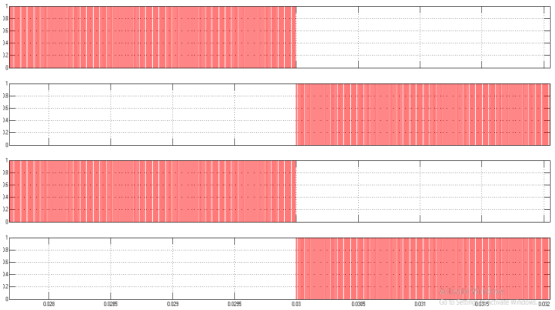

Fig. 7(d) Switching Pulses of Gates

Above Figure gives switching pulses of MOSFETs S1, S2, S3 and S4 from top to bottom. S1, S3 are 180^0 out of phase and S2, S4 are 180^0 out of phase. Switches turn on and off with a frequency of 70 KHz and duty cycle of 50%.

V Simulation Results

Table3. Simulation Results

Type of Design	Input Voltage (V)	Output Voltage (V)	Inductor Current (A)	THD (%)
Conventional Rectifier	50	49.8	-	172
Bridge Boost Rectifier	50	95.94	2.5	81
Bridgeless Boost Rectifier	50	96.87	1.8	75
Interleaved Boost Rectifier	50	100.8	1.8	16
Bridgeless Interleaved Boost Rectifier	50	98.7	1.8	9

One can observe from the table that as we go from conventional circuits to BLIL circuit THD has decreased manifolds from 172% to only 9%, which in any practical case is acceptable. Also, we need to note here that as the power level goes up, the efficiency increases, thus this system can become more and more efficient at higher power levels.

5. Conclusion

Through this project an objective of designing and developing an efficient and improved version of Bridgeless Interleaved Boost Rectifier has been achieved. We have observed that the BLIL circuit has reduced the harmonics and input considerably from around 150 % in conventional circuit to only 9% in BLIL circuit. Also, considering the size of filters usually used in the conventional circuit, the size of capacitor in BLIL is reduced by a

great margin which again reduces the cost, decreases the size of circuit and increases the density of power. This project also helped in understanding boost converters in various applications and the scope can be extended to both high power and low power circuits. It is to be noted here that these circuits are cost efficient for high power circuits only. For, low power circuits, these circuits may become expensive and the gains made through this circuit by improving power efficiency would be nullified in low power circuit due to high complexity of circuitry and deployment. The challenge lies in cost efficient circuits for even low power circuit and research has to proceed in that way from here on.

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