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Research paper

Design of a high-performance multiplier based on multiplexer

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Abstract

This paper presents a high-performance multiplier based on 4×1 multiplexer. The 4×1 multiplexer is defined as a combinational logic circuit. It is used to select one of four digital inputs (X) to introduce single output. Two-digit bits of the second group (Y) are used to control the multiplexer. This feature is used to design the proposed 8 - and 12- multipliers. The proposed multipliers are coded using the Verilog hardware description language (HDL). The coded 8×8-bit and 12×12-bit circuits were synthesized, simulated and verified using Quartus II and Modelsim 6.5 software systems. The designed multipliers are compared with the conventional multipliers based on frequency operation speed and the combinational adaptive look-up-tables (ALUTs). The comparison results show the proposed design circuits demonstrate the conventional multipliers in terms of operation-speed by 22.7% and 47%. They, also, reduced the combinational ALUTs by 50% and 52% for both multipliers.

Keywords: *HDL; FPGA; Multiplexer; Multiplier.*

1. Introduction

The rapid development of the electronic device systems and their applications in recent years made the high-speed arithmetic circuits are increasingly being demanded. The multiplier circuit is considered as a key element for multiple digital systems such as finite impulse response (FIR) filter [1], [2], telecommunication, and digital signal processing (DSP) systems [3]. Based on what has been explained, enhancing the multiplier speed, reducing the power consumption and optimizing the circuit area were always the designer's challenges. Multiple approaches and various techniques have been used to implement the multiplier circuit. An array multiplier as described earlier by Wallace in [4] is computing the partial results, shifting left and summiting together. The conventional multiplier in Fig. 1 consists of group of adders [5], to create the partial results.
A fixed width technique is used in [6-7] to generate a yield result with the same width as the input multiplier circuit. This method optimized the area dimension and reduced the power conception with minimum acceptable errors. A correction algorithm factor is added to the partial products in [8] for a more accurate result. Wallace technique was applied in [9], [10] and improved by [11], to reduce the size area and improve the performance of multiplication. A Vedic algorithm method [12] is used to provide fast mathematical operations. This method has been applied for designing multiplier in multiple techniques for high-speed operation [13], [14], and less delay time.
A novel method for designing the proposed 8x8- and 12×12-bit multiplier circuits based on 4×1 multiplexer is presented in this paper.

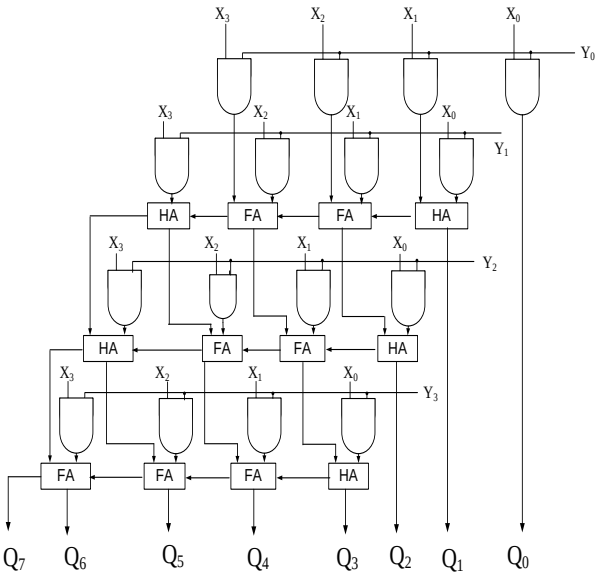

Fig. 1: Block Circuit Diagram of the Conventional Array Multiplier.

2. The designed multiplier architecture

The concept idea of the proposed design depends on utilizing the 4×1 multiplexer to develop the suggested circuit. It is realized that the multiplication number is created by a summation, the digital inputs (X) for all the logic 1 bits of the second group Y, taking into consideration the position of these digits 1 in the second group Y. The two-digit bits of Y-group notifies as a control selector, it is maybe 00, or 01, 10 and 11, as shown in Fig. 2.

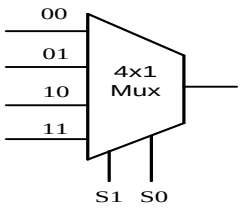

Fig. 2: 4×1 Multiplexer.

To implement this idea, a 4x1 multiplexer is a circuit that permits one of four cases (00, 01, 10, and 11) pass through it. In the case, if the control selector S_1S_0 is (00), all digit bits are zero at the multiplexer output. At the point when the S_1S_0 is (01), the selector allows the X digital values to pass through the multiplexer. In the meantime, when they are (10), the yield result is duplicated the X-digit values (multiplied by 2). The adding zero (0) to the least significant bit (LSB) of the X-number, may duplicate it. Finally, when the control selector S_1S_0 is (11), the outcome might be a summation of the X-number with its duplicate value. It is made by preparing a required adder for a summation of the X-number and its duplicate value.

2.1. 8×8 Multiplier design

To design the 8×8 multiplier circuit based on a 4×1 multiplexer, four units of the designed multiplexer and four binary parallel adders are required. The data inputs of the Y group (8-bits) are apportioned into four sets of 2-bit pairs and separately feeds to the four multiplexers as control selectors. The X digital values (as earlier clarified) are the multiplexer inputs.

To obtain the summation of 8-digit bits (X number) with its value, an additional bit (0) is needed as an LSB of the number. Due to that, 9-bit values are used as an adder input. The yield of the 10-bit adder at the multiplexer inputs compelled to organize the rest multiplexer inputs to be 10-bits. This can be made by adding the zero-bit as a most significant bit (MSB) to X-number. Regarding the bit position of the second multiplexers, two LSB digit bits (00) are expected to add to the output values of the second multiplexer (as described in Fig. 3). The same way is utilized to whatever remains of the third and fourth multiplexer individually. In addition to that, another four zero bits (0000) is added at the output of the second adder in order to obtain the desired 16-bit. The block circuit diagram of the proposed design multiplier is shown in Fig. 3.

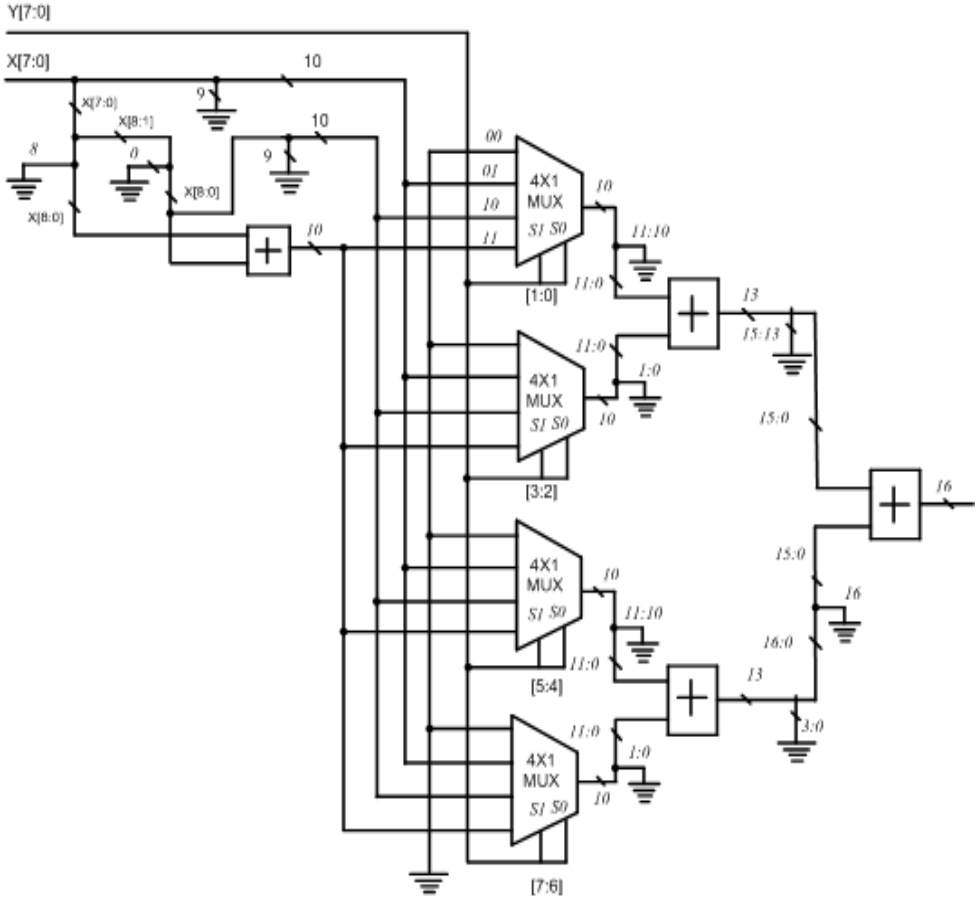

Fig. 3: Block Circuit Diagram of 8×8 Multiplier-Based Multiplexers.

2.2. 12×12 Multiplier design

The 12-bit multiplier circuit is composed in the same manner as the 8-bit multiplier built. The 12-bit is partitioned to six sets of two-digit bits, in this way, a six 4×1 multiplexer with 14-bit inputs are required to implement the desired 12-bit multiplier circuit. Notwithstanding the required three binary adders that use for summation the six multiplexer outputs, one more adder is needed to complete the summation process.

3. Results and discussion

The proposed design multipliers including the multiplexers and adder design circuits are coded in Verilog HDL code. Then, these codes are compiled in ALTERA Quartus II software system with Stratix III FPGA kit board. The prosed design codes are simulated with ModelSim 6.5 software to verify the functionality of the design. The software report described the 8×8 design circuit constructs with 83 ALUTs and 43 Adaptive logic modules (ALMs), whereas 198 ALUTs and 82 ALMs needs to construct 12×12-bit multipliers. The simulation results of the presented 8-and 12-bit multipliers are

shown in Fig. 4 (a, and b). The figure demonstrates the accomplished output results of the design circuits in regards to the given input numbers are matched with the achieved mathematical results. In addition to the showed X and Y-input values in Fig. 4 (a and b), also, the field (D) is shown in the figures. Consequently, it shows up the summation of X-digit inputs with its value, which can be accomplished by adding one more zero as an LSB bit.

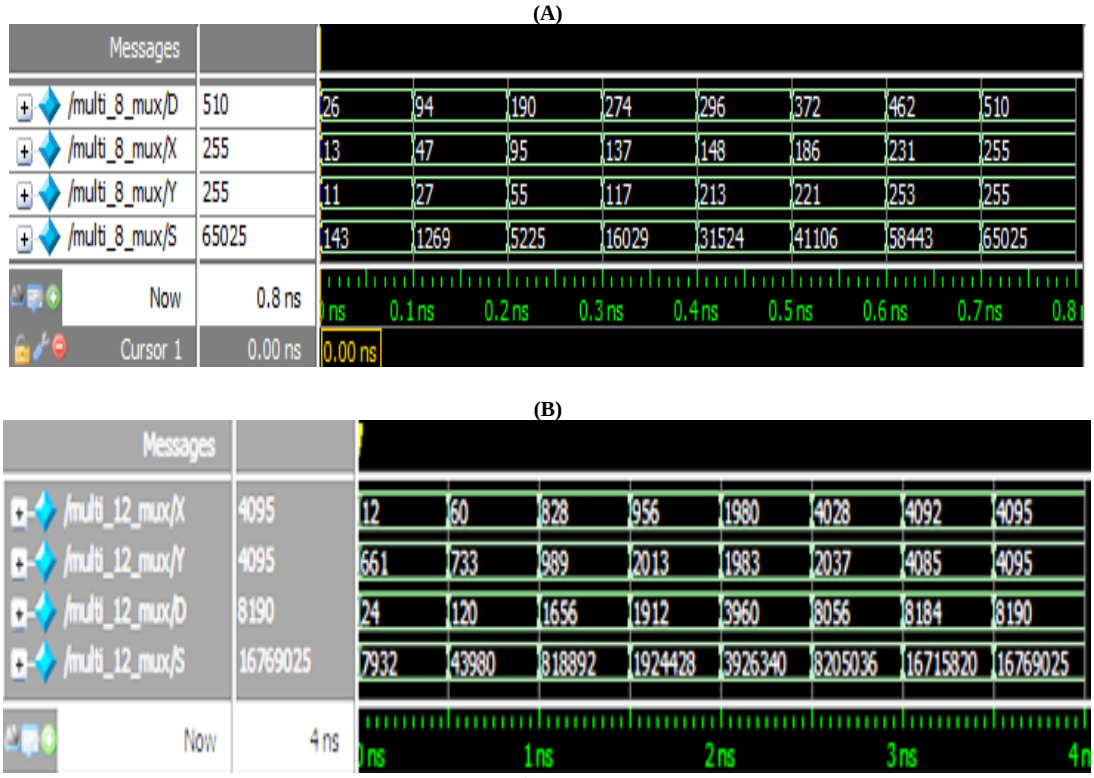

Fig. 4: The Simulation Results of A) 8×8, B) 12×12 Multiplier Circuits.

Table 1: Comparison between the Conventional and the Proposed Design Multipliers

Multiplier	8×8		12×12	
	Conventional	Proposed	Conventional	Proposed
Maximum Operation Frequency (MHz)	248.69	321.75	110.49	208.94
Combinational ALUTs cells & Adaptive logic modules (ALMs)	165 + 84	83 +43	416 + 213	198 +82

To compare the proposed 8 -, and 12-bit design circuits with the conventional multipliers, an 8 -, and 12-bit of both proposed and conventional multiplier circuits had been coded Verilog HDL code, synthesized, elaborated and compiled using ALTERA Quartus II software system with Stratix III FPGA kit board. The proposed multiplier circuits operate with 321.75 and 208.94 MHz for 8 -, and 12-bit multipliers respectively.

A comparison between the proposed design and the conventional multipliers in the term of the frequency operating speed and combinational (ALUTs) cells is shown in Table 1.

The achieved result of the proposed design in Table 1 outperforms the conventional multipliers for higher operating frequency and lower combinational (ALUTs) cells. The proposed design provides a capability to simultaneously insert the digital data to the multiplexers. This operation reduces the critical path delay and so enhances the operation speed of the circuit. Table 1 describes that the frequency operating speed of the proposed design circuits are relatively increased proportionally with increasing the bit multiplier circuits for 8-, and 12-bit multipliers.

4. Conclusion

A novel multiplier design circuit based on 4x1 multiplexer is presented in this paper. The designed multiplier circuits of an 8 - and 12-bit are achieved by employing the 4x1 multiplexer. The multiplicand number was generated by a summation of X digit bits with all the logic 1 bits of Y digit bits. The designed circuit of the 4×1 multiplexer is used to architect the 8- and 12-bit multipliers. The project circuits were coded, synthesized using Quartus II, and simulated with Modelsim software. The designed multiplier outperforms the conventional circuits in the term of operating speed by 22.7% and 47% improvement speed. They, also, achieved a reduction of 50% and 52% of ALUTs cells for the 8 -, and 12-bit multipliers respectively. The mentioned advantages of operating speed and ALUTs reductions make the designed multipliers more attractive for applications in the digital circuits and systems.

References

[1] B. S. Hasan, and A. Yakovlev, "Improved parameterized efficient FPGA implementations of parallel 1-D filtering algorithms using Xilinx System Generator," presented at the Signal Processing and Information Technology (ISSPIT), Luxor, Egypt, 2010. https://doi.org/10.1109/ISSPIT.2010.5711807.

[2] S. B. S. Hasan, and A. Yakovlev, "Parameterized FPGA-based architecture for parallel 1-D filtering algorithms," in *International Workshop on Systems, Signal Processing, and their Applications, WOSSPA*, Tipaza, Algeria, 2011, pp. 171 - 174. https://doi.org/10.1109/WOSSPA.2011.5931443.

[3] N. T. Y. S. S. J. Sami Hasan, "Single-Camera Computer Vision Algorithm for Robot Shortest Path Estimator using morphologicalstructuring element with variable sizes," *International Journal Of Engineering & Technology*, vol. 7, pp. 248-254, 2018. https://www.sciencepubco.com/index.php/ijet/article/view/12937/5171.

[4] C. S. Wallace, "A Suggestion for a Fast Multiplier," *IEEE Transactions on Electronic Computers* vol. 13, p. 4, 1964. https://doi.org/10.1109/PGEC.1964.263830.

[5] T. G. P. Yogesh M. Motey "Traditional and Truncation schemes for Different Multiplier," *International Journal of Electronics and Computer Science Engineering*, vol. 2, p. 7, 2013. https://pdfs.semanticscholar.org/ce51/6dd0acac62ed34c13eb3673bea17e32717a6.pdf.

[6] C.-N. K. Jinn-Shyan Wang, Tsung-Han Yang, "Low-Power Fixed-Width Array Multipliers," presented at the ISLPED'04, Newport Beach, California, USA, 2004. DOI: 10.1109/LPE.2004.241092.

[7] W.-Q. H. Y.-H. C. S.-J. Jou, "High-Accuracy Fixed-Width Booth Multipliers Based on Probability and Simulation," *IEEE Journals & Magazines*, vol. 8, pp. 2052 - 2061, 2015. https://doi.org/10.1109/TCSI.2015.2440731.

[8] S. S. W. a. W. S. F. L. D. Van, "Design of the lower-error fixedwidth multiplier and its application " *IEEE Trans. Circuits Syst. II*, vol. 47, Oct. 2000. https://doi.org/10.1109/82.877155.

[9] S. A. a. Y. Kong, "Low-Area Wallace Multiplier," *Hindawi Publishing Corporation \ VLSI Design*, p. 6 pages, 2014. http://downloads.hindawi.com/journals/vlsi/2014/343960.pdf.

[10] K. C. Anannya Maiti, Razia Sultana, Santanu Maity, "Design and implementation of 4-bit Vedic Multiplier," *International Journal of Emerging Trends in Science and Technology (IJETST)*, vol. 3, pp. 3865-3868, 2016. https://doi.org/10.18535/ijetst/v3i05.06.

[11] T. U. Tongxin Yang, Toshinori Sato., "Low-Power and High-Speed Approximate Multiplier Design with a Tree Compressor," presented at the 2017 IEEE 35th International Conference on Computer Design, Boston, MA, USA, 2017. https://doi.org/10.1109/ICCD.2017.22.

[12] S. C. Koyel Dey, "Design of High Performance 8 bit Binary Multiplier using Vedic Multiplication Algorithm with 16 nm technology," in *2017 1st International Conference on Electronics, Materials Engineering and Nano-Technology (IEMENTech)*, Kolkata, India, 2017, pp. 1-5. https://doi.org/10.1109/IEMENTECH.2017.8076956.

[13] K. N. P. K. H. Y. C. S. M. Visvesvaraya, "Design and implementation of high efficiency vedic binary multiplier circuit based on squaring circuits" presented at the 2017 2nd IEEE International Conference on Recent Trends in Electronics, Information & Communication Technology (RTEICT), Bangalore, India, pp 873 - 977. https://doi.org/10.1109/RTEICT.2017.8256743.

[14] R. K. T. Haniotakis, "Power-delay-area efficient design of vedic multiplier using adaptable manchester carry chain adder," presented at the 2017 International Conference on Communication and Signal Processing (ICCSP), India, pp. 1418 - 1422, 2017. https://doi.org/10.1109/ICCSP.2017.8286618.