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Research paper

Implementation of Full Adder Using 5-Input Majority Gate

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Abstract

In this paper full adder was created employing five-input majority gate according to Quantum-Dot Cellular Automata (QCA) innovation. We used the QCA logic in our modified structure to reduce the delay. That report details the structure furthermore investigate associated with QCA dependent 1-bit full adder design for minimal energy purposes. This method permits decreasing energy expenditure, delay, additionally location involving electronic circuits.

Keywords: Full-Adder, Five-Input Majority Gate, Energy Efficient, Verification.

1. Introduction

Low-power and efficient technologies are the prime concerns for very-large-scale integration (VLSI) system creators. In addition, high-speed full adders with low power consumption have undeniably turned out to be stand-outs among the most crucial components of a processor because they are generally utilized in the arithmetic logic unit. Another consideration in the design of a low-power area-effective full adder structure is the delay that influences the general execution of the circuit. Extensive improvements in the field of compact systems and cellular networks have escalated research efforts in low-power microelectronics. In VLSI implementation, the significant issues are heat dissemination and power utilization. In order to manage among regarding concerns, it is essential to decrease the power provide voltage, changing frequency, and capacitance of the transistor. Area, delay, and energy dispersion have surfaced as the priceless problems for designers [1, 2].

2. QCA Preliminaries

QCA is a promising successor to CMOS technology. QCA offers the unique approach to the transistor worldview. QCA, projected by Lent et al., is a developing innovation that provides an imaginative method of processing on the nano-scale through keeping track of the place of a single electron. This innovation permits the execution concerning logic products utilizing quantum dots as an alternative of transistors or diodes. The fundamental component of QCA is the quantum cell [3, 4].

Commonly, every QCA cell covers four electron wells as well as two electrons. The electron wells are held at a low potential and are coupled to each other by tunnel junctions. A high-level diagram of a four-dot QCA cell shows up in Fig. 1(a). Four quantum dots are placed in order to create a block. The dots are combined by using quantum technical tunneling boundaries and also electrons could tunnel by using all of them based on the state of the method. Majority gate is essential building parts of this technology. The function of the five-input majority gate is to generate five inputs and eventually to get desired output as illustrates in Fig. 1(b) [5].

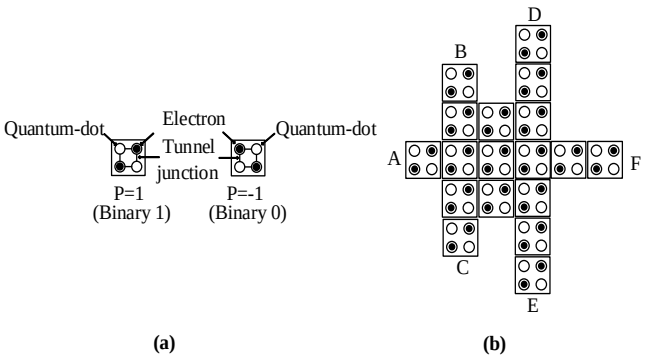

Figure 1:. (a) QCA cells with two different polarizations, (b) Five-input majority gate.

3. Proposed Structure

This part describes the recommended layout around the 1-bit full adder based on five input majority-gate. A new highly area efficient coplanar QCA full adder design is proposed. To develop our enhanced full adder, we have used five-input majority gate [6] and inverter gates. The schematic drawing as well as QCA execution regarding suggested full adder structure as shown in Fig. 2(a), and Fig. 2(b), correspondingly.

The proposed QCA full adder utilizes traditional QCA cells. The use of a compact 5-input majority gate [6] benefits inside a design which a great deal less complicated compared to layouts which use just 3-input majority gates additionally inverters. This layout includes extended vertical wires that might possibly outcome in undependable signal beliefs. The structure is constructed of the regular cell. By the standard, all input cells are placed on one side, the outputs are placed on another side. It helps to actualize the proposed design to combinational QCA designs, such as arithmetic and logic unit architecture. The structure is occupied by 0.05 µm2 total area with low complexity. In this design, single layer wire crossing which is based on QCA clocking is used. It can lead to the compact circuit and realization of the design in complex circuit architecture can be more proper.

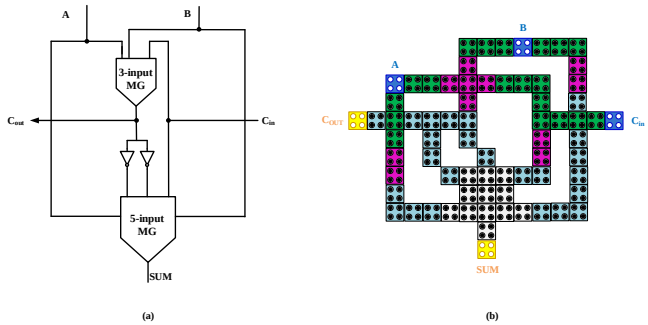

Figure 2. Proposed full adder: (a) The circuit diagram, (b) QCA Representation.

4. Simulation Results and Comparison Analysis

In this section, we evaluate and compare the presented QCA structure for the full adder so far, in terms of structural aspect to select the best design for leveraging in our proposed adder structure. It is worth noticing that all the cells are implemented in a single layer, so it is easy to access the cells with no additional layers in the design. In addition, proposed method shows a high performance in terms of cell count and latency in comparison to other conventional methods [5, 6]. The functionality verification simulation is performed utilizing QCADesigner as shown in Fig. 3.

Figure 3. Simulation result for proposed full adder.

A comparison between proposed full adder and existing full adder designs is illustrated in Table 1. Our design gains 36% and 23%improvement in cell count and consumes same area in comparison to the best single layer designs [5, 6].

Table 1. Complexity comparison of the proposed full adder.

Circuit	Complexity (cell count)	Area (μm²)	Delay (clock cycle)	Cross-wiring	Overall Cost ($A * T^2$)
[5]	111	0.13	2.75	Yes	0.9831
[6]	93	0.09	1.25	Yes	0.1406
Proposed	**71**	**0.05**	**1.00**	**No**	**0.05**

5. Conclusion

This paper presents area productive outline of 1-bit full adder circuits based in QCA nanotechnology. The area enhancement has been accomplished by using efficient and compact 5-input majority gate. The proposed configuration significantly decreases the quantity of cells and uses a more compact region in compare through previous designs.

Acknowledgment

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References

[1] J. C. Jeon, 7-Input Majority Gate Based Priority Encoder Using Multi-Layer Quantum-Dot Cellular Automata, Advanced Science Letters. 23 (2017), 10118-10122.
[2] N. Safoev and J.C. Jeon, Compact RCA Based on Multilayer Quantum-dot Cellular Automata, Information Systems Design and Intelligent Applications, Springer. (2018), 515-524.
[3] J. C. Jeon and K. Y. Yoo, Elliptic Curve based Hardware Architecture using Cellular Automata, Mathematics and Computers in Simulation, 79 (2008), 1197-1203.
[4] J. C. Jeon, Low Hardware Complexity QCA Decoding Architecture Using Inverter Chain, International Journal of Control and Automation, 9 (2016), 347-358.
[5] R. Akeela and M. D. Wagh, A Five-input Majority Gate in Quantum-dot Cellular Automata, NSTI-Nanotech. 2 (2011), 13-16.
[6] D. Abedi, G. Jaberipur, and M. Sangsefidi, Coplanar Full Adder in Quantum-Dot Cellular Automata via Clock-Zone-Based Crossover, IEEE Transactions on Nanotechnology, 14 (2015), 497-504.
[7] S. Angizi1, E. Alkaldy, N. Bagherzadeh and K. Navi, Novel Robust Single Layer Wire Crossing Approach For Exclusive or Sum of Products Logic Design With Quantum-Dot Cellular Automata, Journal of Low Power Electronics, 10 (2014), 259–271.