International Journal of Engineering &Technology, 7 (3.29) (2018) 80-87

International Journal of Engineering & Technology

Website: www.sciencepubco.com/index.php/IJET

Research paper

Novel Design of Multiplexer and Demultiplexer using Reversible Logic Gates

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Abstract

Reversibility is the prominent technology in the recent era. In reversible logic the number output lines are equal to the number of input lines. In reversible logic the inputs are to be retrieved from the outputs. Reversible logic gates are user defined gates. Reversible logic owns its applications in various fields which include low power VLSI. In this paper multiplexer is implemented using QCA, SAM and both QCA & SAM gates. Also demultiplexer is implemented using two new reversible logic gates RAMESH and RAMESH-1 gates. These designs are simulated and synthesized using Xilinx ISE 12.1 and Mentor Graphics tool. The result shows that the proposed designs are more efficient in terms of gate count, quantum cost and power consumption.

Keywords: *Reversible Logic Gates, Multiplexer, Demultiplexer, Quantum Cost, VLSI.*

1. Introduction

Digital circuits are designed using two types of logic gates i.e. irreversible (conventional) and reversible logic gates. In irreversible (conventional) circuit synthesis starts with a universal or basic gates and some specification of a Boolean function. The disadvantages of irreversible logic are it dissipates more power and also it requires more number of transistors. Irreversible logic gates cannot implement the input from the output but in reversible logic gates input can be get from the output. In irreversible logic gates to get the input from the output additional circuitry is needed which increases the number of transistors and also increases the circuit complexity. The system to be reversible there are two conditions to be satisfied. The number of input lines must be equal to the number of output lines and feedback is not allowed & fan-out must be one. The performance of the system is improved if the system dissipates less amount of power.

2. Literature Survey

S. Rambabu, designed different type's combinational circuits such as multiplexer, demultiplexer, adder, and subtractors using reversible logic gates. These designs reduced the power consumption and delay [1]. K. Dipak Kumar and Jhuma Dutta et.al, implemented multiplexer and demultiplexer circuits using FREDKIN reversible logic gate. These designs reduced the gate count, garbage outputs, and quantum cost [2]. H. Rohini and S.Rajashekar, implemented combinational logic circuits like encoder, multiplexer etc., using reversible logic gates to minimize the quantum cost, garbage outputs, garbage inputs, and gate count [3]. A.M Chabi and Arman Roohi et.al, designed QCA reversible logic gate and implemented XOR gate and 2:1 multiplexer. These designs achieved less area and power consumption [4].

Neha Pannu and Neelam Rup Prakash, implemented multiplexer using FREDKIN reversible logic gate. The design was simulated by using Mentor Graphics tool. These designs reduced the gate count, garbage outputs, and quantum cost [5]. S. Mamataj and B. das et.al, implemented multiplexers using a COG reversible logic gate. These designs were simulated and synthesized by using Xilinx and Spartan3E FPGA [6]. Linen Gopal and Nikhil Raj et.al, implemented multiplexer and demultiplexer circuits using R-1 and R-2 reversible logic gates. These designs achieved that different parameters like garbage outputs, delay, and quantum cost were reduced [7]. Rakshith Saligram and Shrihari Shridhar Hegde et.al, designed a fault tolerant reversible multiplexer based multi-Boolean function generator using parity preserving gates. This design generated 16 different Boolean functions [8].

Sumit Gugnani and Arvind kumar, designed 2:1 multiplexer and demultiplexer using FREDKIN, BJN, Peres and a new gates. The designs reduced the power consumption [9]. Md. Selim Al Mamun and David Menville, implemented sequential circuits using SAM reversible logic gate. These designs minimized the quantum cost, garbage outputs, garbage inputs, and gate count [10]. Arijit Roy, Dibyendu Chatterjee et.al, described the behavioral description and synthesis of quantum multiplexer circuits [11]. Himanshu Thapliyal and Srinivas implemented 2:1 multiplexer using 3x3 TKS reversible logic gate. Further half adder and full adder designed using 2:1 multiplexer [12].

In this work three multiplexer designs are implemented using two reversible logic gates QCA [4], SAM [10] and combination of both the gates. Also demultiplexer is implemented using two new reversible logic gates RAMESH and RAMESH-1.

3. Reversible Logic Gates

3.1 QCA Gate [4]

The full form of QCA gate is Quantum-dot Cellular Automata gate. The block diagram of 3*3 QCA reversible logic gate is shown in figure 1. It is a reversible 3*3 gate maps inputs (A, B, C) to outputs (P=A, Q=A⊕B⊕C, R=$\bar{A}$B⊕AC).

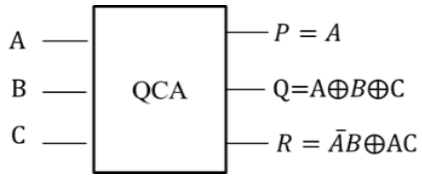

Figure 1: Block Diagram of 3*3 QCA Reversible Logic Gate.

3.2 SAM Gate [10]

The full form of SAM gate is Selim-Al-Mamun gate. The block diagram of 3*3 SAM reversible logic gate is shown in figure 2. It is a reversible 3*3 gate maps inputs (A, B, C) to outputs P= $\bar{A}$, Q=$\bar{A}$B⊕ A$\bar{C}$, R=$\bar{A}$C. The quantum cost of SAM gate is 4.

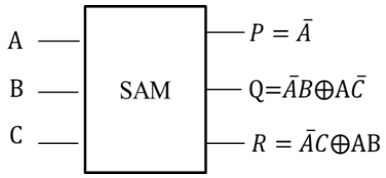

Figure 2: Block Diagram of 3*3 SAM Reversible Logic Gate.

3.3 Ramesh Gate

The block diagram of a 3*3 RAMESH reversible logic gate is shown in figure 3. It is a reversible 3*3 gate inputs (A, B, C) to outputs (P=A⊕BC, Q=B, R=A⊕$\bar{B}$C).

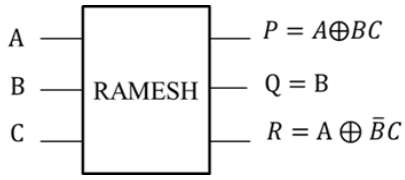

Figure 3: Block Diagram of 3*3 RAMESH Reversible Logic Gate.

3.4 RAMESH-1 Gate

The block diagram of a 3*3 RAMESH-1 reversible logic gate is shown in figure 4. It is a reversible 3*3 gate maps inputs (A, B, C) to outputs (P=AB⊕C, Q=$\bar{A}$B⊕C, R=A).

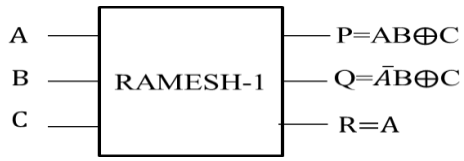

Figure 4: Block Diagram of 3*3 RAMESH-1 Reversible Logic Gate.

4. Proposed work

The multiplexer is implemented in three designs. Design-I using QCA gate, design-II using SAM gate and design-III using both QCA and SAM gates. The demultiplexer is constructed in two designs. Design-I using RAMESH gate and Design-II using RAMESH-1 gate.

4.1 Multiplexer Designs

4.1.1 Design-I using QCA Gate

The 2:1, 4:1, 8:1, and 16:1 multiplexers are implemented using QCA gate. The 2:1 multiplexer realization using QCA gate is shown in figure 5.

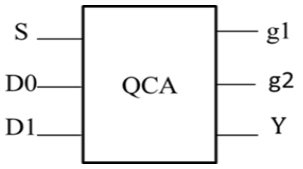

Figure 5: Block Diagram of 2:1 Multiplexer using QCA Reversible Logic Gate.

The block diagram of 4:1 multiplexer using 3*3 QCA reversible logic gate is shown in figure 6. D0, D1, D2, and D3 are inputs to the two QCA reversible logic gates. S0 and S1 are the select lines used to select the data inputs. The number of garbage outputs is represented as g1, g2, g3, g4, and g5. In the first stage there are two QCA reversible logic gates followed by one in the second stage. QCA gate is 3*3 reversible logic gate the inputs are assigned according to the ascending order of the data inputs while the 1st input of each QCA reversible logic gate is assigned with select line S0 in the first stage. The total number of QCA reversible logic gates is three (N-1 where N is the number of data inputs).

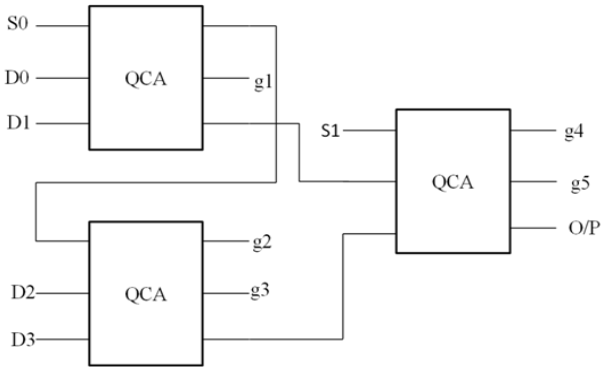

Figure 6: Block Diagram of 4:1 Multiplexer using QCA Reversible Logic Gate.

In the second stage the 1st input of QCA reversible logic gate is S1 and 2nd, 3rd inputs of QCA gate are 3rd output of QCA gates of the previous stage (1st input S1 and 2nd input is 3rd output of first QCA reversible logic gate in the previous stage and 3rd input is 3rd output of second QCA reversible logic gate in the previous stage). The number of gates required for this design is N-1 where N is number of inputs to the multiplexer. The design process is same for 8:1 and16:1 multiplexers respectively. The block diagram of 8:1 and 16:1 multiplexer using QCA gate are shown in figures 7 and 8 respectively.

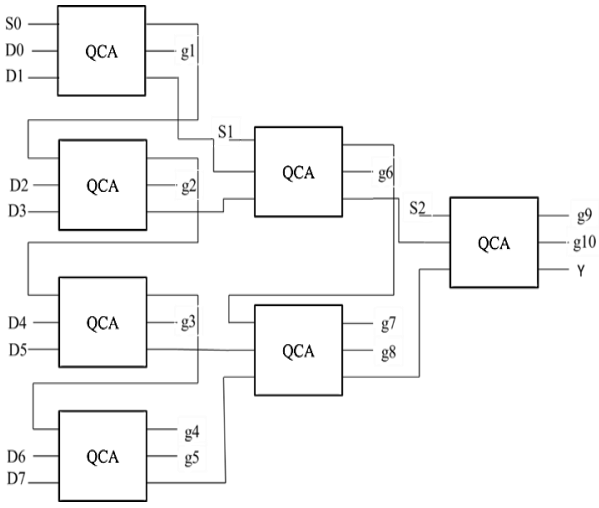

Figure 7: Block Diagram of 8:1 Multiplexer using QCA Reversible Logic Gate.

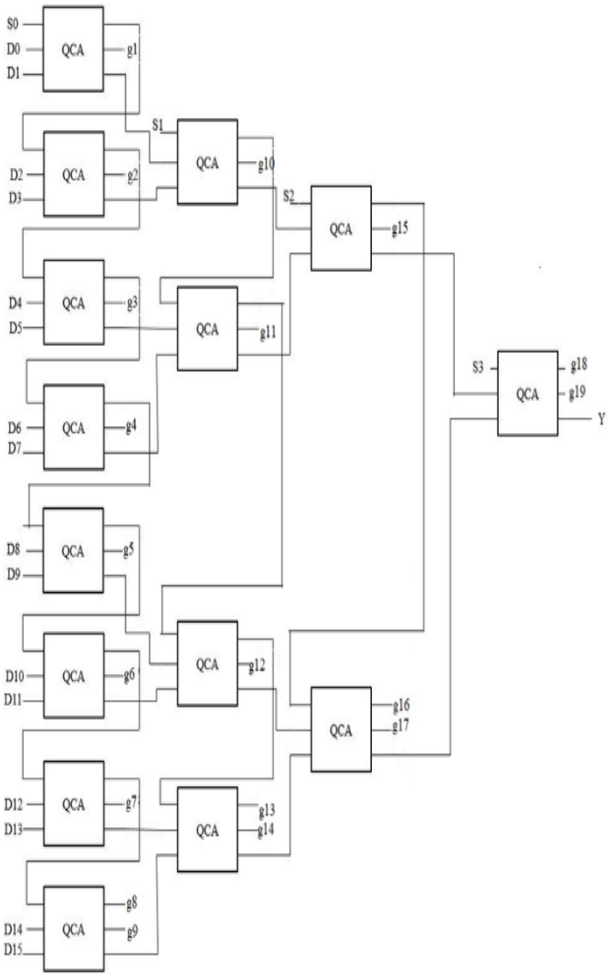

Figure 8: Block Diagram of 16:1 Multiplexer using QCA Reversible Logic Gate.

4.1.2 Design-II using SAM Gate

The 2:1, 4:1, 8:1, and 16:1 multiplexers are implemented using SAM gate. The 2:1 multiplexer realization using SAM gate is shown in figure 9.

Figure 9: Block Diagram of 2:1 Multiplexer using SAM Reversible Logic Gate.

The block diagram of 4:1multiplexer using 3*3 SAM reversible logic gate is shown in figure 10. The number of garbage outputs is represented as g1, g2, g3, g4, and g5. Garbage inputs are represented by logical zero. The quantum cost is 12.

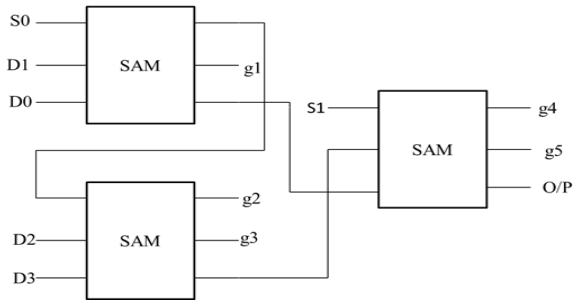

Figure 10: Block Diagram of 4:1 Multiplexer using SAM Reversible Logic Gate.

D0, D1, D2, and D3 are inputs to the SAM reversible logic gate. S0 and S1 are the select lines used to select the data inputs. The 1st input of each SAM reversible logic gate is assigned with S0 and $\overline{S}_0$ respectively, 2nd and 3rd are D1 and D0 for first SAM gate, D2 and D3 for second SAM gate in the first stage. In the first stage there are two SAM reversible logic gates followed by one in the second stage. In the second stage the 1st input of SAM reversible logic gate is S1 and 2nd, 3rd inputs of SAM reversible logic gate are 3rd output of SAM reversible logic gate of the previous stage (1st input S1 and 2nd input is 3rd output of first SAM reversible logic gate in the previous stage and 3rd input is 3rd output of second SAM reversible logic gate in the previous stage). The total number of SAM reversible logic gates is three (N-1 where N is the number of data inputs).The design process is same for 8:1 and 16:1 multiplexers respectively. The block diagram of 8:1 and 16:1 multiplexer using SAM gate are shown in figures 11 and 12 respectively.

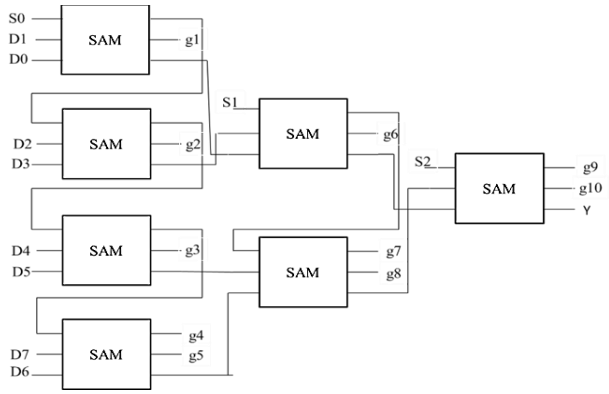

Figure 11: Block Diagram of 8:1 Multiplexer using SAM Reversible Logic Gate.

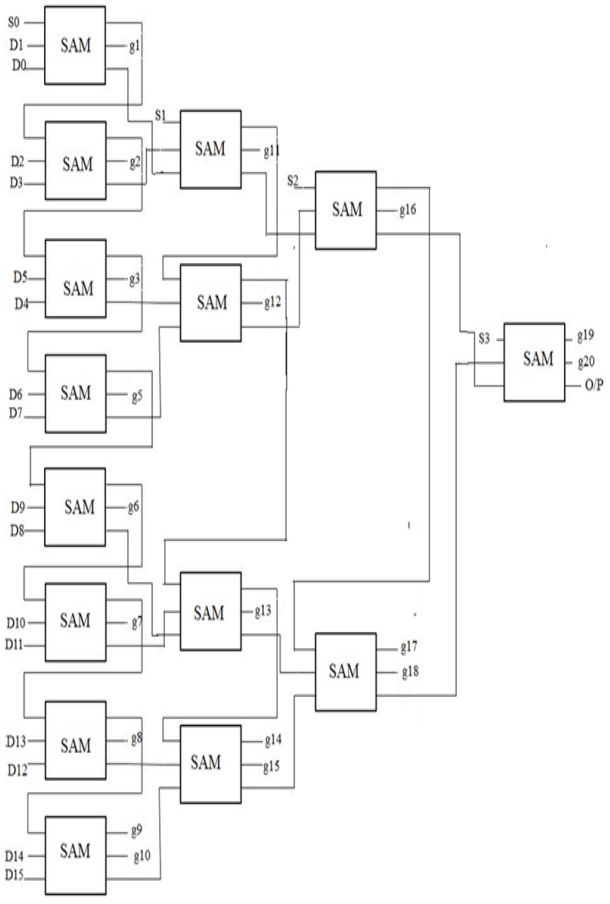

Figure 12: Block Diagram of 16:1 Multiplexer using SAM Reversible Logic Gate.

4.1.3 Design-III using QCA and SAM Gates

The 4:1 multiplexer realization using QCA and SAM gates are shown in figure 13. D0 and D1 are inputs to the QCA reversible logic gate, D3 and D2 are inputs to the first SAM reversible logic gate. S0, S1 are the select lines used to select the data inputs. In the first stage, one QCA reversible logic gate and one SAM reversible logic gate followed by one SAM reversible logic gate in the second stage. In the first stage, the inputs to QCA reversible logic gate are assigned according to the ascending order of the data inputs (1st input is S0, 2nd and 3rd inputs are D0 and D1 respectively) and the inputs to SAM reversible logic gate are assigned according to the descending order of the data inputs (1st input is S0 which is the 1st output of QCA gate in the first stage, 2nd and 3rd inputs are D3 and D2 respectively). In the second stage the 1st input of SAM reversible logic gate is S1,2nd and 3rd inputs of SAM reversible logic gate is 3rd output of QCA and SAM gates of the previous stage (1st input S1, 2nd input is 3rd output of SAM reversible logic gate in the previous stage and 3rd input is 3rd output of QCA reversible logic gate in the previous stage). The total number of QCA and SAM reversible logic gates in this design is 3 (N-1 where N is the number of data inputs).The design process is same for 8:1 and16:1 multiplexers respectively. The block diagram of 8:1 and 16:1 multiplexers using QCA and SAM gates are shown in figures 14 and 15 respectively.

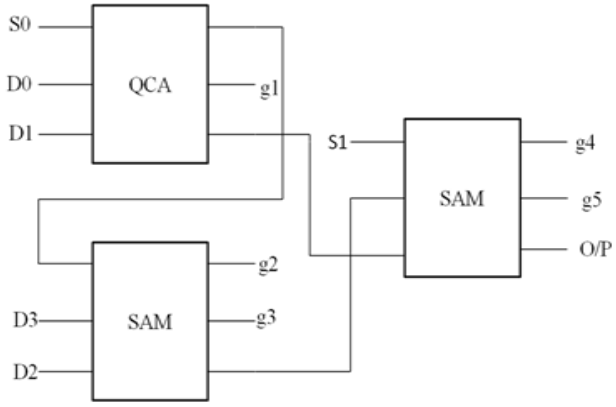

Figure 13: Block Diagram of 4:1 Multiplexer using QCA and SAM Reversible Logic Gates.

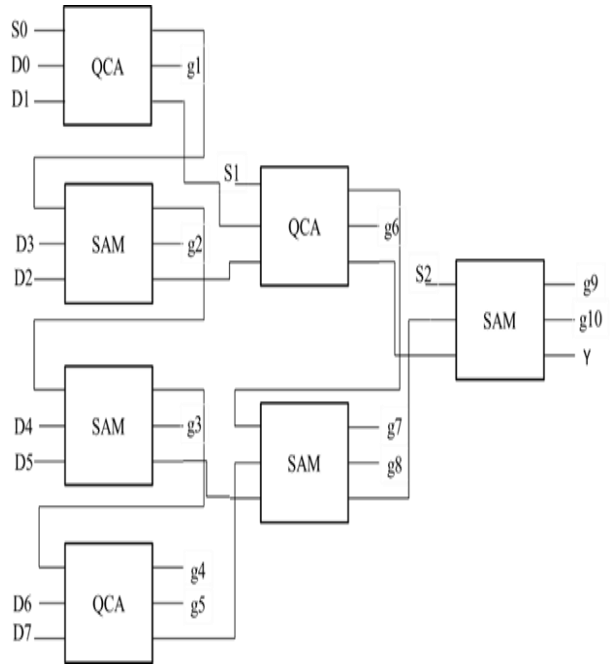

Figure 14: Block Diagram of 8:1 Multiplexer using QCA and SAM Reversible Logic Gates.

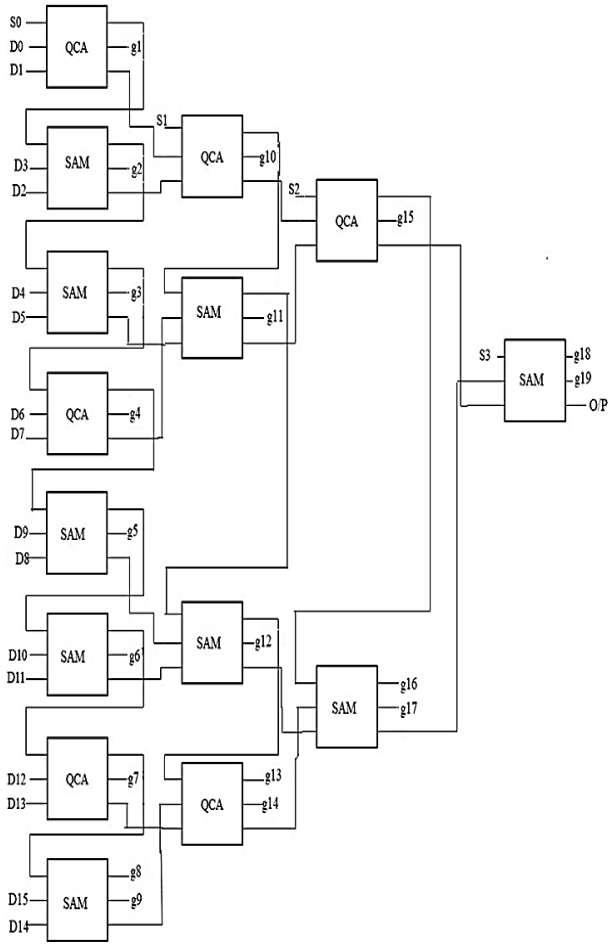

Figure 15: Block Diagram of 16:1 Multiplexer using QCA and SAM Reversible Logic Gates.

4.2 Demultiplexer Designs

4.2.1 Design-I using RAMESH Gate

The 1:2, 1:4, 1:8, and 1:16 demultiplexers are implemented using RAMESH gate. The 1:2 demultiplexer realization using RAMESH gate is shown in figure 16.

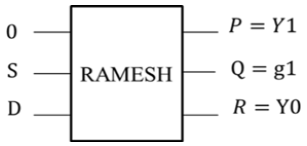

Figure 16: Block Diagram of 1:2 Demultiplexer using RAMESH Reversible Logic Gate.

The block diagram of 1:4 demultiplexer using 3*3 RAMESH reversible logic gate is shown in figure 17. It requires three RAMESH gates. The number of garbage outputs is represented as g1 and g2. Garbage inputs are represented by logical zero. Logic zero is 1st input to every RAMESH reversible logic gate. S0 and S1 are the select bits used to select the data inputs. In the first stage there is one RAMESH reversible logic gate followed by two in the second stage. In the first stage D is 3rd input to the RAMESH reversible logic gate and 2nd input is S0. In the second stage, the second input is S1 for each RAMESH reversible logic gate and 3rd input is 1st and 3rd outputs of previous stage RAMESH reversible logic gate (for the first RAMESH reversible logic gate 3rd input is 3rd output of previous stage RAMESH reversible logic gate for the second RAMESH reversible logic gate 3rd input is 1st output of previous stage RAMESH reversible logic gate). The outputs of the demultiplexer are stored at P and R

outputs of each RAMESH reversible logic gate. The design process is same for 1:8 and 1:16 demultiplexers respectively. The block diagram of 1:8 and 1:16 demultiplexer using RAMESH gate are shown in figures 18 and 19 respectively.

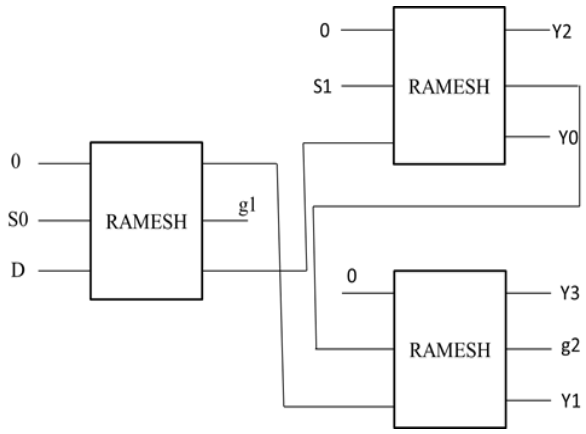

Figure 17: Block Diagram of 1:4 Demultiplexer using RAMESH Reversible Logic Gate.

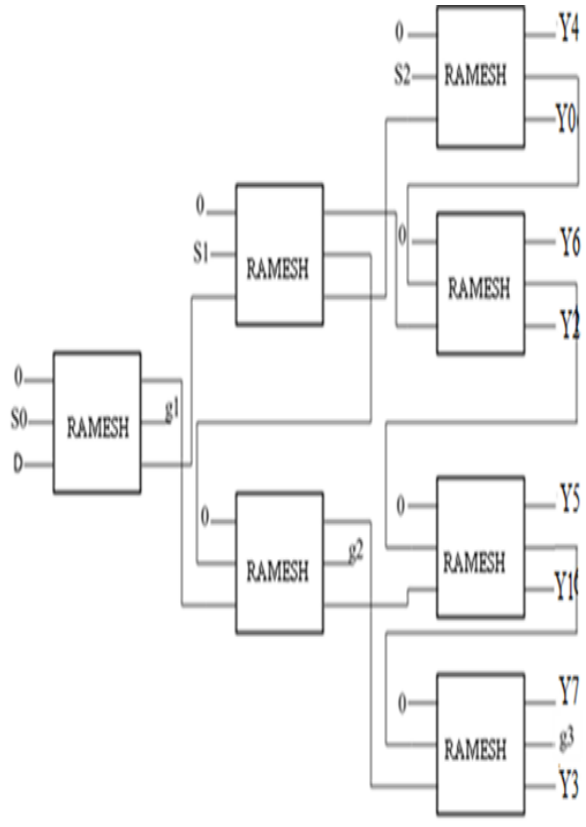

Figure 18: Block Diagram of 1:8 Demultiplexer using RAMESH Reversible Logic Gate.

4.2.2 Design-II using RAMESH-1 Gate

The 1:2, 1:4, 1:8, and 1:16 demultiplexers are implemented using RAMESH-1 gate. The 1:2 demultiplexer realization using RAMESH-1 gate is shown in figure 20.

The block diagram of 1:4 demultiplexer using 3*3 RAMESH-1 reversible logic gate is shown in figure 21. It requires three RAMESH-1 gates. The number of garbage outputs is represented as g_1 and g_2. Garbage inputs are represented by logical zero. Logic zero is 3rd input to every RAMESH-1 reversible logic gate. S_0 and S_1 are the select bits used to select the data inputs.

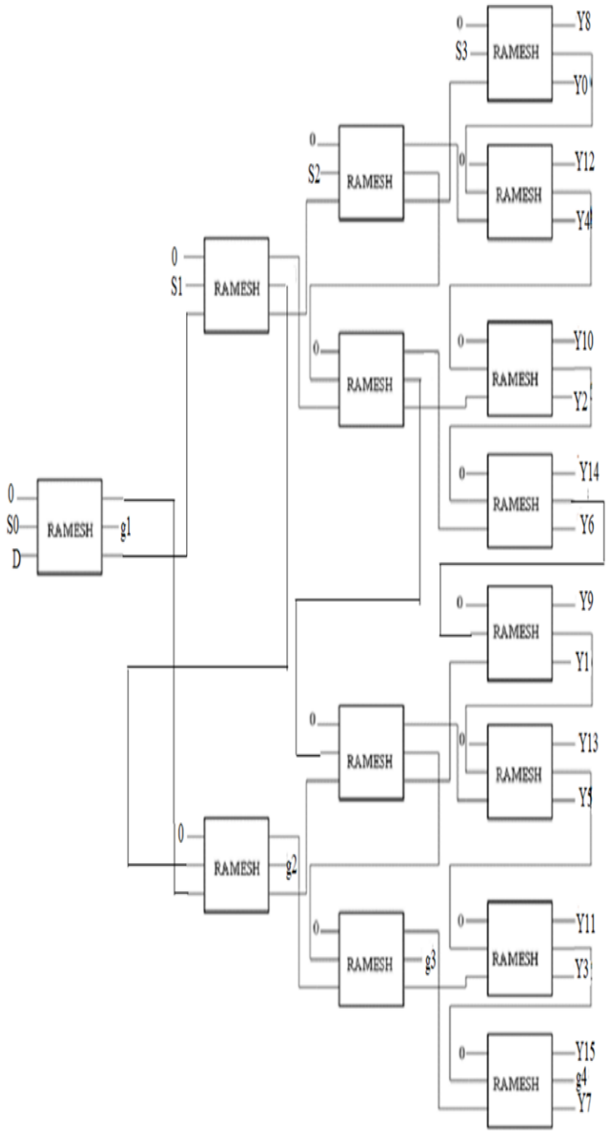

Figure 19: Block Diagram of 1:16 Demultiplexer using RAMESH Reversible Logic Gate.

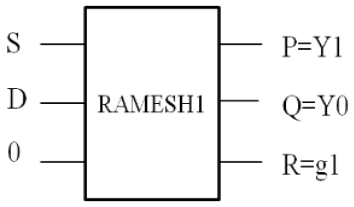

Figure 20: Block Diagram of 1:2 Demultiplexer using RAMESH-1 Reversible Logic Gate.

In the first stage there is one RAMESH-1 reversible logic gate followed by two in the second stage. In the first stage D is 2nd input to the RAMESH-1 reversible logic gate and 1st input is S_0. In the second stage, the first input is S_1 for each RAMESH-1 reversible logic gate and 2nd input is 1st and 2nd outputs of previous stage RAMESH-1 reversible logic gates (for the first RAMESH-1 reversible logic gate 2nd input is 2nd output of previous stage RAMESH-1 reversible logic gate for the second RAMESH-1 reversible logic gate 2nd input is 1st output of previous stage RAMESH-1 reversible logic gate).The outputs of the demultiplexer are stored at P and Q outputs of each RAMESH-1 reversible logic gate. The design process is same for 1:8 and 1:16 demultiplexers respectively. The block diagram of 1:8 and 1:16 demultiplexers using RAMESH-1 gate are shown in figures 22 and 23 respectively.

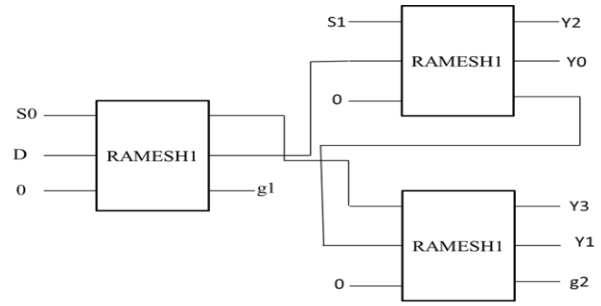

Figure 21: Block Diagram of 1:4 Demultiplexer using RAMESH-1 Reversible Logic Gate.

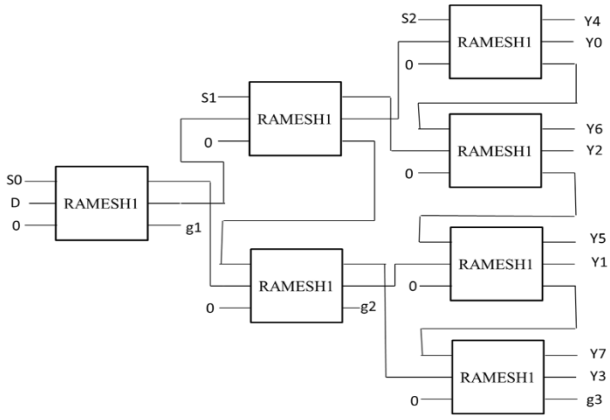

Figure 22: Block Diagram of 1:8 Demultiplexer using RAMESH-1 Reversible Logic Gate.

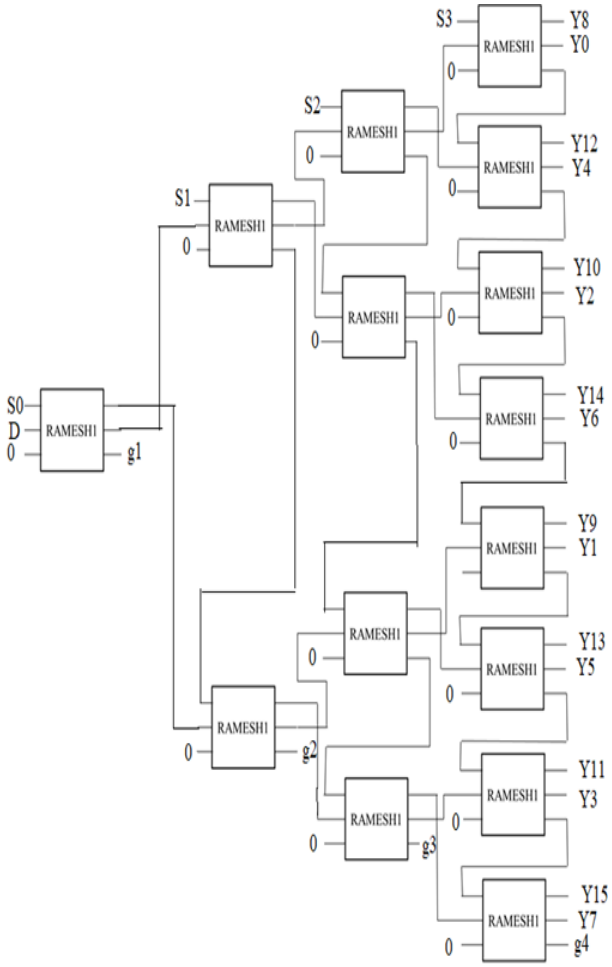

Figure 23: Block Diagram of 1:16 Demultiplexer using RAMESH-1 Reversible Logic Gate.

5. Simulation and Synthesis Results of Multiplexers and Demultiplexers using Reversible Logic Gates

The multiplexers and demultiplexers are implemented with VHDL, simulated and synthesized using Xilinx ISE 12.2i which are mapped on to Virtex-6 (6vlx75tff484-3) FPGA and also the circuits are implemented and simulated using Mentor Graphics. The black box view of 16:1 multiplexer using QCA, SAM and QCA & SAM and 1:16 demultiplexer RAMESH and RAMESH-1 reversible logic gates using Xilinx is shown in figure 24. The schematic diagrams of 16:1 multiplexer using QCA, SAM and QCA & SAM and 1:16 demultiplexer using RAMESH and RAMESH-1 reversible logic gates using Mentor Graphics are shown in figures 25-29 respectively.

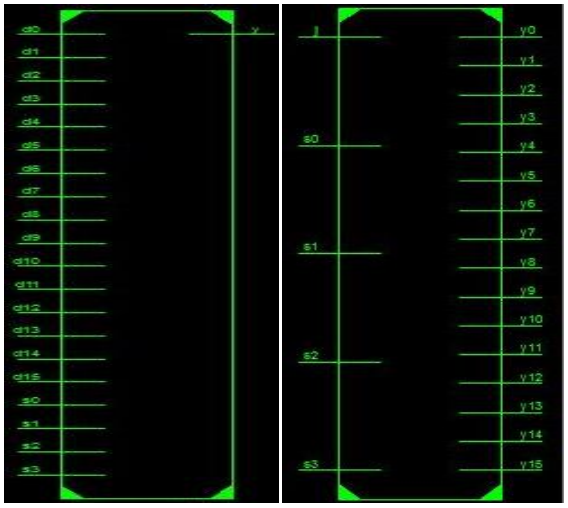

Figure 24: Black Box View of 16:1 Multiplexer using QCA, SAM, and QCA & SAM and 1:16 Demultiplexer using RAMESH and RAMESH-1 Reversible Logic Gates.

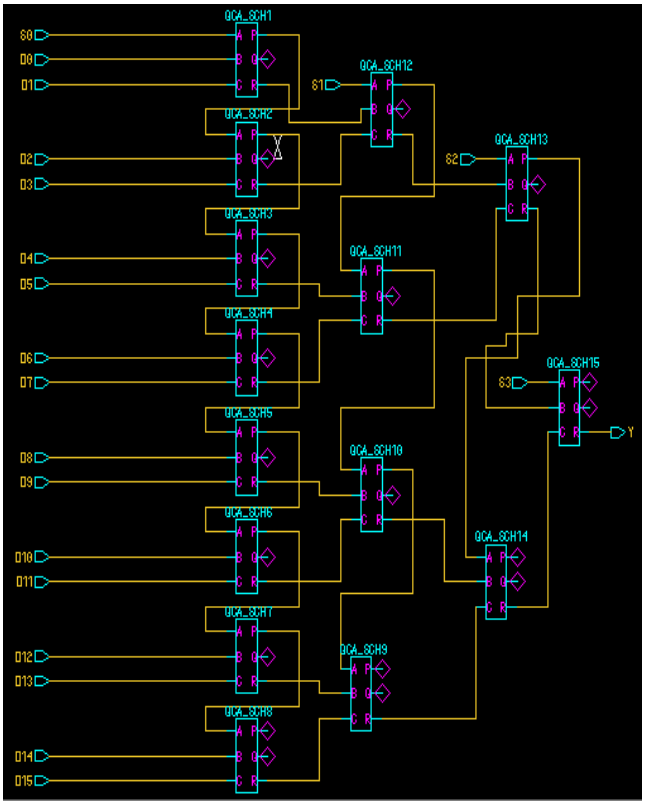

Figure 25: Schematic Diagram of 16:1 Multiplexer using QCA Reversible Logic Gate.

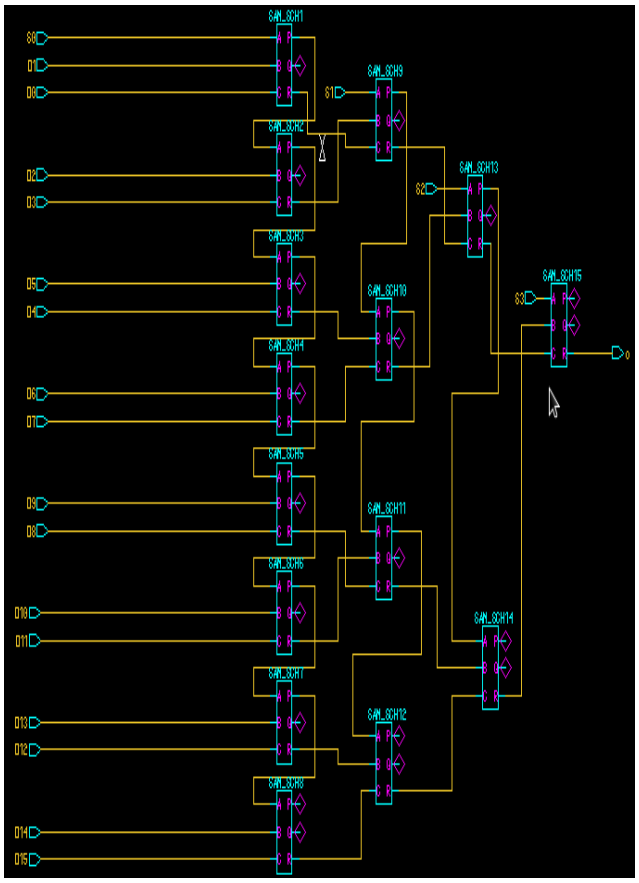

Figure 26: Schematic Diagram of 16:1 Multiplexer using SAM Reversible Logic Gate.

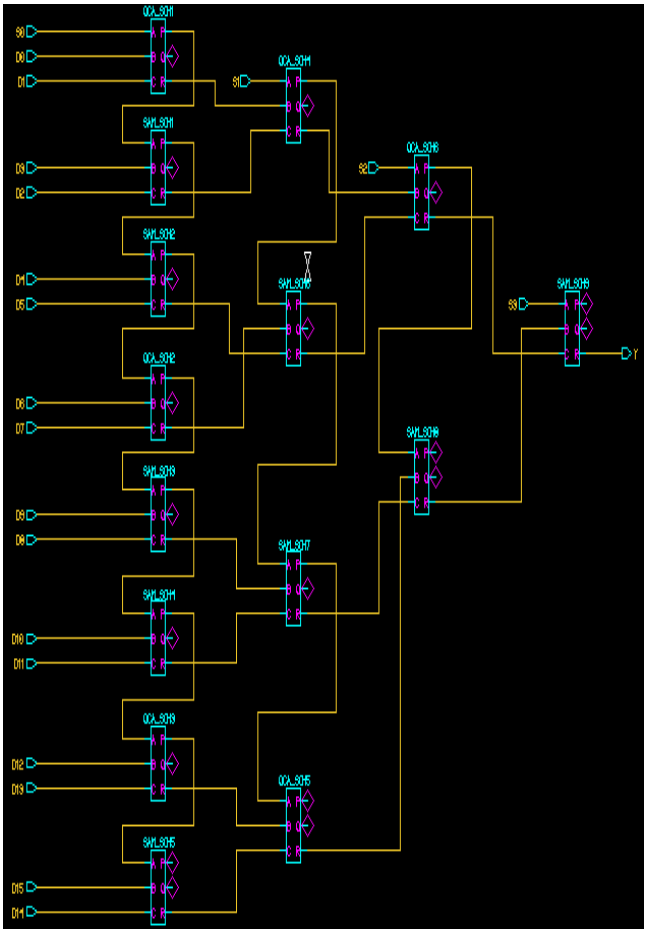

Figure 27: Schematic Diagram of 16:1 Multiplexer using QCA and SAM Reversible Logic Gates.

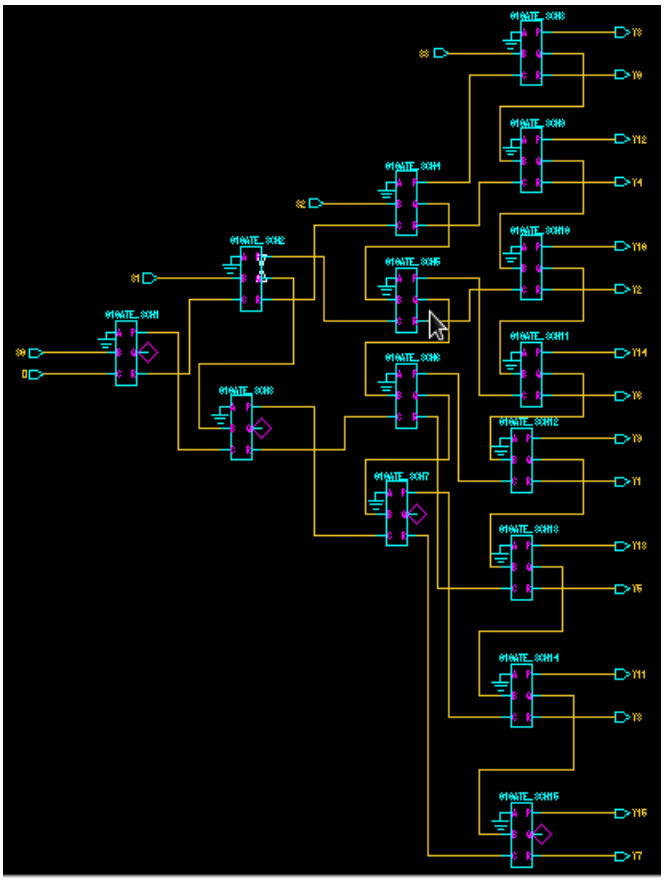

Figure 28: Schematic Diagram of 1:16 Demultiplexer using RAMESH Reversible Logic Gate.

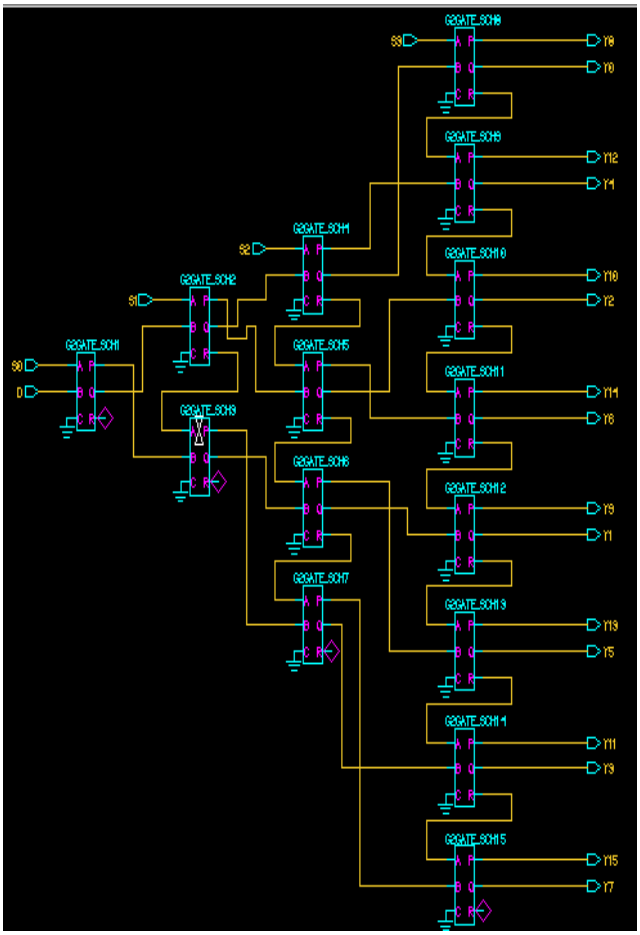

Figure 29: Schematic Diagram of 1:16 Demultiplexer using RAMESH-1 Reversible Logic Gate.

Comparison of power consumption of multiplexer designs, design-I, design-II, and design-III using Mentor Graphics is shown in table 1. The comparison of number of gates and quantum cost for [3] multiplexer designs with existing design [2] and [3] is shown in table 2. Comparison of power consumption of demultiplexer designs, design-I and design- II using Mentor Graphics is shown in table 3. The comparison of number of gates and quantum cost for two demultiplexer designs with existing design [2] and [3] is shown in table 4.

Table 1: Comparison of Power Consumption of Multiplexer Designs, Design-I, Design-II, and Design-III, and with Existing Design [1]

Types of Multiplexer Designs	Power Consumption of Multiplexers				Reduced Power Consumption with Existing Design [1] (%)
	2:1 (µw)	4:1 (µw)	8:1 (µw)	16:1 (µw)	
Existing Method [1]	4.2	--	--	--	--
Design-I using QCA	0.82	3.08	7.66	19.48	80.47
Design-II using SAM	1.14	2.81	6.50	14.58	72.85
Design-III using QCA and SAM	--	3.52	7.30	17.64	---

Table 2: Comparison of Number of Gates and Quantum Cost of Multiplexer Design II with Existing Design [2]

Types of Multiplexer Designs	Design-II				Existing Design [2]			
	2:1	4:1	8:1	16:1	2:1	4:1	8:1	16:1
Number of gates	1	3	7	15	1	3	7	15
Quantum cost	4	12	28	60	5	15	35	75

Table 3: Comparison of Power Consumption of Demultiplexer Designs, Design-I and Design-II with Existing Design [1]

Types Of Demultiplexer Designs	Power Consumption of Demultiplexers				Reduced Power Consumption with Existing Design [1] (%)
	1:2 (µw)	1:4 (µw)	1:8 (µw)	1:16 (µw)	
Existing Method [1]	--	4.7	--	--	----
Design-I using RAMESH	0.97	2.76	6.58	14.30	41.27
Design-II using RAMESH1	0.83	2.76	6.58	14.30	41.27

Table 4: Comparison of Number of Gates of Demultiplexer Design-I and Design-II with Existing Design [3]

Types of Demultiplexer Designs	Design-I and Design-II				Existing Design [3]			
	1:2	1:4	1:8	1:16	1:2	1:4	1:8	1:16
Number of gates	1	3	7	15	-	10	-	-

6. Conclusion

In this work three multiplexer designs, design-I, design-II, and design-III are implemented using QCA [4], SAM [10], and QCA & SAM reversible logic gates respectively. In addition, two demultiplexer designs, design-I and design-II are implemented using RAMESH and RAMESH-1 reversible logic gates respectively.

The 2:1 multiplexer using design-I & design-II reduces 80.47% & 72.85% power consumption compared with existing design [1]. Among these three multiplexer designs, design-II is the best because power consumption reduced by 8.7 % and 20% for 4:1 multiplexer, 15.1% and 10.9% for 8:1 multiplexer, 25.1% and 17.3% for 16:1 multiplexer. Also the quantum cost reduced by 1 for 2:1 multiplexer, 3 for 4:1 multiplexer, 7 for 8:1 multiplexer, 15 for 16:1 multiplexer.

The 1:2 demultiplexer using design-II reduces 14.4 % power consumption compared to design-I. Both the designs reduce power consumption by 41.27 % for 1:4 demultiplexers with existing design [1]. Whereas for 1:4, 1:8, and 1:16 demultiplexer, both designs consumes same power.

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