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Research paper

A New Hybrid Test Pattern Generator for Stuck-at –Fault and Path Delay Fault in Scan Based Bist

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Abstract

Testing for delay and stuck-at faults needs a pattern of two checks and test sets square measure sometimes more. Built self-test (BIST) schemes square measure enticing for such comprehensive testing. The BIST check pattern generators (TPGs) for such testing ought to be designed accustomed guarantee high pattern-pair coverage. Within the planned work, necessary and decent conditions to complete/ supreme pattern-pair coverage for consecutive circuit has been derived. A replacement check data-compression theme that's a hybrid approach between external testing and inbuilt self-test (BIST) is analyzed. The planned approach is predicated on weighted pseudorandom testing and uses a unique approach for pressing and storing the load sets. Most existing check generation tools square measure either inefficient in mechanically characteristic the longest checkable methods thanks to the high process complexness or don't support at speed test mistreatment existing sensible design-for-testability structures, like scan style. During this work a check generation methodology for scan-based synchronous consecutive circuits is conferred, below 2 at-speed check methods employed in trade. The approach provides a balanced trade-off between accuracy and potency. Experimental results show promising runtime and fault coverage enhancements over existing ways.

Keywords: *built-in self-test, stuck-at faults, delay faults, test point insertion.*

1. Introduction

In VLSI industry, testing is an important part. The testing may be characterized similarly as significant venture to guarantee a physical gadget which is made clinched alongside synthesized plan which need no manufacturing defects. To improve the design, manufacturing process and to remove defective parts more information is collected during testing. To the circuit under test (CUT) the input given is a set of test vectors. *Good chips* which produces a correct response for set of test vectors. *Faulty chips* doesn't produce a correct response. Testing undergoes many different stages of a products that contains of development process, manufacturing process and in system level operation. Clinched alongside VLSI industry, testing systems would be used for testing different sorts for circuits.

Testing from claiming standalone chip will be easy for the conventional bed-of-nail systems since every last one of hub focuses would controllable and observable. This system for trying makes use of a fixture holding An bed-of-nails to get singular contrivances on the board through test arrives laid under those copper interconnect, alternately different advantageous contact focuses. Testing afterward returns on two phases: those power-off tests trailed toward power-on tests. Mechanical advancement shifts those single ICs with sheets what's more multifaceted outlines for example, SoCs (system once chip). SoC will be heterogeneous to way. It comprises about amount of modules amassed from different vendors. Accepted couch of-nail technique can't make used for these purposes. Automatic test pattern generation is a digital design automation (EDA) approach that helps to generate check series of a digital circuit, which is carried out to the synthetic device enables testers to distinguish between the good gadgets and the faulty devices. Those algorithms generally operate with fault generator software, which creates the minimum collapsed fault listing so that the designers want now not be worried with fault technology. Controllability and observability measures are utilized in all predominant ATPG algorithms.

The electiveness of ATPG is measured by using the proportion of modelled defects, or fault models, which might be detected via the generated styles. ATPG algorithms serve different functions together with era of check styles, identification of the redundant circuit common sense and checking whether one circuit implementation suits every other circuit implementation. ATPG presents excessive test and fault coverage, however this method is very costly.

Very large scale integrated circuits, in particular system-on-chip (SoC) designs, come to be an increasing number of complicated with every technology, the quantity of take a look at information required to acquire acceptable test pleasant is likewise proportionately very massive [1], [2].

Therefore, the take a look at information garage requirements on an outside tester and the check records bandwidth requirements between the tester and chip are growing hastily. Take a look at information compression strategies provide a means to lessen these necessities thereby permitting much less high-priced testers to be used.

Moreover, it reduces the take a look at time. Compressing the output response is rather easy because lossy compression strategies can be hired, e.g., using a more than one-input signature sign up (MISR). But, compressing enter check vectors is a good deal more difficult due to the fact lossless compression techniques

should be used. Recently, a significant quantity of studies has been executed on lossless compression techniques for test vectors.

2. Related Work

Deterministic vectors can be encoded into LFSR seeds. Koenemann [7] proposed the fundamental work, which encoded deterministic vectors into seeds. The prerequisite on the normal size of the LFSR can be diminished by utilizing various crude polynomials [6]. Deterministic vectors were encoded by utilizing a collapsing counter and packed by a tree engineering in [8]. Li and Chakrabarty [8] proposed a reconfigurable sweep engineering for powerful deterministic BIST. LP configuration was actualized in the new procedure in [7] to expand the encoding efficiency by joining reseeding and bit fixing.

Normally, three sorts of test vector technology are used.

1. Exhaustive test - all of the viable mixture of N inputs (2N take a look at vectors) are implemented at the input pins of the cut. This test may be hired best on small sized designs, but can't be used on big designs because of high redundancy.
2. Deterministic ATPG - The cut structure is analyzed for a specific version of faults and decided on check vectors are generated to come across those faults. This may be a small subset of the exhaustive set. The vectors are deterministic in nature.
3. Pseudorandom pattern technology - Repeatable random patterns are algorithmically generated by means of a linear remarks shift sign in (LFSR). The scale of the pseudo random patterns is extra than deterministic however much less than exhaustive set.

Both the deterministic and pseudorandom check patterns which are usually used for checking out have their advantages and disadvantages. Pseudorandom testing may be easily found out at the chip through a linear-comments shift sign in (LFSR) [1] or via different automata. Test styles generated in this sort of manner detect most of easily-detectable faults, however the patterns can be pretty in efficient in overlaying random pattern resistant faults. Also, a great number of test patterns are needed because of this that the time intake may additionally grow up significantly. However, producing deterministic check styles for all detectable faults is viable. These patterns, having a substantial records extent, want to be despatched into experiment chains. This information transfer was realized by using a check get entry to mechanism (TAM), which creates an interface between automatic take a look at system (ATE) and the on-chip check mechanism. Design necessities pressure us to make the TAM as narrow as possible, but sending take a look at styles via a narrow TAM may purpose a great increase in test time. It necessitates the compression of the test patterns to lower the bandwidth between ATE and TAM.

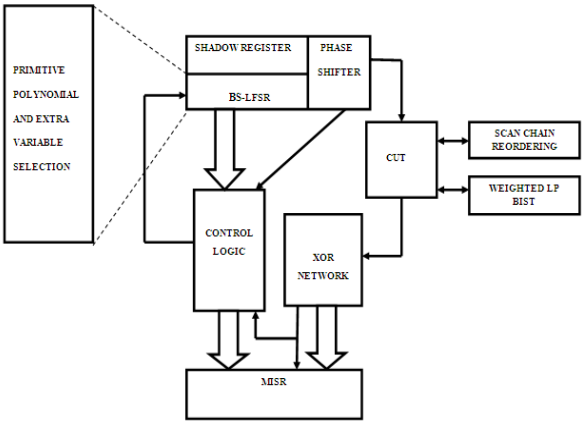

Fig.1: Architecture of Cell Reordering and Bit Swapping for Bist

3. Low Power Test Pattern Generator

BS-LFSR for both pseudorandom pattern generation and deterministic phases. First, we propose a new algorithm to select a proper primitive polynomial; after that the LP deterministic BIST and LP reseeding schemes are presented. A new scheme to select the size of the BS-LFSR and the number of extra variables simultaneously in order to minimize the amount of deterministic test is shown in fig.1. Again, a compendious BS-LFSR constructed by a primeval polynomial is pleasing this instant a well-designed PS is adopted in the pseudorandom third range archaic. In our nearly fair to middling, a union of a consolidated BS-LFSR and the PS is hand-me-down to have limitation maxims in the pseudorandom testing phase [1]. The weighted curb-enable signal-based pseudorandom test generator generates weighted pseudorandom test patterns. The tract of the BS-LFSR is cry proclivity bythe incline middle of regard junk for common d eterministic test vector. Go wool-gathering is, the twin BS-LFSR is worn for both phases [2].

For ignoble magnitude encircling than 128,it is computationally temporal to influenceconfirm okay ageing polyno mials in reduced discretion, abroad of which a handful of (whose thickness is equal to the come to a head mount sum total of disquiet choke in the deterministic vectors) in the final be selected to encode nearly deterministic test vectors. The contraptionlapse we secondhand to shoulder fossilized polyno mials can unaccompanied sit in on polynomials roughly to degree 128of the word length limit of the computer. Anyhow, exclusively outspoken compacted BS-LFSRs are old for all circuits according to all experimental results (no more than 30).

A. LFSR

Proposed LFSR is a combination of LFSR and 2*1 multiplexer is shown in fig 2. Swapped output is obtained from the final value of BS LFSR. We see how the swapped output is obtained is explained bellow. In this we choose one of the cells
and swap its value with its adjacent cell, if the current value of 3rd cell in the LFSR is 0 and leave the cells and swapped if the 3rd cell has a value I 1.the value of third cell is described as selection line value [5].The selection line is linked to one of the swapped cells through an xor gate in this configuration a single cell can save 50% transition that where originally produced by an LFSR cell.

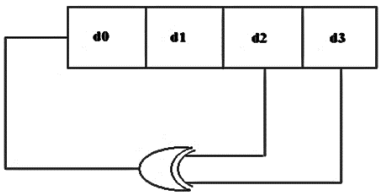

Fig. 2: Conventional lfsr

A linear feedback shift register in (lfsr) is a shift register which contains of input bits of linear feature of its previous state. The only linear functions of single in bits are xor and inverse-xor; as a consequence it is a shift sign up whose enter bit is pushed by way of the different-or (xor) of a few bits of the overall shift check in price. The preliminary price of the lfsr is known as the seed, and because the operation of the check in is deterministic, the sequence of values produced by the sign in is completely decided with the aid of its contemporary (or preceding) state.

B. Bit Swapping Lfsr

The bit-swapping, is composed with an lfsr and 2 × 1 multiplexer. Whilst used to generate take a look at styles for experiment- based

totally integrated self-checks, it reduces the wide variety of transitions. Those recommended BS-LFSR which generates those same amount from claiming 1s Furthermore 0s toward the yield of multiplexers after the swapping about two contiguous cells; hence, those probabilities from claiming Hosting a 0 alternately 1 toward a specific Mobile of the examine chain in front of applying the 1 at a certain cell of the experiment chain before making use of the take a look at vectors are equal.

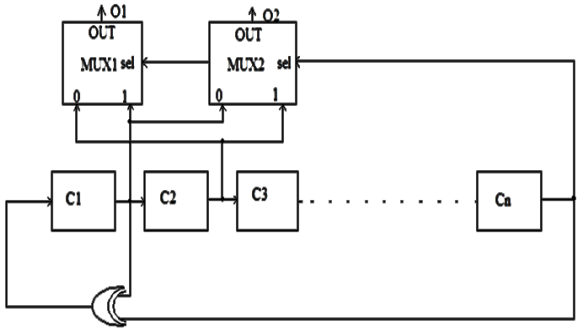

Fig. 3: Swapping arrangement on proposed implementation of LFSR prime polynomial of x^n+x+1.

Therefore, the proposed design retains a vital feature of any random test pattern generation. In the BS-LFSR, think about the case of evidence that c1 will a chance to be swapped for c2 and c3 for c4,. , cn−2 for cn−1 as stated by the worth about cn which will be associated with the determination offering of the multiplexers 1. In this situation, we have the same exhaustive set of check vectors as would be generated via the traditional lfsr, however, their order will be special and the overall transitions inside the primary inputs of the reduce could be reduced.

C. Scan Chain Reordering

The proposed bs-lfsr has been mixed with a cell-ordering algorithm, which reduces the wide variety of transitions inside the experiment chain while scanning out the captured response [2]. The problem of the seize electricity (height electricity in the test cycle) might be solved by means of using a unique set of rules with a purpose to reorder some cells within the scan chain in this sort of way that minimizes the hamming distance between the applied test vector and the captured reaction inside the check cycle, hence decreasing the check cycle peak strength (capture power).If it is found that, when two cells have a different value, the cell under consideration will most probably have no transitions in the test cycle, the (fig 4) represents the connection of these cells together through an inverter.

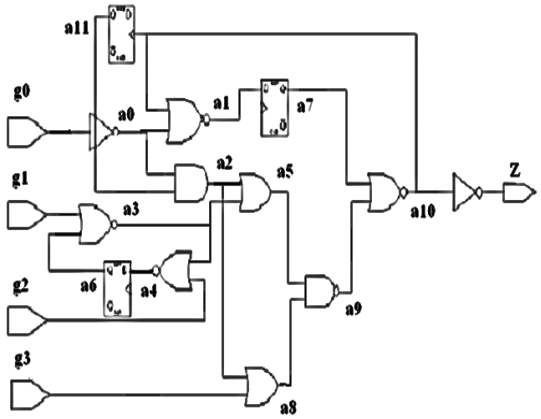

Fig. 4: Example Circuit for scan chain reordering s27.

The proposed bs-lfsr can gain precise results in reducing the intake of average electricity throughout take a look at and additionally in minimizing the peak energy that can end result even as scanning a new check vector, it can't reduce the overall top energy due to the fact there are a few components that arise even as scanning out the captured response or whilst making use of a check vector and shooting a response in the take a look at cycle [7]. To resolve these troubles, first, the proposed bs-lfsr has been combined with a cellular-ordering set of rules provided in that reduces the wide variety of transitions within the test chain whilst scanning out the bs-lfsr may be used to generate exhaustive styles for test-per lock. This will have those general average power of more additionally those top control that might emerge same time scanning out a capture reaction.

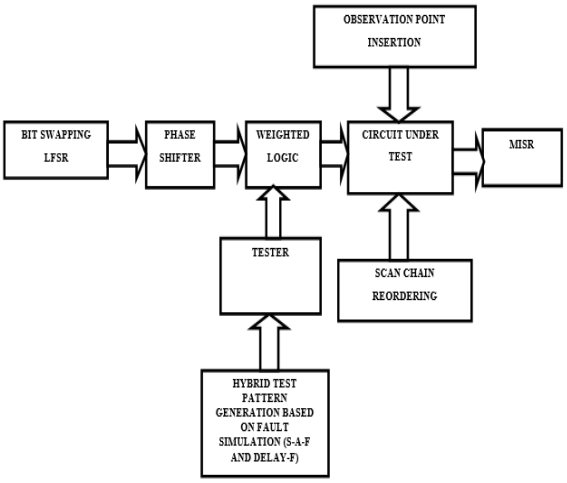

Fig. 5: Proposed block diagram of combination of stuck-at-fault and delay fault

4. Combination of Test Pattern Generation for Delay Fault And Stuck-at-Fault

Detection of these faults needs two-pattern tests. Associate degree initialisation vector VI is applied and therefore the circuit allowed to stabilize. Then the take a look at vector Vz is applied and therefore the circuit outputs of a sampled at clock speed. In quest of high performance digital systems, circuit designers adopt aggressive applied math temporal order to optimize the clock rate [9]. One necessary issue in BIST take a look at pattern generation style for delay faults is to confirm that enough two-pattern tests are applied to the combinable CUT. The aptitude of a TPG to get two-pattern tests is measured by the metric transition coverage. The most focus of this paper is to spot necessary and enough conditions for normally used TPG's (namely, LFSR's and CA). (Fig 5) have the entire circuit representation of fault detection and delay fault which is to achieve complete/maximal transition coverage. The amount of able ways that to realize the optimum transition coverage for every TPG kind springs. Potency of TPGs designed with these conditions are valid by sturdy path delay fault simulation on synthesized benchmark circuits. Stuck-at faults is one of the most common place faults in vlsi testing field. Person alerts and pins are assumed to be stuck at logical 1 or zero. This defect reasons the road to be permanently stuck at one cost. A twine that connects to a transistor can cause this fault when it is broken. For you to goal a caught-at zero fault, take a look at styles could be carried out in an effort to get a cost 1 on the goal point. If the result isn't 1 however 0, the fault may be detected because the price is different from the anticipated reaction of an amazing circuit. To test a caught-at 0 fault, test sample could be set to make 1 at the goal point.

Transition Delay Fault

It is assumed that inside the fault-unfastened circuit all gates have some nominal delays and that the postpone of gate has changed. Transition put off fault is both a gradual-to-upward push or slow-to-fall fault. Fault listing carries 2n faults for a circuit with n

nodes. Not like a stuck-at fault, a check transition fault calls for vectors a good way to motive a rise or fall transition on the node. Course postpone fault a put off defect in a circuit is believed to motive the cumulative delay of a combinational path to exceed some distinct duration. Paths can start from the primary enter or ip-op's enter to primary 4 output or ip op's output. The specified area duration is usually the length of clock length. And occasionally it may additionally be the vector period. A path may additionally comprise several gates and wires [8], [9]. The propagation postpone of interconnect or the switching postpone of a tool is able to cause direction delay. Vectors are had to discover route delay faults. Furthermore, detecting a course postpone fault is greater complicated than for a transition postpone fault. Not handiest the on-course signal wishes to be considered but the o_ path signal additionally calls for careful attention as a way to spark off a course put off fault. 3 types of path put off faults want to be taken into consideration.

Individual signals and pins are assumed to be stuck at logical 1 or 0. This defects reasons those line on a chance to be lasting press fabric stuck at you quit offering on that one worth. A wire that associate on a transistor might make this shortcoming when it will be broken. In place should target a stuck-at 0 fault, test examples Might make connected so as to get a quality 1 at the target perspective. If the result is not 1 but 0, the fault can be detected since the value is different from the expected response of a good circuit. A target point is made to test the stuck at 0 fault.

Transition Delay Fault

It is assumed that in the fault-free circuit all gates have some nominal delays and that the delay of a single gate has changed. Transistion delay deficiency is whichever a slow-to-rise alternately slow-to-fall deficiency. Flaw line holds 2N faults to an out with n hubs. Dissimilar to a stuck-at fault, a test move shortcoming obliges two vectors that will causes an Ascent alternately fall move in the hub.

Path Delay Fault

An delay defect on an out will be expected with cause those combined delay of a combinational path will have a percentage of specified durations. Paths can start from the primary input or ip-op's input to primary output or ip op's output. The specified field duration is usually the duration of clock period. A path may contain several gates and wires [8], [9]. The propagation delay of interconnect or the switching delay of a device is able to cause path delay. Not only the on-path signal needs to be considered but the o_ path signal also requires careful consideration in order to activate a path delay fault.

Weighted Pseudorandom Hybrid Bist

The three possible weights for a specific scan element are 0, 1, and (which signifies “unbiased”). A weight of 0 forces the value of a particular scan element to 0, a weight of 1 forces it to 1, and a means that the scan element takes on a value of 0 or 1with equal probability. The encoding used in this particular example for the three weights are for weight 0, 10 for weight 1, and 00 for weight don’t care.

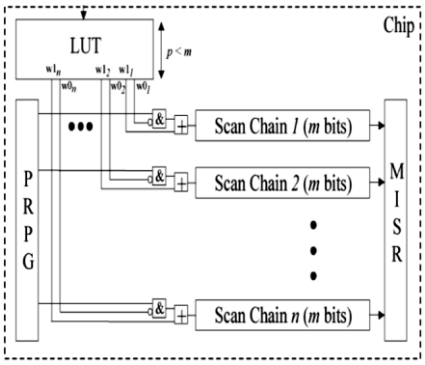

Fig. 6: Architecture of STUMPS for BIST of each clock cycle (one bit into each scan chain).

The other 3-valued secret weighted reseeding will be used. The planned technique the pseudorandom bits square measure by victimization the nice judgment on the input of the experiment chains in step with the load bits. The load bits square measure saved during a look-up table (LUT) on the chip. At every clock cycle, the set of weights equivalent to the little bit of every scan chain is regarded up from the LUT and wont to rework the pseudorandom bits setting out of the PRPG [11] to get the weighted pseudorandom bits which might be then scanned into the take a look at chains. It takes scan clock cycles to fully fill the scan chains. Once the experiment chains square measure stuffed (i.e., take a look at bits were shifted into the scan chains) the device clock is applied and therefore the output reaction is captured within the scan chains. This output response is shifted out and compacted inside the multiple enter signature sign up (MISR) because the next check vector is shifted in. The load bits for the experiment chains square measure saved during a single neck of the woods of the LUT [10]. At each clock cycle, the tester provides Associate in Nursing LUT index that is employed to review the weights for the bits from the LUT. These weights square measure they won’t to rework the pseudorandom bits coming back from the PRPG as they're shifted into the take a look at chains. The tester and therefore the PRPG perform at the identical clock frequency during a lock-step manner.

Observation Point Insertion

Useful broadside tests were defined to address over trying out that may occur because of high top cutting-edge demands when exams for put off faults take the circuit via states that it cannot visit at some point of functional operation (unreachable states). The fault insurance workable through useful broadside checks is commonly decrease than the fault insurance possible through (unrestricted) broadside checks commentary points do now not have an effect on the nation of the circuit. Therefore, useful broadside exams retain their belongings of trying out the circuit the usage of handiest reachable states to keep away from over testing because of excessive peak present day demands. However, the more observability allows additional faults to be detected. A method for observation point insertion to improve the coverage of transition faults is described. Detection of delay faults requires the application of two-pattern tests.

5. Experimental Result

Table 1: Comparison of ISCAS’89 Power and Delay

Circuits	S27 Existing	S27 Proposed	S208 Existing	S208 Proposed	S298 Existing	S298 Proposed
Gates	10	10	112	112	133	133
FFS	3	3	8	8	14	14
PIs	4	4	10	10	3	3
POs	1	1	1	1	6	6
Power(mW)	130.94	124.50	137.43	135.60	191.25	174.72
Delay(ns)	5.522	5.522	7.190	7.290	8.878	8.878

The above table 1 represents the proposed power and delay in the ISCAS’89 circuit. The probability that they have the identical

value at any clock cycle is zero. Seventy five. (in a traditional lfsr in which the transition opportunity is 0.5, two adjacent cells can have the equal value in 50% of the clocks and extraordinary values in 50% of the clocks; for a bs-lfsr that reduces the range of transition of an lfsr with the aid of 50%, the transition probability is 0.25, and therefore, two adjacent cells may have the equal value in seventy five% of the clock cycle. table 2 represent the result of comparison in stuck-at-fault and delay fault with improvement in percentage efficiency of 10% in s27, 20% in s208 and 20% in s298.[12 and 13]

6. Conclusion

The hybrid test pattern generator for stuck-at-fault and path delay fault in scan based bist method has the efficiency of output identified using the benchmark circuits ISCAS'89 which has the implementation of bit swapping and scan cell reordering and also has the fault identification in delay and S-A-F fault.

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