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Research paper

Novel design of multiplexers using adiabatic logic

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Abstract

Multiplexer (or Mux) is a digital circuit that selects one of several analog or digital input signals and forwards the selected input into a single line. A multiplexer is also called a data selector. Multiplexers implemented in different ways. Adiabatic logic dissipates less energy loss because of thermodynamic process, in which there is no energy exchange. Adiabatic logic works with the concept of switching activities which reduces the power by giving stored energy back to the supply. These circuits are low power circuits which use reversible logic to conserve energy. In this paper three multiplexer designs are implemented using CMOS logic and two adiabatic logic methods i.e., Efficient Charge Recovery Logic (ECRL) and Clocked Adiabatic Logic (CAL). These circuits are designed, simulated and synthesized using Mentor Graphics tool. The result shows that CAL design consumes less power compared with ECRL and CMOS logic.

Keywords: *Multiplexer; CMOS Logic; Adiabatic Logic; Low Power.*

1. Introduction

A multiplexer is a digital circuit that allows one of several analog or digital input signals, which are to be selected and transmits the input that is selected into a single medium. Multiplexer is abbreviated as Mux. A multiplexer of 2^n inputs has n select lines that will be used to select input line to send to the output. The block diagram of 2^n x1 multiplexer is shown in figure 1. In that 2^n indicates the number of input signals and n indicates the number of control lines or selection lines. A multiplexer is used in numerous applications like, where multiple data can be transmitted using a single line. A novel class of logic circuits called adiabatic logic offers less energy dissipation during the switching events, and also it recycle and reuse the energy.

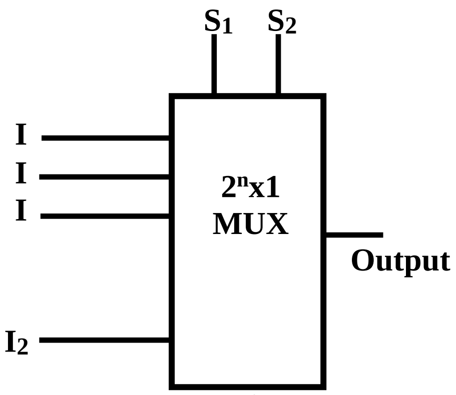

Fig. 1: Block Diagram of 2^n x1 Multiplexer.

2. Literature survey

G.P.S. Prashanti, N. Navya Sirisha and N. Akhila Reddy [1] implemented the basic gates i.e. inverter and NAND gates using adiabatic logic with ECRL method. Durgesh Patel, Dr. S. R. P. Sinha, and Meenakshi [2] implemented the gates i.e. NAND, NOR, and XOR gates using adiabatic logic with PASCL method. Munish Mittal, and Anil Khatak [3] implemented the adder and subtractor circuits using adiabatic logic with ECRL method. Anu Priya, and Amrita Rai [4] implemented inverter using adiabatic logic with ECRL method. The ECRL inverter chain shows 10 to 20 times power gain over a conventional inverter chain. Li, Yimeng Zhang, and Tsutomu Yoshihara [5] implemented the inverter using adiabatic logic with clocked method. The above designs reduce the power consumption compared to CMOS logic.

Multiplexers can be implemented in many ways. In this work, three multiplexer designs are implemented using CMOS logic and two adiabatic logic methods i.e., ECRL and CAL. 2:1 multiplexer is implemented using NOT, AND, and OR gates, 4:1 multiplexer is implemented using 2:1 multiplexers and 8:1 multiplexers is implemented using 4:1 and 2:1 multiplexers.

3. Proposed work

3.1. Multiplexers designs (2:1, 4:1, and 8:1) using CMOS Logic, ECRL, and CAL

The 2:1, 4:1, and 8:1 multiplexers are implemented using CMOS logic, ECRL, and CAL. The schematic diagram of 2:1 multiplexer is shown in figure 2. It consists of NOT, AND, and OR gates. It has two inputs (I_0 and I_1), one select line (S), and one output (Y). The output of the multiplexer depends on the value of the select line S.
The block diagram of 4:1 multiplexer is shown in figure 3. It consists of three 2:1 multiplexers. It has four inputs (Co to C4), two select lines (A and B), and one output (OUT). In the first stage the outputs of the two 2:1 multiplexer are given to the input of 2nd stage 2:1 multiplexer which gives the desired output. The output of the multiplexer depends up on the values of the select lines (A and B).

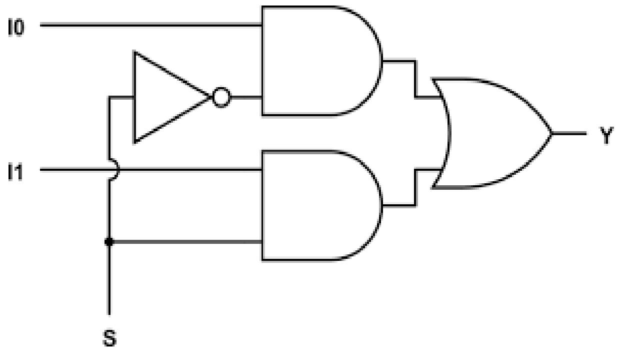

Fig. 2: Schematic Diagram of 2:1 multiplexer Using CMOS logic, ECRL, and CAL.

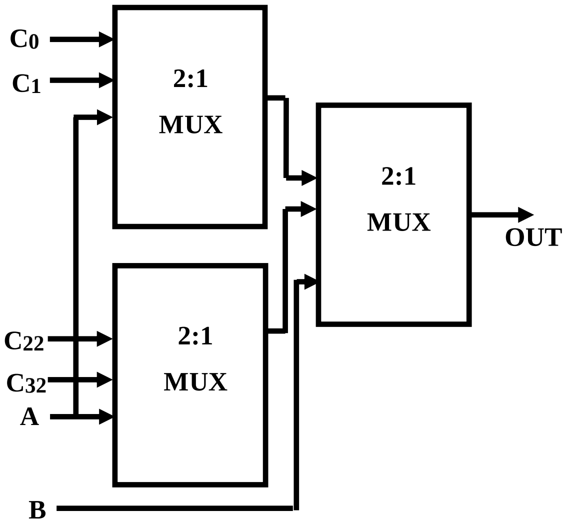

Fig. 3: Block Diagram of 4:1 Multiplexer Using CMOS Logic, ECRL, and CAL.

The block diagram of 8:1 multiplexer is shown in figure 4. It consists of two 4:1 and one 2:1 multiplexers. It has eight inputs (C_0 to C_7), three select lines (S_0 to S_2), and one output (OUT). In the first stage the outputs of the two 4:1 multiplexer are given to the input of 2nd stage 2:1 multiplexer which gives the desired output. The output of the multiplexer depends on the values of the select lines (S_0 to S_2).

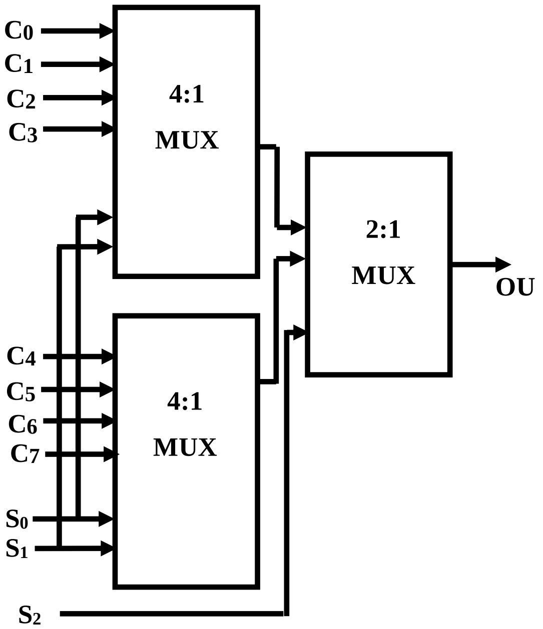

Fig. 4: Block Diagram of 8:1 Multiplexer Using CMOS logic, ECRL, and CAL.

The schematic diagram of 2:1 multiplexer is implemented using NOT, AND, and OR gates with CMOS logic. The block diagram of 4:1 and 8:1 multiplexers are implemented using three 2:1 multiplexers and one 2:1 & two 4:1 multiplexers respectively. Similarly the schematic diagram of 2:1 multiplexer is implemented using NOT, AND, and OR gates with ECRL. The block diagram of 4:1 and 8:1 multiplexers are implemented using three 2:1 multiplexers and one 2:1 & two 4:1 multiplexers respectively. Similarly the schematic diagram of 2:1 multiplexer is implemented using NOT, AND, and OR gates with CAL. The block diagram of 4:1 and 8:1 multiplexers are implemented using three 2:1 multiplexers and one 2:1 & two 4:1 multiplexers respectively.

3.2. NOT, AND, OR gates designs using CMOS logic

CMOS circuits are constructed in such a way that all P-type metal-oxide-semiconductor (PMOS) transistors must have either an input from the voltage source or from another PMOS transistor (pull-up network). Similarly, all NMOS transistors must have either an input from ground or from another NMOS transistor (pull-down network).

The schematic diagram of NOT gate using CMOS is shown in figure 5. It consists of one input (A) and one output (Q). When a logic 1 (5 V) is given at input terminal (A) of the inverter, the PMOS becomes OFF and NMOS becomes ON, so the output will be pulled down to Vss. When a logic 0 (0 V) is given at input terminal (A) of the inverter, the PMOS becomes ON and NMOS becomes OFF, so the output will be pulled up to Vdd.

The schematic diagram of AND gate using CMOS is shown in figure 6. It consists of two inputs (A, B) and one output (F). When any one of the inputs are at logic 0 (0 V), the output will be pulled down to Vss. When both the inputs are at logic 1 (5 V), the output will be pulled up to Vdd. The schematic diagram of OR gate using CMOS is shown in figure 7. It consists of two inputs (A, B) and one output (Q). When both the inputs are at logic 0 (0 V), the output will be pulled down to Vss. When any one of the inputs are at logic 1 (5 V), the output will be pulled up to Vdd.

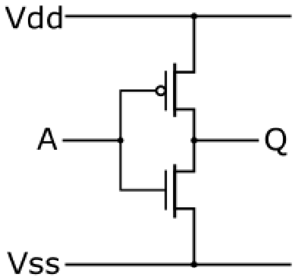

Fig. 5: Schematic Diagram of NOT Gate Using CMOS Logic.

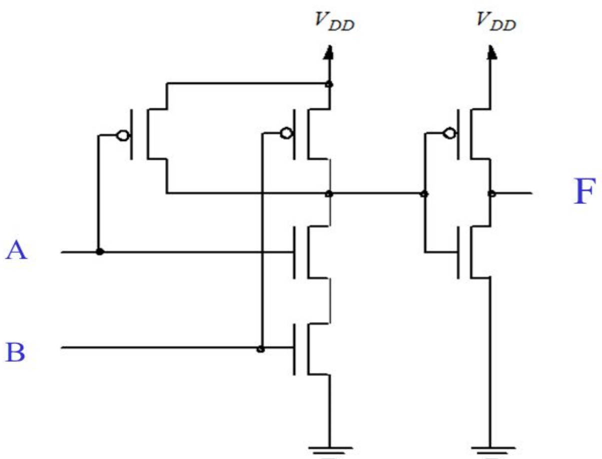

Fig. 6: Schematic Diagram of AND Gate Using CMOS Logic.

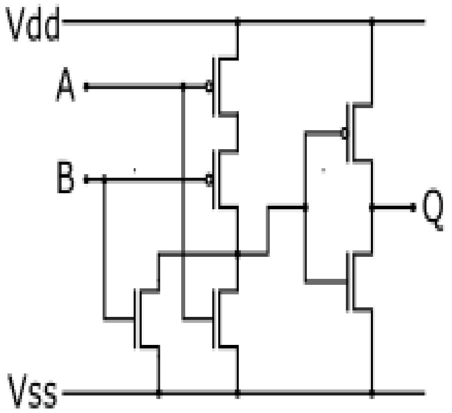

Fig. 7: Schematic Diagram of OR Gate Using CMOS Logic.

3.3. NOT/NOTBAR, AND/NAND, OR/NOR gates designs using ECRL

ECRL performs pre charge diode and dissipates less energy. In ECRL pre charge and evaluation are perform simultaneously. VDD is used to recover and reuse the supply energy. The schematic diagram of NOT gate using ECRL is shown in figure 8. The transistors N1 and N2 implement the inverter logic whereas P1 and P2 allow the output nodes to discharge the VDD. Assume A=1 and Abar =0, when the VDD power clock supply VCLK rises from 0 to VDD, voltage at OUT node remains at VSS i.e. low due to switching ON of the N1 transistor. The voltage at the OUT node capacitance follows the VCLK signal. When the power clock reaches VDD level, the outputs hold valid logic levels. These values are maintained during the hold phase. After the evaluation or hold phase, the VCLK falls down to a ground level, the OUT node capacitance discharges adiabatically into the power clock supply recovering the energy.

The schematic diagram of AND / NAND gate using ECRL is shown in figure 9. AND / NAND gate multiplies A and B. It comprises of two outputs such that one output OUT gives the operation of AND gate and $\overline{\textbf{OUT}}$ gives the complimentary operation of AND gate i.e. NAND gate. The schematic diagram of OR/ NOR gate using ECRL is shown in figure 10. OR/ NOR gate multiplies A and B. It comprises of two outputs such that one output OUT gives the operation of OR gate and $\overline{\textbf{OUT}}$ gives the complimentary operation of OR gate i.e. NOR gate.

3.4. NOT, AND, OR gates designs using CAL

CAL consists of two stages logical evaluation and hold stage. The CMOS logic part acts for logical evaluation and clock control part controls the connection between logic part and the output node. The circuit is powered by two complementary sinusoidal supply clocks power clock (PC) and PC_bar. The schematic diagram of NOT gate using CAL is shown in figure 11.

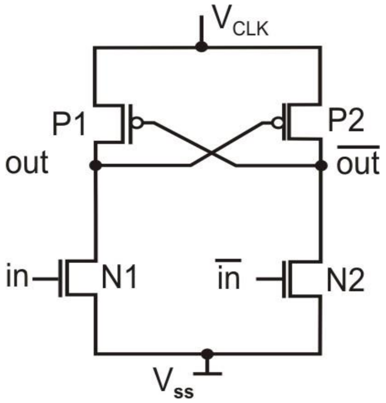

Fig. 8: Schematic Diagram of NOT Gate Using ECRL.

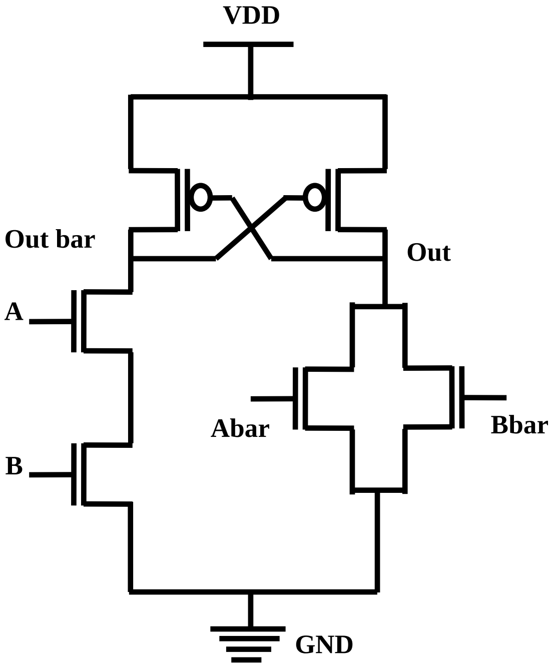

Fig. 9: Schematic Diagram of AND/NAND Gate Using ECRL.

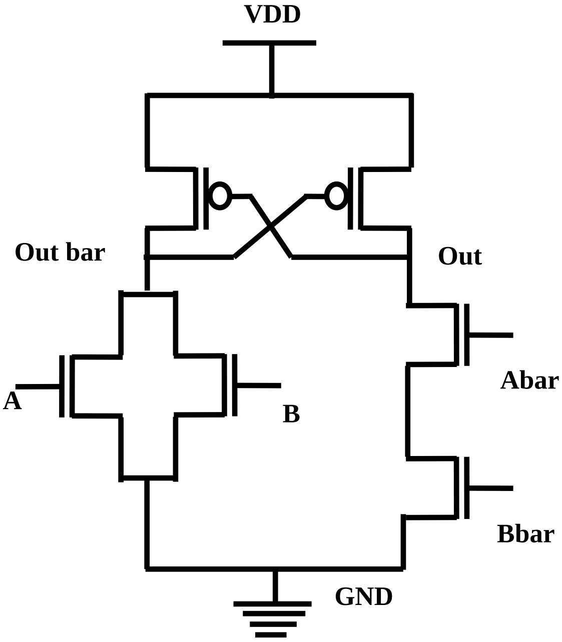

Fig. 10: Schematic Diagram of OR/NOR Gate Using ECRL.

The PC and PC_bar are high half cycle and low half cycle respectively, M1 and M2 becomes ON. Then both the P and N logic blocks are connected to the output node, evaluate the logic values and transferred to the output node. When the input signal is high, M4 is ON, and then the output turns low. When the input signal is low, M3 is ON, and then the output turns high. When the PC and PC_bar are low half cycle and high half cycle respectively, M1 and M2 are OFF. So the output is in a high impedance state. The schematic diagram of AND gate using CAL is shown in figure 12. The AND gate is designed by cascading the NAND with inverter gate. The AND gate output is obtained when the transistors M1, M2 in inverter and transistors M6, M7 in NAND are turned ON. The schematic diagram of OR gate using CAL is shown in figure 13. The OR gate is designed by cascading the NOR with inverter gate. The OR gate output is obtained when the transistors M1, M2 in inverter and transistors M5, M6 in NOR are turned ON.

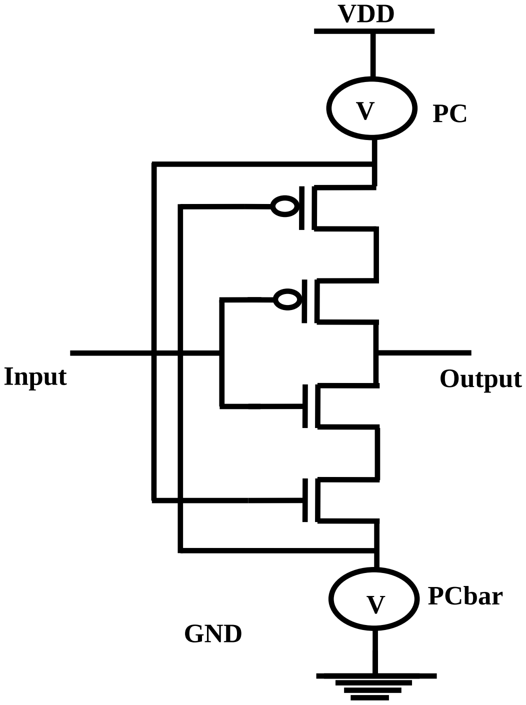

Fig. 11: Schematic Diagram of NOT Gate Using CAL.

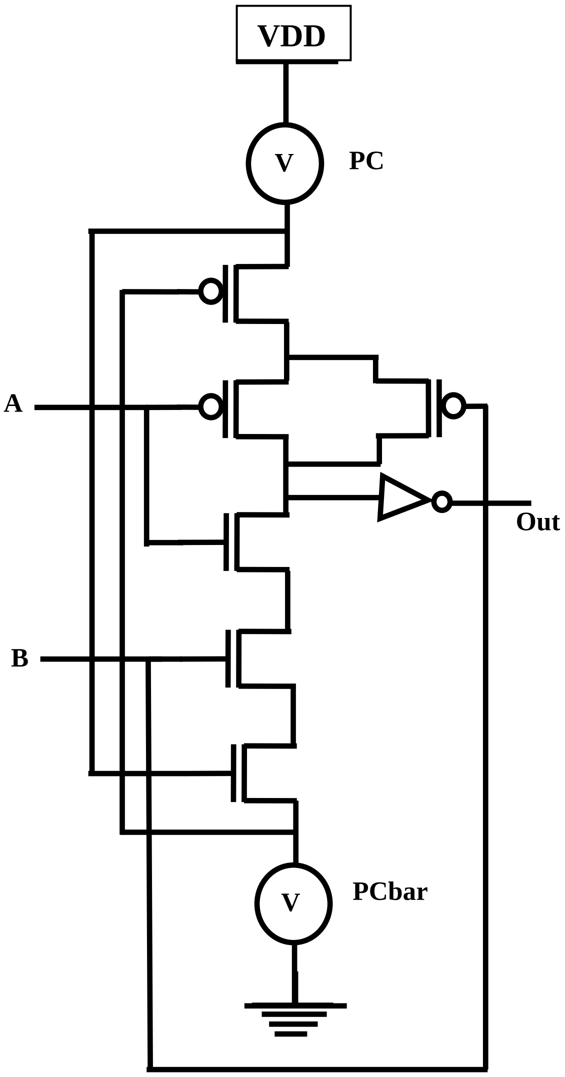

Fig. 12: Schematic Diagram of AND Gate Using CAL.

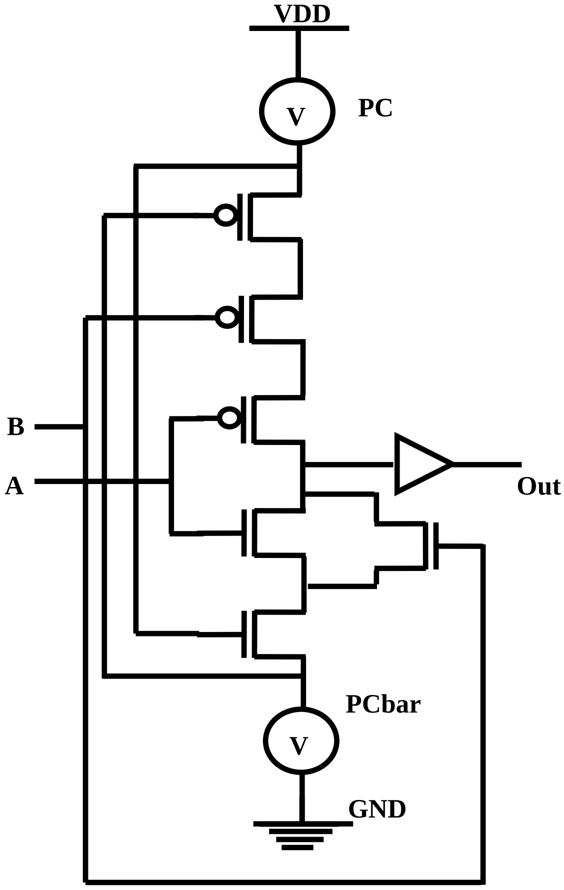

Fig. 13: Schematic Diagram of OR Gate Using CAL.

4. Simulation and synthesis results of multiplexers using CMOS logic, ECRL, and CAL

The three multiplexer circuits are designed, simulated, and synthesized using Mentor Graphics tool. The schematic diagram of NOT, AND, OR gates, and 2:1 multiplexer, the block diagrams of 4:1 and 8:1 multiplexers using CMOS logic are shown in figures 14 to 19 respectively. The schematic diagram of NOT, AND, OR gates, and 2:1 multiplexer, the block diagrams of 4:1 and 8:1 multiplexers using ECRL are shown in figures 20 to 25 respectively. The schematic diagram of NOT, AND, OR gates, and 2:1 multiplexer, the block diagrams of 4:1 and 8:1 multiplexers using CAL are shown in figures 26 to 31 respectively.

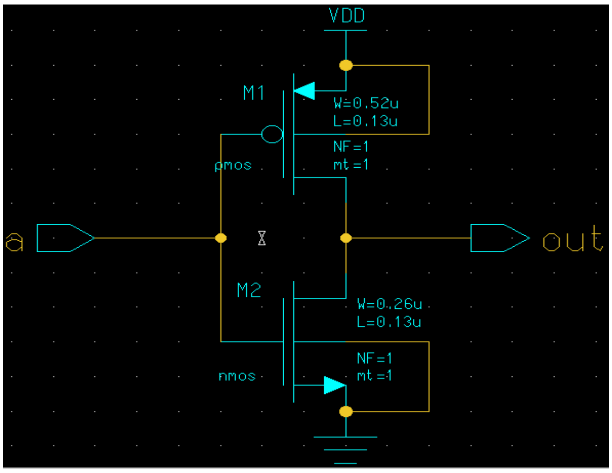

Fig. 14: Schematic Diagram of NOT Gate Using CMOS Logic.

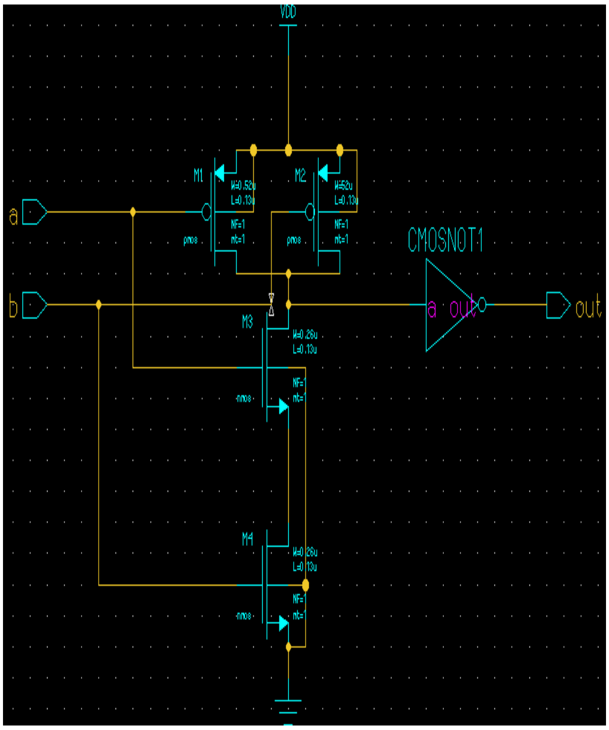

Fig. 15: Schematic Diagram of AND Gate Using CMOS Logic.

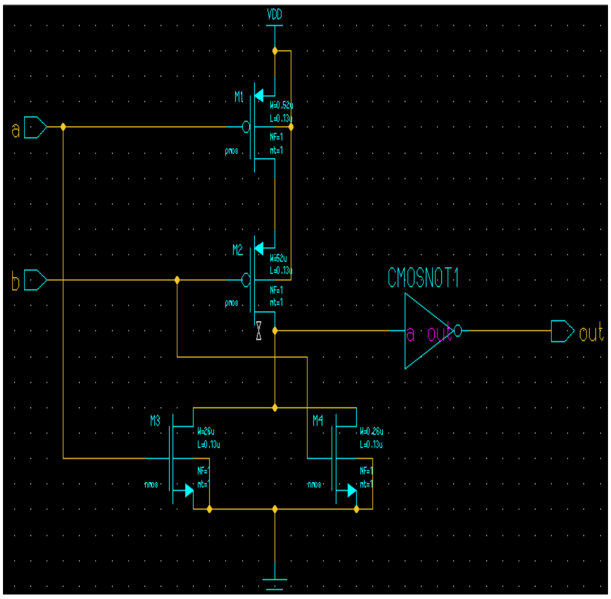

Fig. 16: Schematic Diagram of OR Gate Using CMOS Logic.

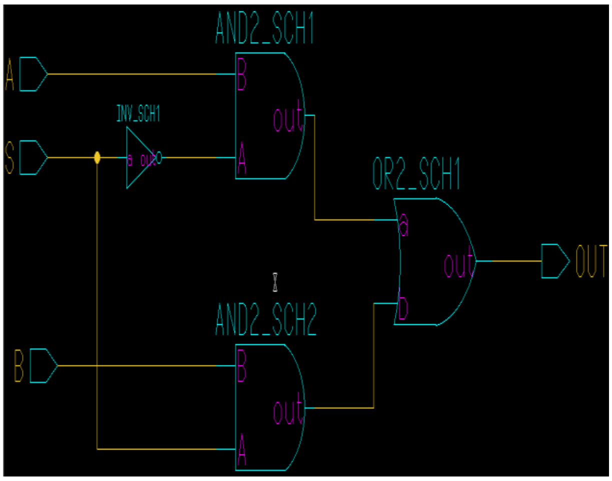

Fig. 17: Schematic Diagram of 2:1 Multiplexer Using CMOS Logic.

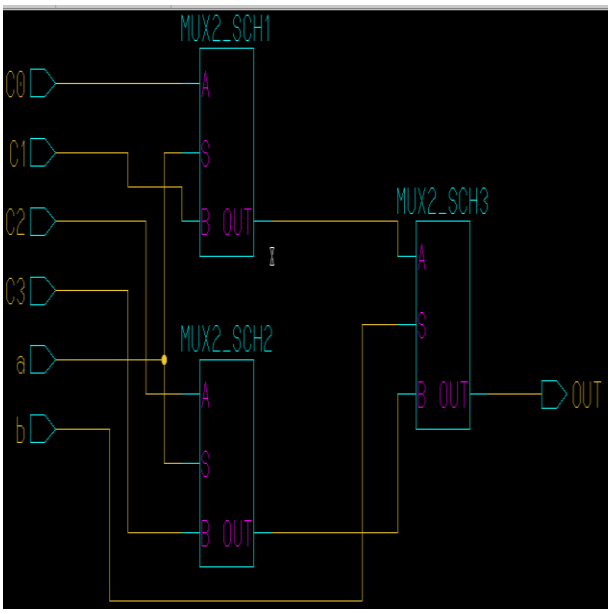

Fig. 18: Block Diagram of 4:1 Multiplexer Using CMOS Logic.

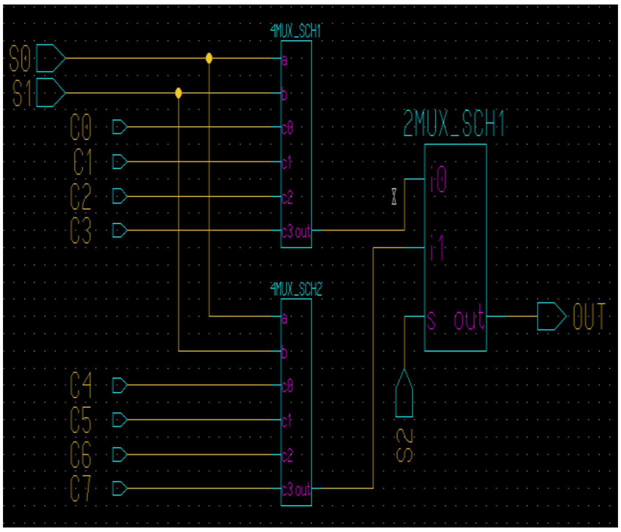

Fig. 19: Block Diagram of 8:1 Multiplexer Using CMOS Logic.

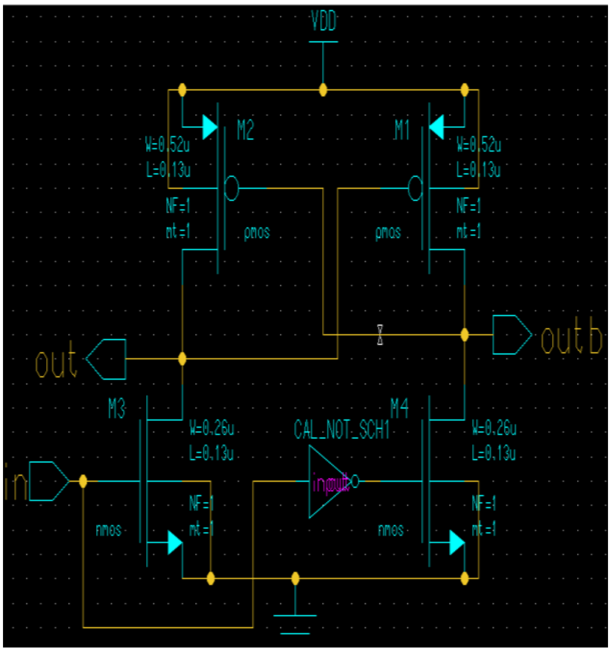

Fig. 20: Schematic Diagram of NOT Gate Using ECRL.

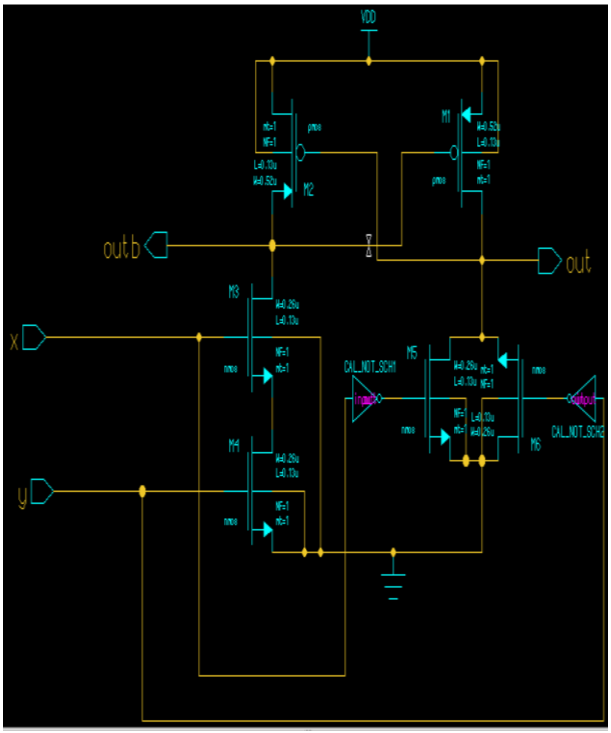

Fig. 21: Schematic Diagram of AND/NAND Gate Using ECRL.

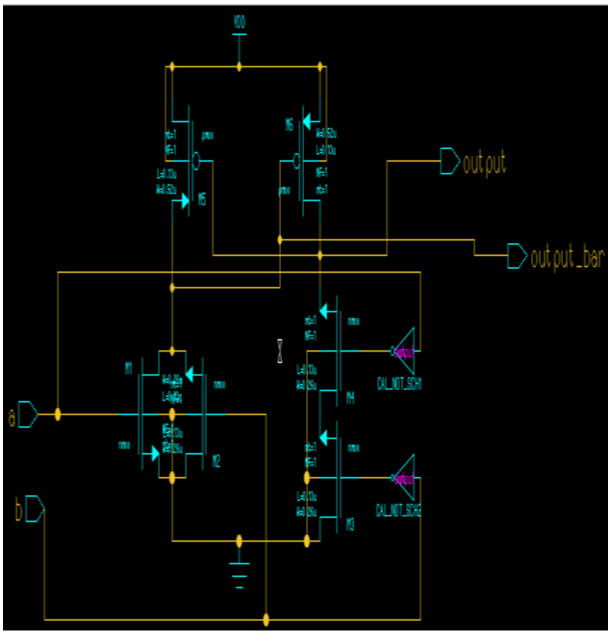

Fig. 22: Schematic Diagram of OR/NOR Gate Using ECRL.

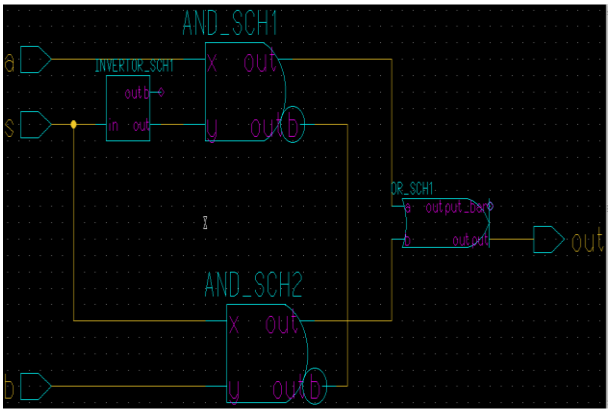

Fig. 23: Schematic Diagram of 2:1 Multiplexer Using ECRL.

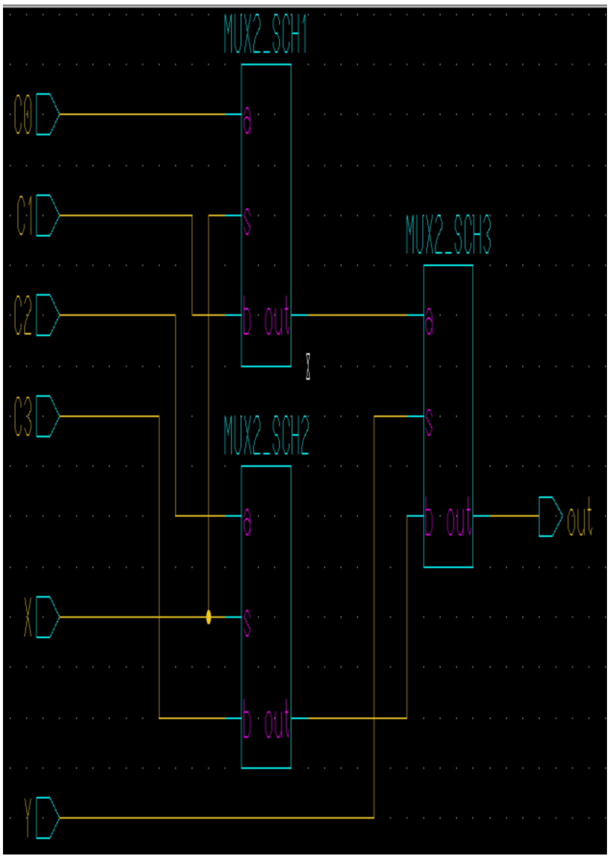

Fig. 24: Block Diagram of 4:1 Multiplexer Using ECRL.

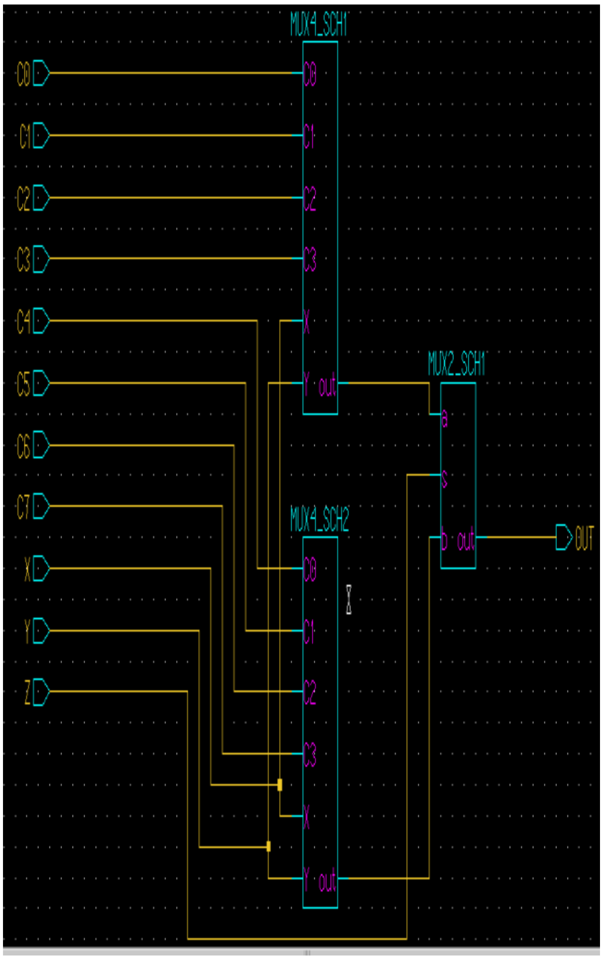

Fig. 25: Block Diagram of 8:1 Multiplexer Using ECRL.

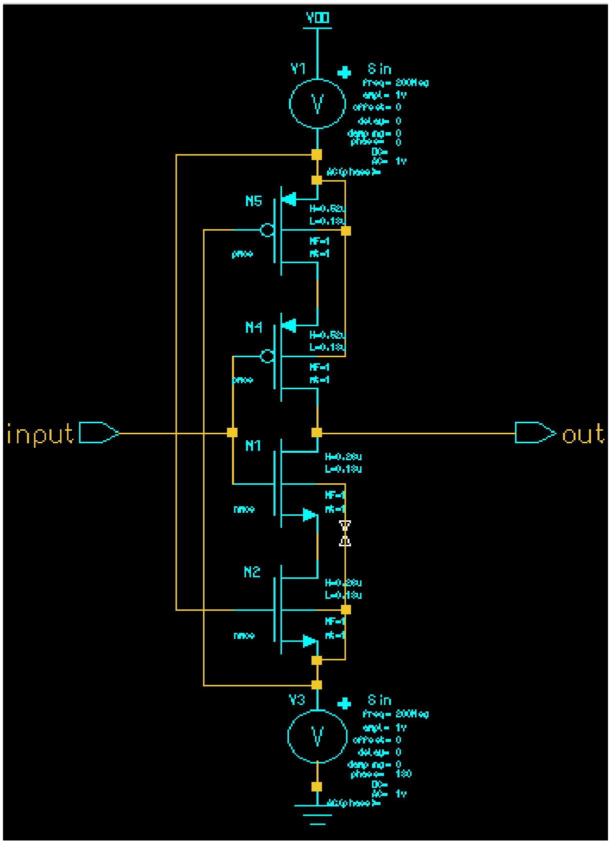

Fig. 26: Schematic Diagram of NOT Gate Using CAL.

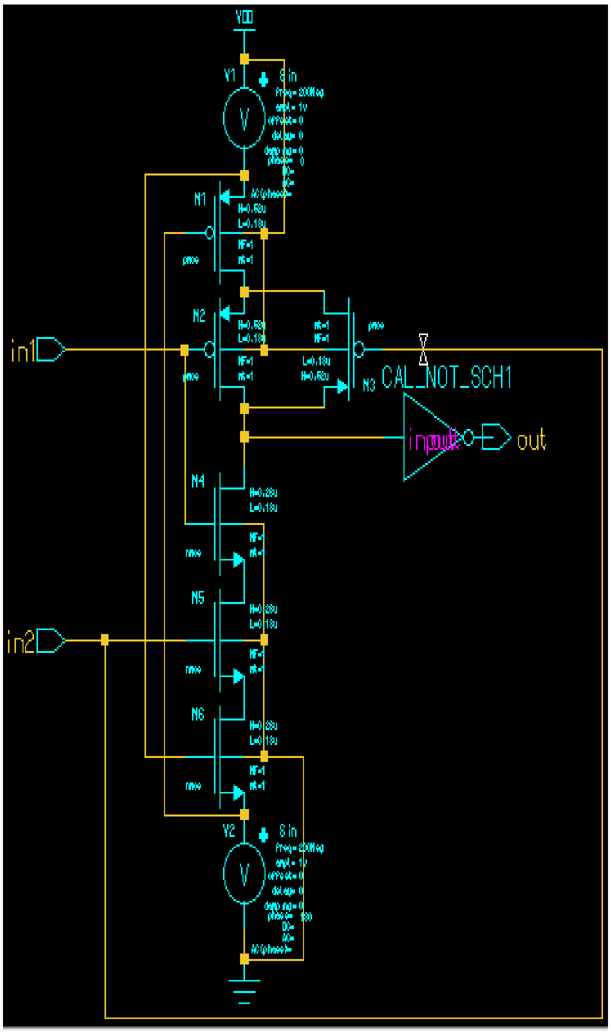

Fig. 27: Schematic Diagram of AND Gate Using CAL.

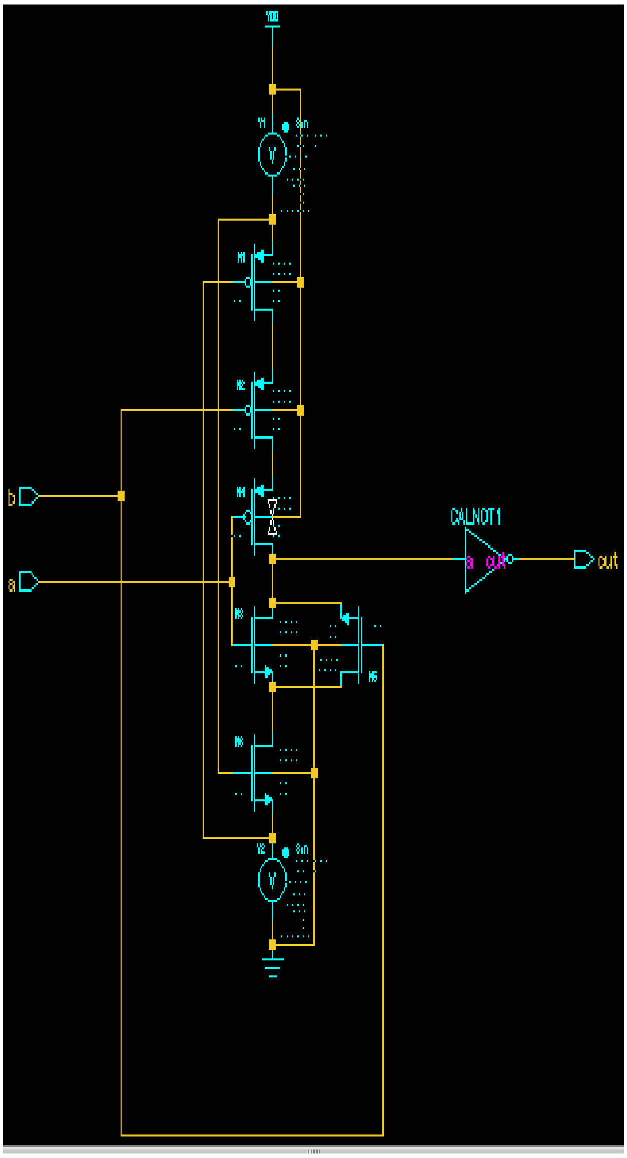

Fig. 28: Schematic Diagram of OR Gate Using CAL.

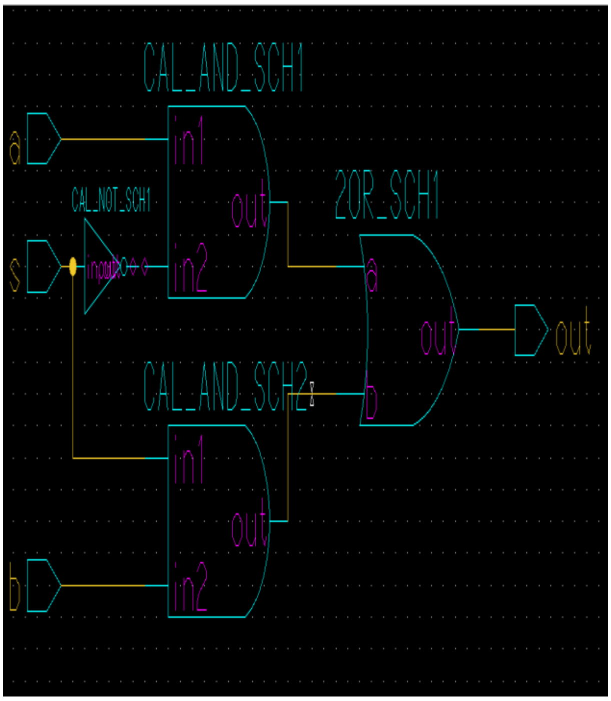

Fig. 29: Schematic Diagram of 2:1 Multiplexer Using CAL.

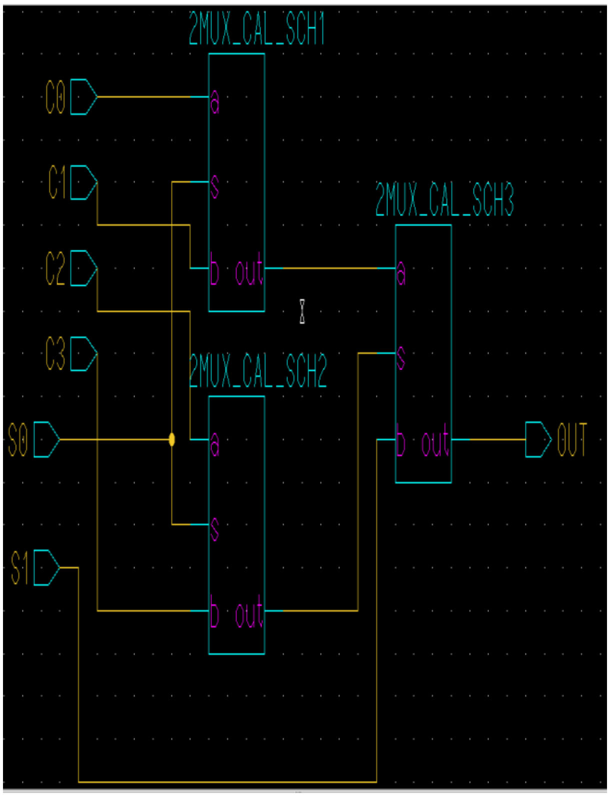

Fig. 30: Block Diagram of 4:1 Multiplexer Using CAL.

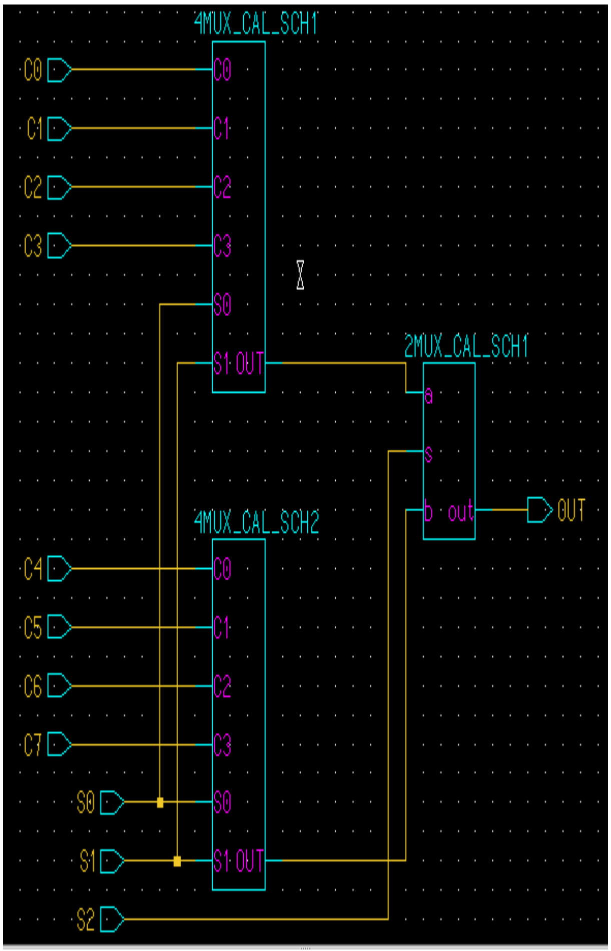

Fig. 31: Block Diagram of 8:1 Multiplexer Using CAL.

The simulation waveform of 4:1 Multiplexer using CMOS logic, ECRL, and CAL using Mentor Graphics are shown in figures 32 & 33 respectively.

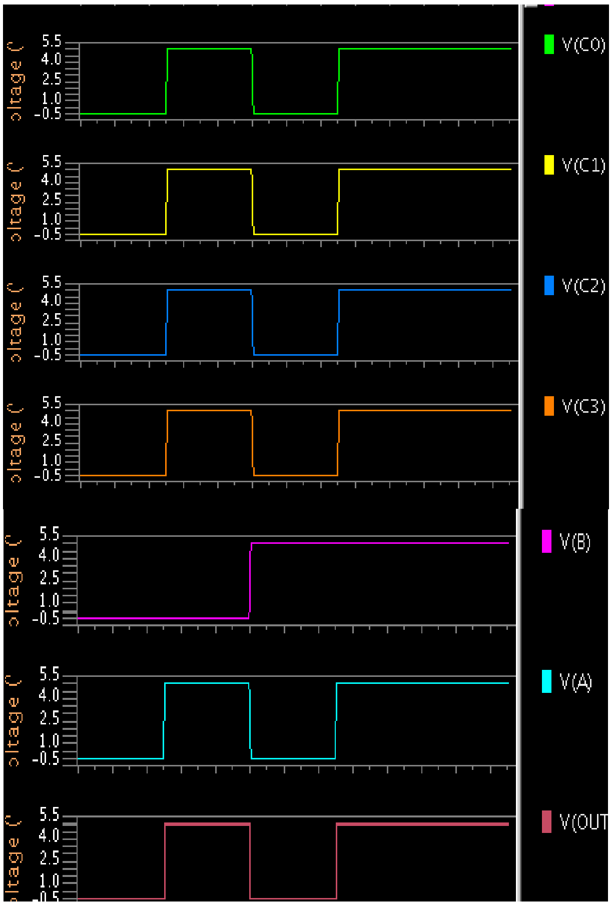

Fig. 32: Simulation Waveform of 4:1 Multiplexer Using CMOS Logic and ECRL.

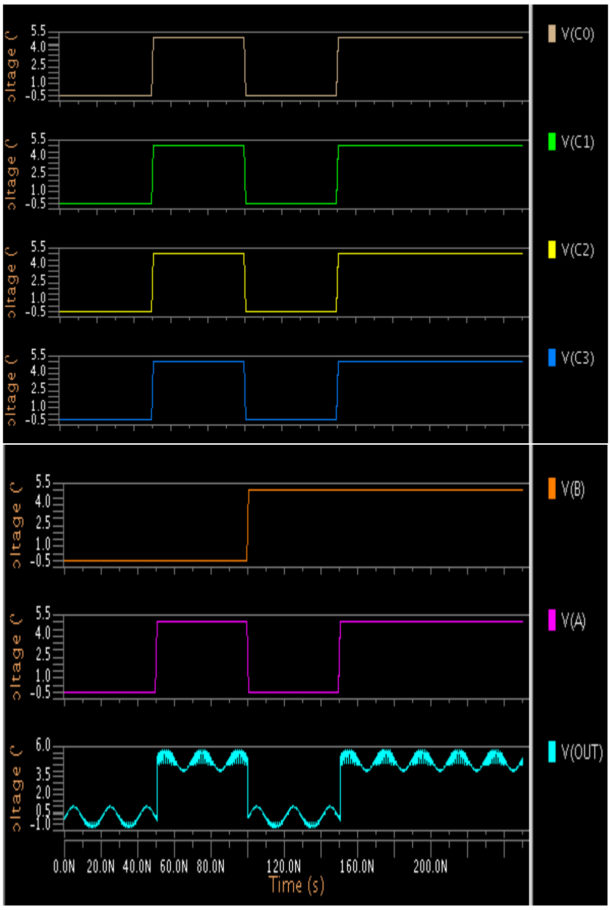

Fig. 33: Simulation Waveform of 4:1 Multiplexer Using CAL.

The comparison of power consumption of NOT, AND, and OR gates using CAL, ECRL, and CMOS logic is shown in table 1. The comparison of power consumption of 2:1, 4:1, and 8:1 multiplexer designs using CAL, ECRL, and CMOS logic is shown in table 2. The comparison of number of transistors required for 2:1, 4:1, and 8:1 multiplexer designs using CAL, ECRL, and CMOS logic is shown in table 3.

Table 1: Comparison of Power Consumption of NOT, AND, and OR Gates using CMOS Logic, CAL, and ECRL

Technology	NOT Gate (nw)	AND Gate (nw)	OR Gate (nw)
CAL	65.82	7.59	136.36
ECRL	136.44	139.28	268.14
CMOS Logic	65.84	7.59	1000.39

Table 2: Comparison of Power Consumption of 2:1, 4:1, and 8:1 Multiplexer Designs Using CMOS Logic, CAL, and ECRL

Technology	2:1 Multiplexer (µw)	4:1 Multiplexer (µw)	8:1 Multiplexer (µw)
CAL	0.28	0.84	1.96
ECRL	0.68	2.05	4.79
CMOS Logic	1.53	3.91	10.75

Table 3: Comparison of Number of Transistors required for 2:1, 4:1, and 8:1 Multiplexer Designs Using CMOS Logic, CAL, and ECRL

Technology	2:1 Multiplexer	4:1 Multiplexer	8:1 Multiplexer
CAL	34	102	238
ECRL	32	96	224
CMOS Logic	20	60	140

5. Conclusion

In this work, the three multiplexer designs are implemented using CMOS logic and two adiabatic logic methods i.e., Efficient Charge Recovery Logic (ECRL) and Clocked Adiabatic Logic (CAL). The 8:1 multiplexer using CAL reduces 59.08 % and 81.76 % power consumption compared to ECRL and CMOS logic respectively. The number of transistors required for CAL 8:1 multiplexer is 5.88% and 41.17 % more compared to ECRL and CMOS logic respectively. The designs are implemented using Mentor Graphic Tool (Technology: 130 nm, p MOS transistor W=0.52µ, L=0.13µ and n MOS transistor W=0.26µ, L=0.13µ, V_{DD}=5V).

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