International Journal of Engineering & Technology, 7 (3.1) (2018) 34-38

International Journal of Engineering & Technology

Website: www.sciencepubco.com/index.php/IJET

Research paper

Encoding Schemes for Reducing Transition Activity and Power Consumption in VLSI Interconnects-A Review

Vithyalakshmi.N[1]*, Nagarajan.P[2], Ashok Kumar.N[3], Vinoth.G.S[4]

1, 2,3Associate Professor, Sree Vidyanikethan Engineering College, Tirupati, Andhrapradesh.
[4]Technical Lead, Quest Global, Technopark, Trivandrum, Kerala.
**Corresponding author E-mail: vidhyavinoth@gmail.com*

Abstract

Low power design is a foremost challenging issue in recent applications like mobile phones and portable devices. Advances in VLSI technology have enabled the realization of complicated circuits in single chip, reducing system size and power utilization. In low power VLSI design energy dissipation has to be more significant. So to minimize the power consumption of circuits various power components and their effects must be identified. Dynamic power is the major energy dissipation in micro power circuits. Bus transition activity is the major source of dynamic power consumption in low power VLSI circuits. The dynamic power of any complex circuits cannot be estimated by the simple calculations. Therefore this paper review different encoding schemes for reduction of transition activity and power dissipation.

Keywords: *Static power dissipation, dynamic power dissipation, Self Transition, Coupling Transition, Encoding, CMOS, Low power.*

1. Introduction

Scaling of low power very large scale integrated circuits has boosted the sensitivity of CMOS circuits to produce large energy dissipation. Most of the energy is being washed out on the data buses and lengthy interconnects as dynamic power dissipation for charging and discharging of inter- wire capacitances and internal node capacitances. To improve on the whole performance of the application it is essential to control and reduce the technology scaling effects such as transition activity on data buses. One of the favorable techniques to increase the efficiency of the system is to encode the data on the bus. Hence this paper reviews several high performance encoding techniques to reduce transition activity, area and power dissipation.

2. Coding Scheme for Reduction of Power Dissipation

The importance of data coding technique is to reduce the data transition between data on parallel buses or neighboring data within the bus. Various research works carried out in reduction of power dissipation using data coding technique. Some of them are listed below.

A Stan & Burleson [7] developed bus invert coding for Low power I/O. In this scheme entire buses are used for encoding purpose and include a redundant bit along with bit line. This scheme is simple and effectively reduces the switching activity. The bus invert method was explained in the meticulous location of dynamic input and output power dissipation the identical method can be useful in any case where huge capacitances are occupied.

Yoo & Choi (1999) suggested how to design low power reconfiguration of FPGAs using interleaving partial bus invert coding. The authors suggested a bus encoding scheme which partitions the data sequence into several sub sequences. After that reconfiguring FPGA partial bus invert coding algorithm is used in each and every sub sequence to diminish the amount of data bus transitions. The proposed method is very useful in massive reduction of bus transitions compared with the conventional bus invert coding such as partial bus invert coding and beach coding.

Further, Partial bus invert coding is extended with decomposed bus invert coding technique for low power I/O buses recommended by Hong et al [32].In this work amount of bus transitions are reduced by innovative bus-invert coding scheme. Here, the bus positions are partitioned and each partitioned bus group is considered autonomously for reducing the overall transitions to get maximum efficiency. Results prove that the decomposed bus-invert coding scheme reduces the total number of bus transitions than the conventional and partial bus-invert coding algorithms in the same way.

Sotiriadis & Chandrakasan [10] developed Low power bus coding technique considering interwire capacitances. The energy dissipation with driving large data buses would be significant, when considering the growing inter wire capacitance. Transition reduction is taking in to least consideration for reducing power when the effects of inter wire capacitance are taken into consideration. If model designed with submicron technologies then proper coding techniques is proposed that can reduce the average power consumption on the bus.

Similar to this Youngsoo Shin et al (2001) suggested Partial bus invert coding scheme with power optimization techniques for ASIC devices. In this work two encoding algorithms were implemented. That is named as Partial Bus-Invert coding and Multiway Partial Bus-Invert coding. Firstly chosen subgroups of bus lines are encoded to avoid redundant inverted data or uncorrelated bus lines which are not included in the subgroup. In the extended method, partition a bus into several sub groups of buses by clustering with heavily correlated bus lines and then encode each sub bus individually.

Zhang et al (2002) developed bus invert coding for odd/even buses seperately for two phase transfer of buses with coupling effects. In this scheme the authors considered the numbered bus line and also coupling capacitances will charge and discharge by the activity of the neighbors. One line will be odd and the other neighbor line will be even. To reduce the coupling activity by independently controlling the odd and even bus lines with two separate lines, Odd Invert and Even Invert line to obtain significant reductions in power simply by comparing the coupling activity for the four possible cases of the Odd and Even Invert lines (00, 01, 10, 11), and then choosing the value with the smallest coupling activity to be transmitted on the bus. So after encoding, the transition for a pair of bus lines is still strongly dependents on data. The toggling sequences 01→10 and 10→01 result in 4 times more coupling energy dissipation than other coupling events.

Youngsoo & Takayasu (2002) have introduced model order reduction algorithm for analysis of power distribution in VLSI interconnects. The analysis and simulation effect induced by interconnects become progressively more essential as the scale of process technologies gradually shrinks. In this paper the power distribution study of interconnects is deliberated using reduced model algorithm. The difference between power utilization and the poles and residues of a transfer function is calculated and a simple accurate deriver model is also developed, for effective power computation.

Lee et al (2004) developed novel silent algorithm to reduce power dissipation in the serial bit stream. In this scheme, data is coded as XOR between the continuous data words. In the receiver side, original transmitted data word can be recovered by XOR of encoded word and previously decoded words.

Lin Xie et al [29] have developed partitioned bus coding for energy reduction. This paper proposes the bud partition scheme for the Transition pattern Coding (TPC). The genetic algorithm based approach is used. A closed form of expression is derived to calculate the energy dissipation for the partitioned bus with TPC coding. The bus lines are shuffled and portioned in order to minimize the total energy reduction. The resulted portioned bus coding reduces the encoding and decoding complexity.

Youngsoo & Junghyup (2006) have introduced power analysis of VLSI interconnect with RLC tree models and model reduction. The existence of wire resistance ignored by the lumped capacitance model, which has been estimate the charging and discharging power consumption of CMOS circuits. During this study it was revealed that about 20% of the power is consumed in the wire resistance of the buffered global interconnect, when an interconnect is modeled with RC tree networks. The power distribution analysis of interconnect with RLC tree networks based on a reduced order model. The individual analysis of the driver circuits and the role of interconnect is much constructive to realize the sources of energy dissipation.

Massimo et al [26] introduced energy consumption in RC tree circuits. In this paper, resistance, capacitance tree networks are modeled in terms of their energy consumption associated with an input transition. Based on Single pole approximation, the energy consumption circuits are modeled and equivalent time constant is also analytically derived from an exact analysis for very slow and very fast I/P transitions. Then this model is extended to arbitrary values of the input rise time by exploiting some intrinsic properties of RC tree networks. This method is fully analytical and leads to closed-form results.

Transition skewing coding scheme proposed by Akl & Bayoumi [1] reduces power dissipation and area. This scheme deals with area, noise, cross talk, peak energy and signal integrity and switching and leakage power. The authors used 90nmtechnology to simulate. The encoded bus is compared against a standard bus and a bus with shields inserted between every two wires. The encoding and decoding latencies are also analyzed. Simulations show that transition skew coding is efficient in terms of energy and area with low encoding and decoding latency overhead. This work has been further extended in 90nm encoding scheme considering 2 GHz global clock frequency.

Variable cycle transmission for on chip interconnects algorithm developed by Kalyan et al (2008). It proposes a scheme which exploits both dynamic voltage scaling and variable cycle transmission mechanisms for minimizing on chip interconnect energy consumption. Transmit data using variable cycle transmission method, based on the delay saving achieved through variable cycle transmission method at frequent intervals. To obtain energy saving by scale the voltage and frequency.

Verma & Kaushik [4] have reviewed and analyzed various encoding techniques for reducing delay, energy dissipation and crosstalk effects in VLSI interconnect. From this paper we can understand how the encoding techniques are formulized to get the minimum energy loss circuits. Crosstalk is induced by simultaneous switching activity of adjoining bus lines. This is the main cause for the malfunctioning of VLSI chip. Most of the occasions due to intensified crosstalk affect the system delay and power dissipation. Switching activities are reduced all the way through coupled transmission line results in huge reduction of power dissipation. The researchers consequently focus on encoding scheme that reduces the transitions of the signals.

Venkateswara & Tilak [6] analyzed crosstalk noise effect in system on chip then developed a innovative bus encoding technique to decrease the obtained issue. This coding scheme proposes how to reduce the crosstalk outcomes in system on chip. since the system is submicron technology circuit layouts become small, internal components closer together, so the coupling capacitance inflated between nodes. In the meantime, substrate capacitance is less then interconnections and circuit delays are decreased as transistors become smaller. Substrate capacitance is the foremost effect for circuit geometries higher than 0.25 micron. Conversely with geometries at 0.18 micron and below, the coupling capacitance becomes considerable.

Karunamoy & Subhashis [30] developed a novel method for analysis of power consumption in VLSI global interconnects. The investigation of effects induced by interconnects become more important as the technologies scale down. The analysis method based on a reduced order model and discrete domain Z transform. Power dissipation can be computed expertly in Z-domain using an algebraic equation, instead of inappropriate integration in time domain. The theoretical conclusion relies on the pole and residues of transfer function can be used in any class of model order reduction practice.

Padmapriya [16] developed modified bus invert scheme for low Power VLSI circuits in Deep Submicron technology. In this work peak power is a most critical design factor as it determines the thermal and electrical limitations of designs, cost of the system, precise battery type size and weight, component and system packaging and heat sinks, and aggravates the resistive and inductive voltage drops. Therefore it is essential to have the peak power in control. The cross talk is dependent on the data transition patterns on the bus. As a result the proposed bus invert encoding design is suitable for reducing the power dissipation and cross talk delay in VLSI circuits.

Sanjay et al (2013) developed Reduction of Sub threshold Leakage Current in MOS Transistors. Here NMOS and PMOS are simulated in different layout techniques show considerable reduction in sub threshold leakage and junction leakage currents by the use of double-finger and four-finger techniques. Junction and subthreshold leakage reduction is observed by varying different parameters in single NMOS and PMOS transistors. So the memory is fabricated by large number of PMOS and NMOS transistors and also can be reduce leakage current in memory.

Nima et al [17] introduced encoding scheme for network-on-chip to reduce energy consumption in data buses. By using this encoding technique power can be reduced in the links of a NoC. Analysis carried out on both fake and real traffic scenarios show the efficiency of the design. This scheme used to minimize not only the switching transition, but also the coupling switching activity which is mainly responsible for link power dissipation in the deep submicron meter technology regime

Amit & Jyoti (2014) developed an energy efficient advanced low power CMOS design to reduce power consumption in deep Submicron technologies in CMOS circuit. Here energy efficient and eco friendly techniques were focused for calculation of power-dissipation in various components and also the determination of different ways to reduce the total power consumption in a CMOS device. This technique has less power dissipation than the conventional CMOS design style.
Kanchan & Deshmukh (2015) proposed Power Optimization of Combinational Quaternary Logic Circuits. By the need of interconnections design of the binary logic circuits is restricted. Interconnections increase energy consumption, area and delay in digital CMOS circuits. Multiple valued logic full adder can decrease the average power needed for transitions and reduces the number of required interconnections using unique encoding technique.
Prabhakaran & Shenbagavelrajan [14] have developed modified data encoding and decoding scheme for data transmission in network-on-chip. The main cause of dynamic power dissipation in network on chip is due to coupling capacitance and self-transition effects. The self-transition is decreased by examine the switching activity and then the coupling technique is included with the routed network, which is encoded by the network interface before they are injected in the network and are decoded by the destination network interface. The encoding scheme on a set of data showing that it is possible to reduce the power consumption for both self and coupling switching activity in an inter router links.

3. Coding Scheme for Reduction of Self and Coupling Transition

In CMOS circuits most power is dissipated as dynamic power due to switching transition during charging and discharging of load capacitance. Transition activity is classified in to self transition and coupling transition. In this field most of the research work analyzing coupling transition, self transition and combined both self and coupling transition techniques to reduce the power dissipation.
Sumant et al [8] introduced a coding frame work for low power address and data busses presents a source coding frame work for design of coding schemes to reduce transition activity. In this frame work a data source is first passed through a decorrelating function f1 ,Next, a variant of entropy coding function f2 is employed, which reduces the transition activity. In this scheme incremental xor (inc-xor) method for address bus and probabilistic based mapping xor (xor-pbm) method for data bus is used to encode the data to reduce transition activity.
Vijay & Keshab [3] have developed limited weight coding with codeword slimming technique to reducing bus transition activity. In this work introducing redundant information on data lines to reduce number of transitions data busses. A new coding technique that leads to tremendously reduce bus transitions to the transmission of lower bound depending on the redundancy of bits considered. So there is a huge reduction of power dissipation over an uncoded information.

Ki-Wook et al (2000) proposed coupling driven signal encoding scheme for low power design. Effects of coupling an on-chip interconnects ought to be addressed in ultra deep submicron and system-on-a-chip designs. Here coupled switching activity which dominates the on-chip bus is minimized by introducing low-power bus coding technique. Hardware overhead diminished by the coupling-driven bus inverts method use slim encoder and decoder architecture .

Jorg & Harish [31] have considered the coupling effects in low power deep sub micron designs using an adaptive address bus coding technique. The source is a physical bus model that quantifies coupling capacitances. Due to large group of buses and deep sub micron technology where the self and coupling capacitances among bus lines are dominant factor for energy consumption of interconnects starts to have a major impact on a systems entire energy dissipation. The A2BC encoding method is applied in the two stages of ACCS and LSIS.
Madhu et al [24] designed chips for low power applications is one of the most important challenges faced by the VLSI fabricators. Because the power dissipated by I/O pins of CPU is a significant source of power consumption. Dynamic coding technique for low power data bus encoding scheme developed for reducing switching activity on external buses. This technique considers two logical groupings of bus lines, each being a permutation of the bus and energetically chooses the grouping which yields the minimum number of transitions.

Naveen et al [18] has implemented a new deep submicron bus encoding for low Energy. In present low power digital circuits the total amount of power scattered to wires is increasing day by day. Reducing power dissipation in wires plays a major role in low power applications. Switching transitions meet the expense of momentous energy loss in deep sub-micron buses. As a conclusion this method reduces the coupling transitions activity for submicron technologies compared to the usual un-coded data lines. This process is adaptive it decreases the signal transmission for all sorts of data streams.
Menon et al [27] introduced switching activity minimization in combinational logic design. The reduction of switching activity in combinational logic design an algorithmic way using karnaugh map has been proposed which modifies the normal optimal solution obtained from k-map to reduce its switching activity. More than 10% reduction in switching activity has been observed using this method. The final solution gives a good tradeoff between cost and power consumption.
Tina et al (2004) have developed deep sub micron bus invert coding presents a deep sub micron bus invert coding for on chip parallel data buses. Similar to bus invert coding technique it is used to realize low complexity encoding and decoding circuitry, and with a complexity that scales linearly with the bus width. By introducing redundancy it is possible to reduce the energy dissipation in on chip parallel data buses.
Muroyama et al introduced a variation aware low power coding methodology for tightly coupled buses. Variable length coding is proposed to reduce the self capacitance and switching power. Probabilistic information is used to for assigning the code. The smaller length code is assigned for more frequent data, in which the major sources of the power consumption are the activities on the signal lines and the coupling capacitances of the lines[20].
Avnish et al (2006) proposed an adaptive low power bus encoding based on weighted code mapping. The Weighted code mapping considers the self and coupling capacitance of the bus wires. Window-based adaptive coding method is proposed to improve the energy saving by adaptively changing the code mapping for different data probabilistic characteristics. The authors extended their work in another encoding scheme is called an adaptive hybrid low power bus encoding technique (2006), in which the WCM algorithm is combined with delayed bus encoding technique will further reduce the bus energy.
Sainarayanan et al [13] introduced coding for minimizing energy in VLSI interconnects. The main target of VLSI designers is to minimize the switching activity on the on-chip buses. Authors introduced a bus encoding technique which minimizes both self and coupling transition activity to curtail the global power consumption. Simulation results shows that the proposed method is suitable for the continually shrinking technology and low power VLSI applications.
Madhu [23] introduced CMOS process technology scaling to deep submicron level. Delay in long on-chip buses is becoming one of the main performance limiting factors in high speed designs. Propagation delay is most important when adjacent wires are transitioning in opposite direction as compared to transitioning in the same direction.. This work proposes a technique, namely, selective shielding, to eliminate crosstalk transitions. Selective shielding

significantly reduces the number of extra wires which gives a lower bound on the number of wires required to encode n-bit data
Shankaranarayana & Yogitha [11] developed universal rotate bus invert coding for Low power VLSI circuits. Switching activity is the major issue that affects the dynamic power. Reduction of switching transitions in the data busses attains impacts on the bus width and bus capacitance. Encoding scheme suggested in this paper firstly the data is coded with either rotate left or rotate right algorithm. Secondly the coded data lines compared with the original un-coded data line to calculate the amount of transition between the bus lines. Finally least transition count encoding scheme will be taking in to consideration for further transmission .This work has given better performances than the existing methods like as shift invert coding and bus invert coding for sample data in terms of switching activity, without the need for any extra calculation and design.
Verma & Kaushik [5] developed a bus encoding scheme for RC coupled VLSI interconnects to reduce crosstalk and power dissipation. The crosstalk is caused by both self and coupling transition activities that are considered when there is a transition on the bus lines or between neighboring bus lines. To enhance the performance of the system design is to minimize the simultaneous switching activities of the entire bus lines. Several algorithms and analysis are carried out by researches to rectify the problems such as power dissipation, delay and crosstalk reduction. Encoding is the most unbeaten and trendy method for enhancing the activities of on chip buses. The transition reduction improves performance in power dissipation, coupling activity and delay in on-chip buses.

Nagendra Babu et al [21] proposed Bus encoder for crosstalk avoidance in RLC models. In recent years most encoding methods deal with only RC modeled VLSI interconnects. In deep submicron (DSM), inductive effects have increased due to faster clock, smaller rise times and longer on-chip interconnects. All these raise power dissipation, propagation delay and crosstalk. So, this research introduces an efficient Bus Encoder method using Bus Inverting (BI). This proposal reduces both crosstalk and power dissipation in RLC modeled interconnects which makes it suitable for current high-speed low-power VLSI interconnects.
Padmapriya [15] proposed for low power bus encoding for deep sub Micron VLSI circuits. In recent year's low power and power awareness has become a major driving force especially due to portable electronics and the growing cost of the power dissipation. DSM bus power dissipation is directly related to the switching activity of the coupling capacitance that exist between the bus lines and also the switching activity of the self capacitance present between the bus interconnect and the ground. The technique used here is to reduce the switching activity of both self and coupling capacitances through encoding the data on buses.
Mullainathan & Ramkumar [19] proposes switching reduction through data encoding techniques in Network on chip. Here encoding scheme is used to reduce the power dissipation and the energy consumption of the communication system in NoC. On-chip interconnect has more significant fraction of the overall system power/energy budget. So in the definition of new methodologies and techniques aimed at optimizing the on chip communication system not only in terms of performance but also in power. The method followed is, encoding the packets before they are injected into the network in such a way as to minimize both the switching activity and the coupling transition effects in the NoC's links which represent the main factors of power dissipation.
Devendra Kumar et al [34] have introduced FDTD based transition time dependent crosstalk analysis for coupled RLC interconnects based on FDTD analysis of transition time effects on crosstalk. The investigation carried out is for equal and unequal transition times. The unequal rise time effects are also equally important because, it is common to have mismatch in the rise time of the signals transmitting through different wire length. As an example, two distributed RLC lines coupled inductively and capacitive are considered. The FDTD method is followed because it gives accurate results and carries time domain analysis of coupled lines.

4. Conclusion

In this review paper, various encoding schemes have been reviewed. it is observed that with the rise in VLSI technology , complexity of encoding have increased . The main emphasis of different researches is to reduce the signal transition in the bus. Area and different type of transition activity like self transition and coupling transition are the main cause of dynamic power dissipation. Researchers have suggested various encoding methods to reduce self and coupling transition effects from micrometer to nanometer technology.

References

[1] Akl, CJ & Bayoumi, MA 2008, 'Transition skew coding for global
[2] on chip interconnects', in IEEE Transaction on VLSI systems, vol.
[3] 16, no. 8, pp. 1091-1096.
[4] Verma, SK & Kaushik, BK 2013, 'Crosstalk reduction using bus
[5] encoding in RLC modeled interconnects', European journal of
[6] scientific Research, vol. 110, no.1, pp. 106-118.
[7] Vijay Sundararajan & Keshab K Parhi 2000, 'Reducing bus transi
[8] tion activity by limited weight coding with codeword slimming',
[9] Proceedings of the 10th great lakes symposium on VLSI, pp. 13- 16.
[10] Verma, SK & Kaushik, BK 2010, 'Encoding schemes for reduction
[11] of power dissipation, crosstalk and delay in VLSI interconnects: A
[12] Review', International journal of Recent trends in Engineering and
[13] technology, vol. 3, no. 4, pp. 74- 79.
[14] Verma, SK & Kaushik, BK 2012, 'A bus coding method for cross
[15] talk and power reduction in RC coupled VLSI interconnects', In
[16] ternational journal of VLSI design & Communication systems, vol.
[17] 3, no. 2, pp.
[18] Venkateswara Rao, J & Tilak, AVN 2011, 'A Bus encoding to
[19] reduce crosstalk noise Effect in system on chip', International
[20] Journal of VLSI design & Communication Systems (VLSICS)
[21] vol.2,no.2, pp. 110-117
[22] Stan, MR & Burleson, WP 1995, 'Bus- Invert coding for low power
[23] I/O', IEEE Trans. On VLSI, vol. 3, pp. 49-58.
[24] Sumant Ramprasad, Naresh R Shanbhag & Ibrahim N Hajj 1999,
[25] 'A Coding frame work for low power address and data busses',
[26] IEEE Transactions on very large scale integration systems, vol. 7,
[27] no.2, pp. 212-221.
[28] Shikha Singh & Sulochana Verma, V 2012, 'Crosstalk noise and
[29] delay reduction in VLSI interconnects', International journal of
[30] advanced technology&Engineering Research (IJATER), vol. 2, no.
[31] 2, pp. 105-109.
[32] Sotiriadis, PP & Chandrakasan, A 2000, 'Low power bus coding
[33] techniques considering inter-wire capacitances', Proc. IEEE Cus
[34] tom Integrated Circuits Conference, pp. 507-510.
[35] Shankaranarayana Bhat, M & Yogitha Jahnavi, D 2012, 'Universal
[36] rotate invert bus encoding for Low power VLSI', International
[37] Journal of VLSI design & Communication Systems (VLSICS) vol.
[38] 3,no.4, pp. 97- 109.
[39] Sathish, A, Madhavi Latha, M & Lalkishor, K 2011, 'An efficient
[40] switching activity reduction technique for on chip data bus', In
[41] ternational Journal of Computer Science Issues, vol. 8, Issue 4, no.
[42] 2, pp. 407-413.
[43] Sainarayanan, KS, Ravindra, JVR, Kiran T Nath & Srinivas, MB
[44] 2006, 'Coding for minimizing energy in VLSI interconnects', The
[45] 18th International Conference on Microelectronics, pp. 166-169.
[46] Prabhakaran, K & Shenbagavelrajan, B 2015, 'Modified data
[47] encoding and Decoding scheme for data transmission Technique
[48] in NoC', International journal of research and science & technolo
[49] gy,vol.1, no. 1, pp. 340-348.
[50] Padmapriya, K 2013, 'Low power bus encoding for deep sub Mi
[51] cron VLSI circuits', International journal of electrical and electron
[52] ic engineering & telecommunications, vol. 2, no. 2, pp. 68-72.
[53] Padmapriya, K 2013, 'Modified bus invert technique for low Pow
[54] er VLSI design in DSM technology', International journal of elec
[55] trical and electronic engineering & telecommunications, vol. 2, no.
[56] 2, pp. 54-57.
[57] Nima Jafarzadeh, Maurizio Palesi, Ahmad Khademzadeh & Ali
[58] Afzali-Kusha 2014, 'Data Encoding Techniques for Reducing Ener
[59] gy Consumption in Network-on-Chip', IEEE Transactions On Very
[60] Large Scale Integration Systems, vol. 22, no. 3, pp. 675- 685.
[61] Naveen K Samala, Damu Radhakrishnan & Baback Izadi 2004, 'A
[62] Novel Deep Sub-micron Bus Coding for Low Energy', In Proceed
[63] ings of the International Conference on Embedded Systems and

[64] Applications, pp. 25-30
[65] Mullainathan, SR & Ramkumar, S 2014, 'Switching reduction
[66] hrough data encoding techniques in NoC', Discovery, vol. 23, no. 76,
pp. 38- 41.
[67] Muroyama, M, Tarumi, K, Makiyama, K & Yasuura, H 2005, 'A
[68] variation aware low power coding methodology for tightly coupled
[69] buses', in proceedings of Asia and south pacific Design Automation
[70] Conference , pp. 557-560.
[71] Nagendra Babu, G, Deepika Agarwal, Kaushik, BK & Manhas, SK
[72] 2012, 'Bus encoder for crosstalk avoidance in RLC modeled inter
[73] connects', International journal of VLSI design & Communication
[74] systems, vol. 3, no.2, pp. 29-39.
[75] Lindkvist, T, Lofvenberg, J & Gustafsson, O 2004, 'Deep sub-micron
[76] bus invert coding', in Proceedings of the Sixth Nordic Signal
[77] Processing Symposium, pp. 133-136.
[78] Madhu Mutyam 2007, 'Selective shielding A Crosstalk free bus
[79] coding technique', IEEE/ACM Conference on Computer aided de
[80] sign,pp. 618-621.
[81] [24] Madhu, M, Srinivas Murty, S & Kamakoti, V 2003, 'Dynamic cod
[82] ing Technique for Low-Power data bus', Proceedings of the. IEEE
[83] computer Society Annual Symposium on VLSI.
[84] Malathi, SR & Ramya Asmi, R 2013, 'Reduction of Bus Transition
[85] for compressed code systems', International journal of VLSI design
[86] & Communication systems, vol. 4, no. 1, pp. 123- 134.
[87] Massimo Alioto, Gaetano Palumbo & Massimo Poli 2006, 'Energy
[88] consumption in RC tree circuits', IEEE transaction on very large
[89] scale integration systems, vol. 14, no. 5, pp. 452- 461.
[90] Menon, RV, Chennupati, S, Samala, NK, Radhakrishnan, D & Iza-di,
[91] B 2004, 'Switching Activity Minimization in Combinational Logic
[92] Design', Proceedings of the International Conference on Embedded
[93] Systems and Applications, pp. 47-53.
[94] Lekatsas, H, Henkel, J & Wolf, W 2005, 'Approximate arithmetic
[95] coding for bus transition reduction in low power designs', IEEE
[96] Transactions on Very Large Scale Integration Systems, vol. 13, no.
[97] 6, pp. 696-706.
[98] Lin Xie, Peiliang Qiu & Qinru Qiu 2005, 'Partitioned Bus Coding
[99] for Energy Reduction', Asia and south pacific Design Automation
[100] conference – ASP-DAC, pp. 1280-1283.
[101] Karunamoy Chatterjee & Subhashis Das 2012, 'A Novel method for
[102] analysis of power consumption in VLSI global interconnects', Inter
[103] national journal of scientific and Research publications, vol. 2, issue
[104] 1, pp. 1-5.
[105] Jorg Henkel & Haris Lekatsas 2001, 'Adaptive Address bus coding
[106] for low power deep sub-micron designs', Design Automation confe
[107] rence proceeding IEEE publication, pp. 744-749.
[108] Hong, S, Chung, K, Narayanan, U & Kim, T 2000, 'Decomposition
[109] of bus invert coding for low power I/O', Journal of circuits systems
[110] and computers, vol. 10, no. 1-2, pp. 101-111.
[111] Gopala Krishnan, M & Rachelin Sujae, P 2014, 'System Design for
[112] Encoding and Decoding to Minimize the Crosstalk in VLSI Circuits',
[113] Middle-East Journal of Scientific Research, vol. 20, no. 12, pp. 2405-2411.
[114] Devendra Kumar Sharma, Brajesh Kumar Kaushik & Sharma, RK
[115] 2014, 'FDTD based transition time dependent crosstalk analysis for
[116] coupled RLC interconnects', Journal of semiconductors, vol. 35, no.
[117] 5, pp. 1-5.
[118] Brahmbhatt, AR, Zhang, J, Wu, Q & Qiu, Q 2006, 'Adaptive low
[119] power bus encoding based on weighted code mapping', in Proceed
[120] ings of IEEE international symposium on circuits and systems.
[121] Brahmbhatt, AR, Zhang, J, Wu, Q & Qiu, Q 2006, 'Low power bus
[122] encoding using an adaptive hybrid algorithm', in Proceedings of the
[123] 43rd Annual conference on Design Automation, pp. 987-990.
[124] Akl, CJ & Bayoumi, MA 2007, 'Transition skew coding A power
[125] and area efficient encoding technique for global on chip intercom
[126] nects', IEEE Design Automation conference, pp. 696-701.