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Research paper

Design of High frequency Voltage Controlled Oscillators for Phase Locked Loop

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Abstract

This paper presents the analysis of various oscillators that generate high frequency of oscillation for high speed communication, clock generation and clock recovery. The Ring oscillator and the Current Starved Voltage Controlled Oscillator(CSVCO) (for 5-stagewithout resistor and with resistor) have been implemented using the Cadence Virtuoso tool in 90 nm technology. The generated frequency of oscillation and the power consumption values of the voltage controlled oscillators have been calculated after inclusion in the PLL, and were also compared to identify the most suitable voltage controlled oscillator for a given application.

Keywords: *Current Starved VCO, PLL, Ring VCO.*

1. Introduction

The Phase Locked Loop(PLL) is an integral part of all communication systems. It is a closed loop control system that generates an output signal proportional to the phase of the input signal. It is primarily used for clock synthesis and synchronisation. The Voltage controlled oscillator(VCO) is one of the most vital part of the PLL design as the overall performance characteristics of the PLL is judged based on the performance of the VCO. This paper deals with the performance analysis of the Ring VCO and the Current Starved VCO comprising of both 5 stages and 7 stages.

The section-wise division of this paper is as follows. Section 2 consists of 2 subdivisions. Section 2.1 introduces the concept and circuitry behind the working of Ring VCO. Section 2.2 focuses on a specific type of Ring VCO called the Current Starved Ring VCO of 5 stages. Two variants of the 5 stage VCO, that is one without source degeneration and another with source degeneration are discussed. Section 3 covers the design equations governing the 5 stage Current Starved VCO with source degeneration. Section 4 covers the schematic and simulation results of all the designed VCOs and compares their performance. Section 5 concludes on the preferred design of voltage controlled oscillator for PLL.

2. Concept and Design

2.1 Ring VCO

The Ring VCO is a feedback system that consists of several delay stages to achieve the required frequency of oscillation. In this paper single ended ring VCO design is implemented.

A single-ended ring VCO comprises of odd number of delay stages. This paper focuses on the 3 stage ring VCO whose circuit is as shown below in Figure1.[3]

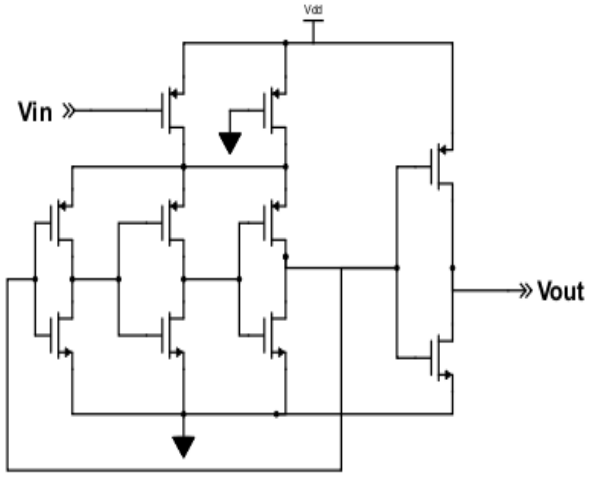

Fig. 1: Ring VCO

Each delay stage consists of two MOSFETs i.e., a PMOS and an NMOS connected to form an inverter. For instance, the MOSFETs M1 and M2 form one delay stage. The gate of M4 is grounded to initiate the oscillation and that of M3 is triggered by a control voltage to control the frequency of output oscillation. In an N stage ring VCO, each of the delay stages in the ring gives a phase shift of π / N and the last inverter stage gives an additional phase shift ofπ.

2.2 Current Starved Ring VCO

This section explains an improved design of Ring VCO called the Current Starved Ring VCO. In the Current Starved design, unlike

the basic design of the Ring VCO, there are four MOSFETs in each delay stage as shown in Figure 2.[8]

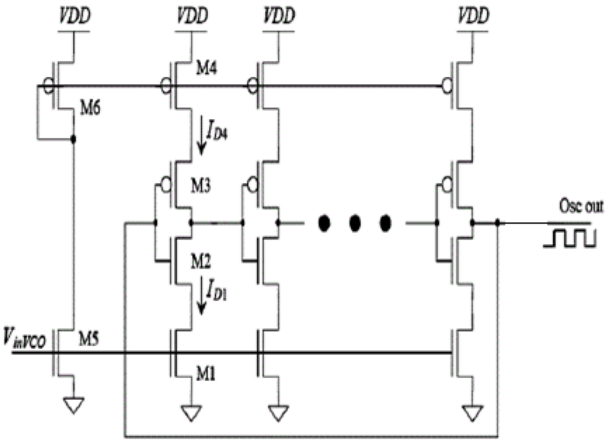

Fig. 2: Current Starved Ring VCO

In Figure2., The PMOSM3 and NMOSM2 form the inverter, while PMOSM4 and NMOSM1 operate as current sources that limit the current available to the inverter i.e., the inverter is starved for current. The current in the NMOS M5 and PMOS M6 are mirrored at each inverter stage.

2.2.1 Five Stage Current Starved Ring VCO

The circuit shown in Figure3 is a5 stage Current Starved Ring VCO. There are 5 delay stages.

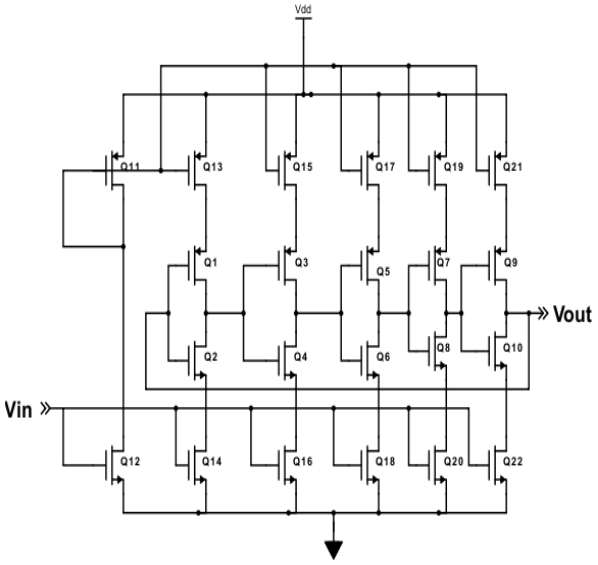

Fig. 3: Five stage CSVCO

In the above circuit, the drain current depends non-linearly on the overdrive voltage. Thus, this circuit is prone to high amount of non-linear distortion with changes in working conditions like temperature.
These drawbacks can be overcome by source degeneration caused by inclusion of a resistor in the design.

2.2.2 Five Stage Current Starved Ring VCO with Resistor

The circuit in Figure4 represents the modified 5stage Current Starved Ring VCO after source degeneration.

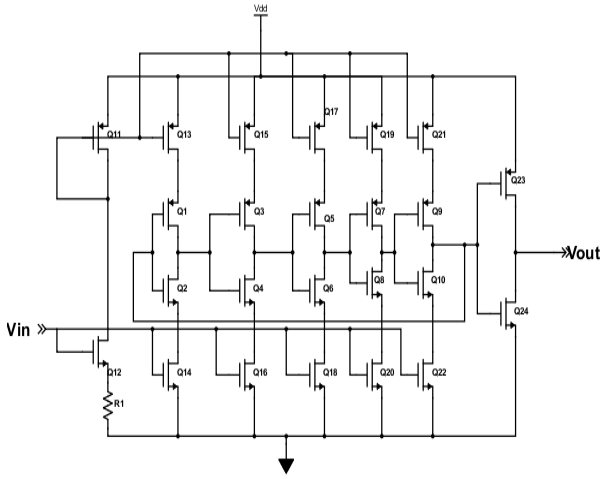

Fig. 4: Five stage CSVCO with resistor

Due to the inclusion of a resistor between the source and ground terminal as shown in Figure 4, the drain current now depends linearly on the overdrive voltage. This circuit now works independent of MOSFET device characteristics and exhibits an overall linear and stable behaviour.

3. Design Equations

This section covers the design equations that govern the working of 5 stage CSVCO with resistor.

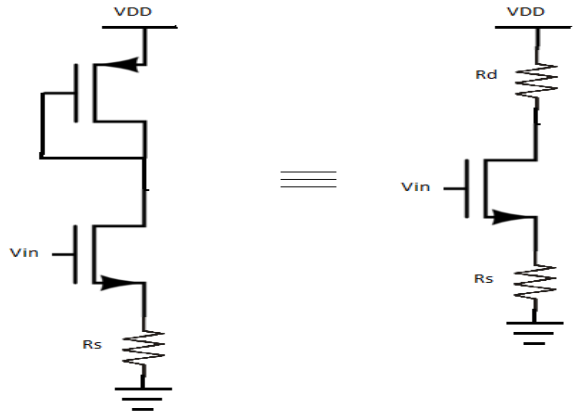

Fig. 5: Source Degeneration

$$V_{out} = -I_D R_d \quad (1)$$

I_D(drain current) depends non-linearly on V_{in}(input voltage). Thus, from equation (1), V_{out} depends non-linearly on V_{in}, resulting in non-linear behaviour of the circuit.
By source degeneration, transconductance of the circuit is given by equation (2), where g_m is the transconductance of the MOSFET.

$$G_m = \frac{g_m}{1 + g_m R_s} \quad (2)$$

As R_s increases, G_m becomes a weakly dependent on g_m and hence the drain current I_D.
For $R_s >> (\frac{1}{g_m})$, we get

$$G_m \approx \frac{1}{R_s} \quad (3)$$

$$\Delta I_D \approx \frac{\Delta V_{in}}{R_s} \quad (4)$$

Equation (4) indicates that drain current is a linear function of input voltage.

4. Simulation Results

This section covers the schematic of each of the discussed oscillators designed using Cadence Virtuoso tool in 90nm technology and their corresponding simulation results.

4.1 Ring VCO

Figure 6. is the schematic of the Ring VCO designed using Cadence Virtuoso tool in 90nm technology.

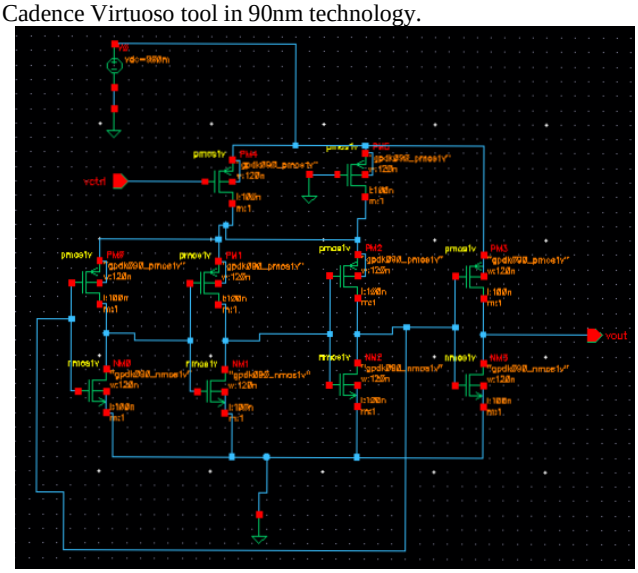

Fig. 6: Ring VCO schematic

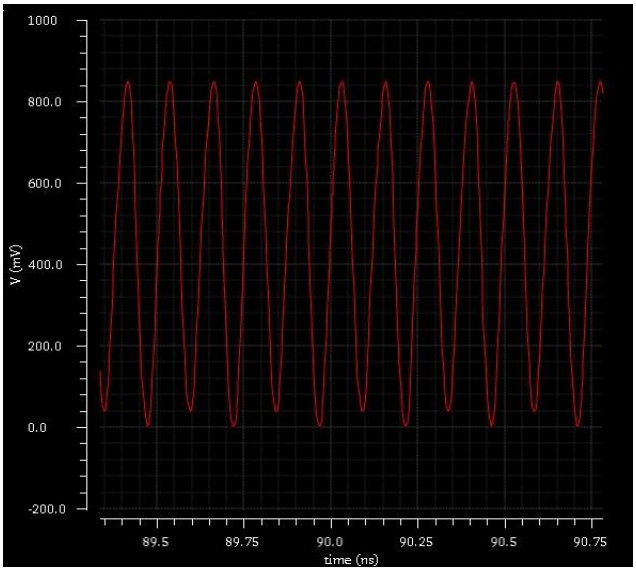

Fig. 7: Ring VCO simulation

Figure 7. is the output of the oscillator. It can be observed that output wave is sinusoidal in nature. The waveform is however not a perfect sine wave. The position of troughs in the wave is fluctuating.

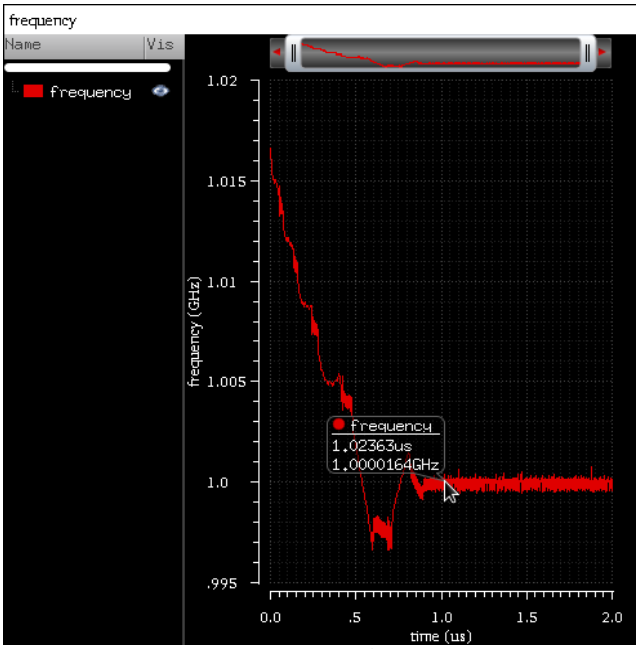

Fig. 8: Ring VCO output frequency plot

The frequency that was achieved is shown in the Figure8., which is around 1GHz. It can be observed that the frequency of oscillation is highly unstable. This was overcome in the latter discussed models of VCO.

4.2 Five Stage Current Starved VCO without Resistor

Figure 9. is the schematic of the 5-stage CSVCO without resistor designed using Cadence Virtuoso tool in 90nm technology.

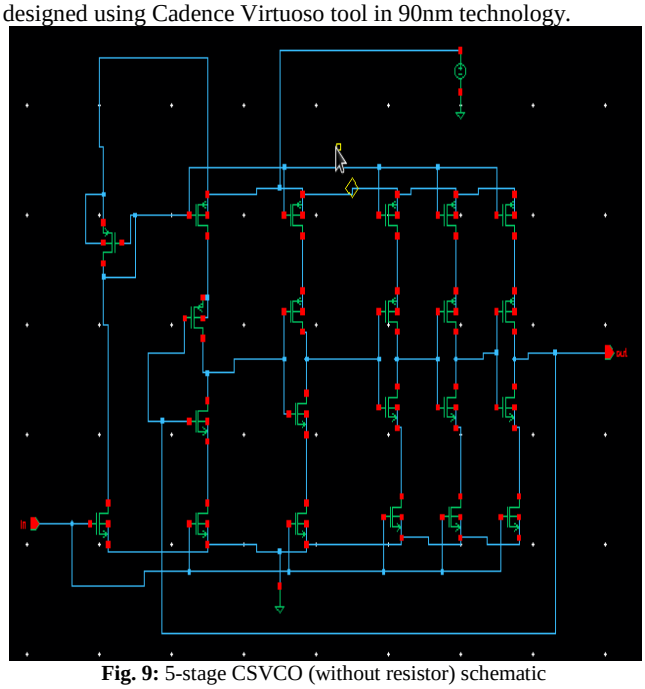

Fig. 9: 5-stage CSVCO (without resistor) schematic

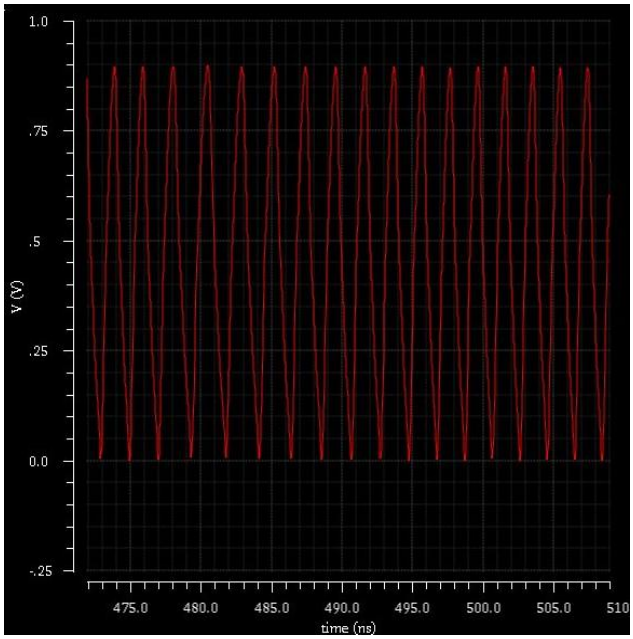

Fig. 10: 5-stage CSVCO (without resistor) simulation

Fig.10 is the output of the oscillator, after the oscillation frequency has become constant. The output is a sinusoidal wave. The shape of the output waveform is uniform when compared to the output waveform of the previously discussed ring VCO.

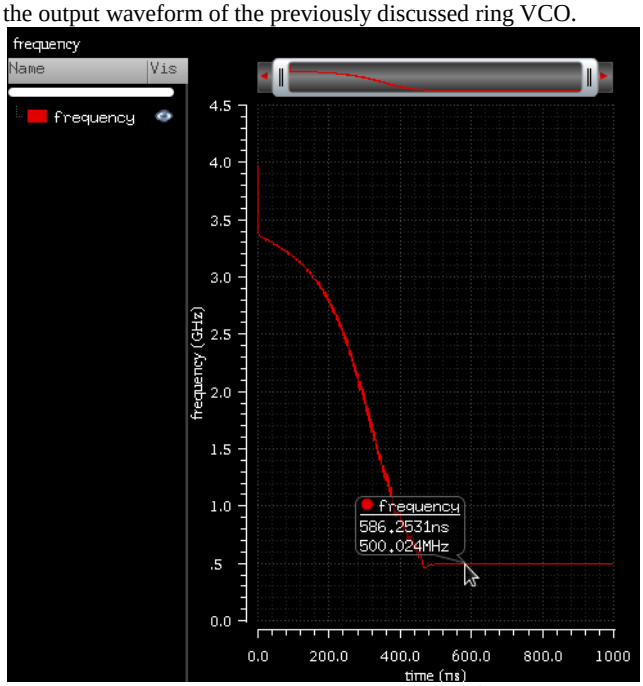

Fig.11: 5-stage CSVCO (without resistor) output frequency plot

The final output frequency attained is shown in the Frequency plot given in Fig.11. The frequency attained is about 500 MHz.

4.3 Five Stage Current Starved VCO with Resistor

Figure 9. is the schematic of the 5-stage CSVCO with resistor designed using Cadence Virtuoso tool in 90nm technology.

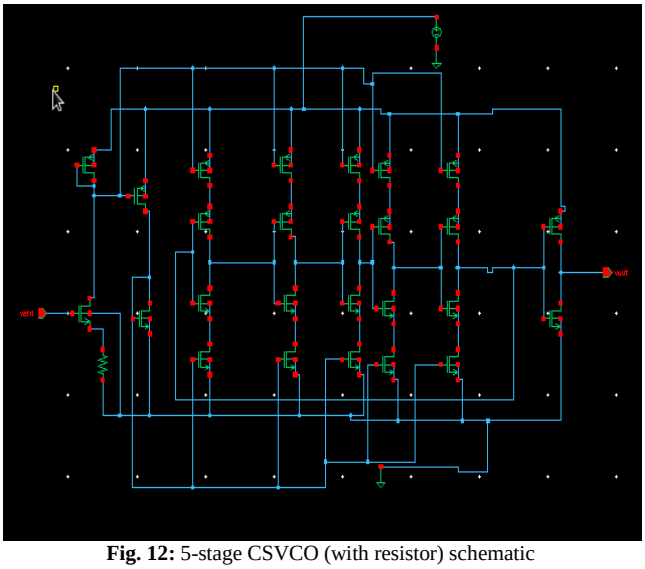

Fig. 12: 5-stage CSVCO (with resistor) schematic

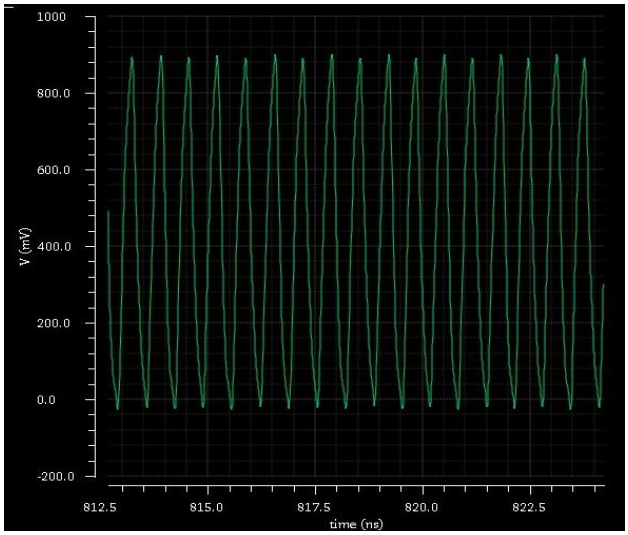

Fig. 13: 5-stage CSVCO (with resistor) simulation

Fig.13 is the output of the oscillator, after the oscillation frequency has become constant. A sinusoidal waveform is obtained.

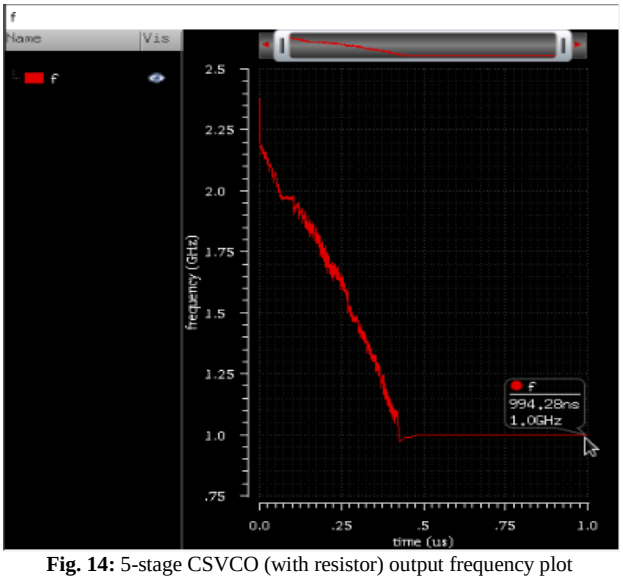

Fig. 14: 5-stage CSVCO (with resistor) output frequency plot

The final output frequency attained is shown in the Frequency plot given in Fig.14.The frequency of output waveform obtained was observed to be 1 GHz.

4.4 Frequency and Power Consumption Comparison Table

OSCILLATOR	FREQUENCY	POWER
Ring VCO	1 GHz	92.27 µW
5 stage CSVCO(without resistor)	500 MHz	32.06 µW
5 stage CSVCO(with resistor)	1 GHz	72.73 µW

From the table, it can be observed that the 5 stage CSVCO without resistor consumed the least power i.e., 32.06 µW while generating a frequency of 500MHz. On the other hand, the Ring VCO consumed maximum power i.e., 92.27 µW while generating a frequency of 1 GHz. The 5 stage CSVCO with resistor generated a frequency of 1 GHz with a power consumption of 72.73 µW that is intermediate to the other VCOs.

5. Conclusion

The comparison in the performance of the Ring VCO, 5 stage Current Starved Ring VCO with resistor and without resistor has been done in terms of frequency and power consumption using Cadence Virtuoso tool in 90nm technology. Each of these oscillators where placed in the PLL to conclude on the best fit for the application of high speed communication. It was observed that the Current Starved design of Ring VCO was better than the basic design of the Ring VCO in terms of power consumption. In order to achieve higher frequencies, the number of stages in the CSVCO can be increased. With the inclusion of resistance in the 5 stage CSVCO, a linear and stable behaviour of the circuit is observed. Also the frequency of oscillation is higher, however with a trade-off in power consumption.

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