International Journal of Engineering &Technology, 7 (3.12) (2018) 62-68

International Journal of Engineering & Technology

Website: www.sciencepubco.com/index.php/IJET

Research paper

Reduction of Power Consumption using Joint Low Power Code with Crosstalk Avoidance Code in Case of Crosstalk and Random Burst Errors

Ashok Kumar.K[1*], Dananjayan.P[2]

Department of ECE, Pondicherry Engineering College, Puducherry, India
**Corresponding Author E-mail: [1]kashok483@gmail.com*

Abstract

When technology is scaling down, reliability and power issues are arise in the intercommunication of System on Chip (SoC). The intercommunication links are suffers with various noise sources like crosstalk, temperature variation and voltage deflection which lead to communication link failure. To get reliable system, the strong error detection and correction codes are required. In this proposed work, Crosstalk avoidance code detects and corrects of one bit error, two bit error and some of three bit errors. The Hybrid Automatic Re-transmission Request is also used when the CAC detects the burst error of three. Apart from this, the Low Power Codes are used to get low power consumption using Bus Invert (BI) technique in proposed work. The LPC code reduces the power consumption of interconnection wires using reducing switching activity. The performance of proposed work evaluated in Xilinx 14.7 in Vertex-6 Field Programmable Gated Array (FPGA) device. The proposed work is calculated of power consumption of codec module and interconnection wire, delay of CAC and LPC code and link swing voltage. This work provides 11.7% improvement in power consumption and presents high reliability than JTEC. The energy dissipation of wires in the proposed work is decreased 23.5% than un-coded schemes.

Keywords: *Network on Chip; Crosstalk Errors; CAC; LPC; Reliability.*

1. Introduction

With shrinking of feature sizes, increasing of die size, increasing of storage equipment, increasing of functional blocks and increasing of processing elements (PEs) leads to complex in single chip [1]. As number of functional blocks is increasing in a single chip, needs powerful intercommunication system. A bus based intercommunication popularly used in system on chip (SoC) when number of functional blocks is less but it limiting performance in terms of scalability and reliability. Fig.1. shows the trend of gate delay and global wire delay with scaling of technology [2]. According International Technology Roadmap for Semiconductors (ITRS), the gate delay is decreasing and wire delay is increasing with scaling of technology hence the bus delay is affecting more on performance of SoC and preserving the signal integrity is important issue in the deep submicron (DSM) technology. Network on Chip (NoC) is the new paradigm to solve communication issues in SoC and improves the performance even at more functional blocks because of parallel communication between components in chip multiprocessor (CMP). The communication in of NoC is mainly associated with switches and PEs. The NoC switch affects the overall system performance hence the design of switch is crucial. The fault tolerance scheme needs extra circuit which leads loss of performance in terms of area and delay hence the circuits of fault tolerance should be optimized. In nano scale technology, the communication architectures are suffers mainly three issues. 1. Delay because of capacitance crosstalk, 2. Power because of parasitic and coupling capacitance 3. Reliability because of various noise errors. the reliability is a challenge issue when technology scaling down. The coupling capacitance is one of important parameter when technology is scaling down because decreasing of inter wire spacing and increasing of coupling capacitance is showing negative effect on metrics of communication architecture. Crosstalk is one of challenging issues for intercommunication in nano scale technology thereby Crosstalk Avoidance Codes (CAC) are used for reducing the noise and coupling capacitance. Shielding is also another technique to reduce the crosstalk with help of grounded wire between the pair of links. Though it is better solution, the doubling of wires limits performance of system hence the wire size is optimized to preserve the performance of system. Adding of CAC scheme in NoC switch, reduce the crosstalk effect without increasing number of wires hence the energy of intercommunication link is controlled. The energy dissipation and worst case delay increases when adjacent wires are switch opposite direction simultaneously. CAC techniques are reducing the worst case switching capacitance as well as avoiding of switching transitions of adjacent wires at opposite directions and avoiding the transitions of adjacent code word 101↔010. This condition reduces the worst case capacitance from $(1+4\lambda)C_L$ to $(1+2\lambda)C_L$hence the energy of interconnection wire reduced from $(1+4\lambda)C_L\alpha{V_{dd}}^2$ to $(1+2\lambda)C_L\alpha{V_{dd}}^2$ where λ be the ratio of coupling capacitance to the bulk capacitance, α isthe transition activity factor, C_L is the self capacitance of wire and V_{dd} is the

supply voltage. The energy dissipation is reduced with reducing of the worst case capacitance in CAC schemes.

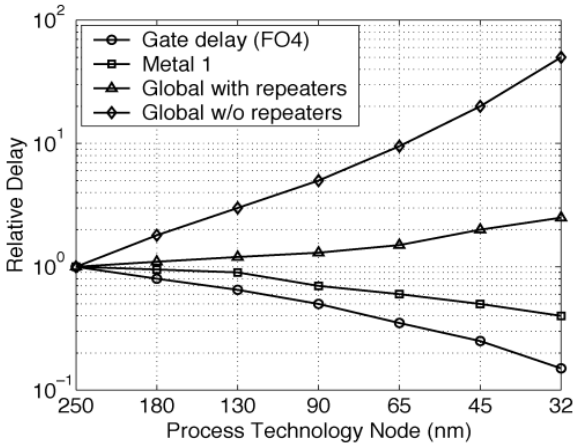

Fig. 1: Delay vs scaling of technology [2]

To reduce power consumption, a low power code (LPC) scheme is presented for interconnection links by reducing the wire transition activity [xii]. This LPC concentrates on only reduction of self switching activity of a wire but not reduction of power in CAC. To decrease the overall power consumption and increase of reliability, the joint crosstalk avoidance code with enhanced double error correction (CAEDEC) scheme is used. CAEDEC is increasing the error detection and correction capability with reduction in worst case bus delay but not concentration on power consumption due to interconnection wires. The proposed work aims to get low power consumption and high reliability in case of crosstalk errors. In this paper, joint LPC-CAC scheme is proposed for decreasing in power consumption of wires and increasing of reliability of crosstalk errors. LPC technique measures the hamming distance of data packet and applies Bus Invert method (BI) and inverts the data packet depending the hamming distance. The encoder CAC is using triplicate add parity for data encoding and the data re-constructed with help sent parity bit in decoder. In this work, the CAC is correcting errors maximum upto three. Hybrid Automatic Re-transmission Request (HARR) is enabled when burst error of three detected at decoder section.

The remaining of the paper organized as follows: section-2 presents the background work of various error correction schemes. The advanced router architecture with combination of joint LPC-CAC scheme is explained in the section-3. In section-4, the proposed joint LPC-CAC method with HARR described. The performance evaluation is presented in the section-5 and finally, concludes the paper in section-6.

2. Related work

Detection and correction of soft errors is important to efficient data transfer in SoC interconnects. A lot of scope for research in this domain for presenting different algorithms for crosstalk avoiding or correcting errors present in the communication architecture and various techniques are presented for error detection and correction in literature. Parity codes are detecting only single error (SED) but not correction [3]. Hamming code is popularly used for single error correction and double error detection (SEC-DED) [4, 5].These techniques are handling only errors but not involved crosstalk avoidance code. Forbidden Transition Condition (FTC), Forbidden Overlap Condition (FOC) and Forbidden Pattern Condition (FPC) are three different codes of crosstalk avoidance code [6, 7]. The worst case crosstalk induced bus delay (CIBD) calculated for these conditions and delay is reduced from $(1+4\lambda)\tau$to $(1+3\lambda)\tau$in FOC and other two conditions reduced to $(1+2\lambda)\tau$. To detect and correct multiple errors, the combination of Error Correcting Code and Crosstalk Avoidance Code is used. Duplicate Add Parity (DAP) [8] is using the concept of duplicating data for reducing the delay to$(1+2\lambda)\tau$. S. R. Sridhara, and N. R. Shanbhag [9] are proposed a framework for reducing power consumption in case of crosstalk avoidance code. The low power code is concentrated on reducing the transition activity but not on codec module of CAC.

Dual Rail (DR) [10], Modified Dual Rail (MDR) [11] and Boundary Shift Code (BSC) [12] are techniques to reduce the bus delay with reducing of switching capacitance from $(1+4\lambda)C_L$to$(1+2\lambda)C_L$ and correcting the single random error. The operation of BSC technique is similar to DR and MDR only the difference is the parity bit adding for each clock cycle at encoding. B.Fu and P. Ampadu [13] are proposed a scheme for detection and correction of two bit burst errors with Hybrid Automatic Repeat Request (HARQ). DAP scheme is combined with hamming code to increase capacity of detection to four and correction of three errors [14]. Joint triple error correction- simultaneous quadruple error detection (JTEC-SQED) is re places Hsiao code that of hamming code. Hsiao codes are improving error detection and correction capability than hamming code. Po Tsang Huang, Wei Hwang [15] proposed Triplicate Add Parity (TAP) and multiple groups of hamming code used at decoder section to increase performance of CAC. Crosstalk avoidance code with TAP corrects two bit errors when errors found in different groups but in [16], the scheme corrects complete possibilities one bit and two bit errors and some of three bit errors.

Majority of existing works are concentrated on combination of error correction codes with crosstalk avoidance and correcting maximum of error upto three. In this work, triplicates add parity (TAP) crosstalk avoidance code is used for correcting one bit, two bit and some of three bit random errors. The Hybrid Automatic Re-Transmission Request (HARR) is enabled when decoder sends negative acknowledgement (NACK) because of burst error of three bit. The low power code is also used for reducing the power consumption because of number of wires increased when compared with existing work. Bus-Invert method is used to get low power consumption with help of reducing transition activity in data sequences. Best of knowledge, this is the first joint LPC-CAC technique for detection and correction of errors with low power consumption.

3. Advanced NoC Switch Architecture

The error detection and correction codes are increase the reliability but decreases the performance of NoC switch hence maintaining of the performance of switch in case of faults is difficult. This NoC switch is designed with Crosstalk Avoidance Code for detection and correction of cross talk error. To this end, the switch architecture is modified and advanced to get high performance and low power consumption. The codec modules are inserted in between of input port and output port and BI technique is also inserted for NoC switch. The advancement in switch architecture is shown in fig.2 which is combination arbiter and crossbar switch. This NoC switch is consisting of 6 bi-directional input and output ports to increasing interfacing capability with memory or input-output devices. The arbiter is resolving the conflict between the ports which are ready transfer the data [19]. The arbiter is constructed with distributed round robin technique to provide the priorities of the request of ports. The crossbar is used to transfer the data packets from input port to output port. A store and forward switching technique is used to data switching because of avoiding dead lock error. Each port is having buffer and its controller to store and control the data transfer depends on the traffic in the link.

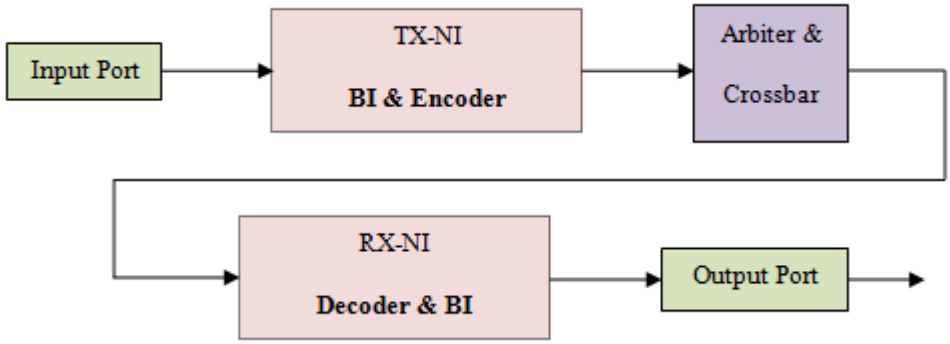

Fig. 2: Advanced NoC switch architecture with low power code with CAC codec components

If traffic is more towards the destination switch, the data packet will store in the buffer until finds the alternative route from current switch to destination switch. Adaptive routing is the best routing algorithm for data packet routing in case of high traffic between switches and it finds shortest path towards destination switch. Network Interface (NI) is key component in this switch architecture because of proposed work is implemented in it. Transmit NI (TX-NI) is having the BI and encoder of CAC for encoding the original data packet and Receive NI (RX-NI) is having decoder and BI for re-construct the original data packet from the errors.

From literature, adding of encoder and decoder modules in NoC switch causes increases in the power consumption. This CAC uses Triplicate Add Parity (TAP) thereby the number of wires are increased than existing work. These wires increases power consumption of the interconnection links. Apart from encoding and decoding, the re-transmission is another important parameter to increase the power consumption. When the CAC detects burst error, the hybrid automatic request is enabled and data transmission is repeated from source to destination. To reduce the power, the BI method added before encoding process and after decoding process but area of switch is increasing because of number of full adders and inverters are used. The joint LPC-CAC technique is implemented in NI of switch to maintain the high performance in case of crosstalk errors. The PEs are associated with NI to process the data packets and transferring to input or output devices. The producer- consumer PEs are used for each switch to increase speed of the NoC switch, it means each switch has two PEs to control the data transfer between source switch and destination switch. this advance NoC switch improves the performance because of PE pair.

4. Crosstalk Avoidance Code-Burst Error Correction

The reliability of the NoC switch is depends on the capacity of fault-less transaction of encoder and decoder. The energy consumption of codec is also considering metric in case of crosstalk faults hence the design of codec module crucial for NoC switch. This work involves technique for low power and crosstalk avoidance code technique for detection of one bit error, two bit errors and some possibility of the detection three bit errors and burst error. When burst error of three bit is detected, the re-transmission is requested. The Hybrid Automatic Retransmission Request (HARR) is turned on when burst error is detected by CAC.

Operation of Encoder

The data packet transfers from buffer of input port to Network Interface (NI). The codec modules are implemented in NI for detection of crosstalk errors. In encoder module, the original data duplicates thrice and combined with parity bit by standard triplication scheme. Among various encoding schemes for detection, triplication scheme is most suitable for detection and correction with less energy consumption. The encoder in fig.3 enhances the capacity of detection of errors and improves the reliability of wires among ports because of adding only one parity bit to the scheme. The problem with this scheme is using more interconnection wires but these on-chip wires are very cheap and increasing huge number with advance in technology scaling of SoC.

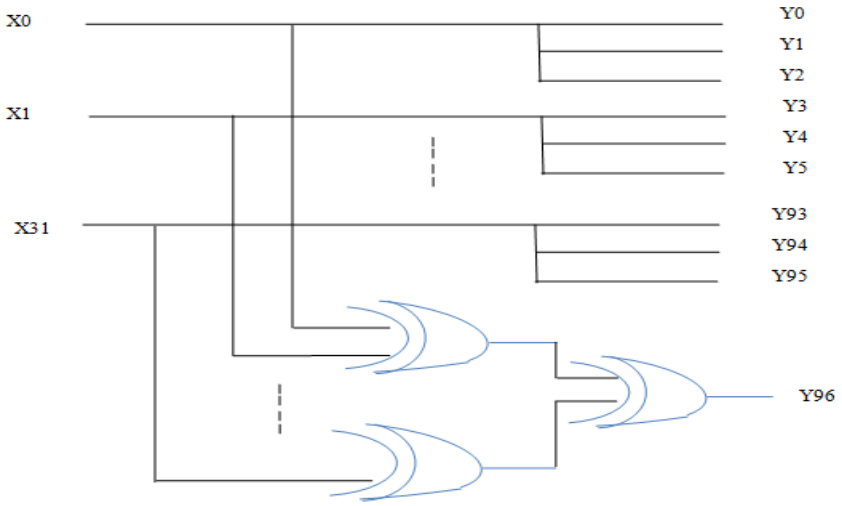

Fig. 3: architecture of CAC encoder (32, 97)

This encoder is using with triplication of original data packet with parity bit for efficiently detection and correction of errors due to cross coupling capacitance [20]. The parity bit is calculated by adding logically (XORing) of entire original data packet. Depends

on parity bit, the output port decodes the original data correctly hence encoding of parity bit is more important in this technique. This encoder detects utmost three errors and corrects two errors because of triplication. The number of detection and correction of errors is depending on hamming distance of the code. If the hamming distance of k for original data packets, the number of detection errors is k-1 and correction is (k-1)/2. In this work, the hamming distance is 4(triplication of data packet and one parity bit) hence number of error detection is three bits and correction is two bits. Initially, the 32 bit data packet is triplicates 96 bits and adds one parity bit to identify erroneous bits in the data packet.

Decoder

The decoder is working based on following algorithm explained with help of single, double and three error bits in the data packet. The encoded data separated into three groups because of original data triplicates and encoded. The group separator is dividing the encoded data to the groups. The parity bit (p0) is identified from encoded parity and also parity of each group is calculated (p1, p2, p3). The single error detected when changes the parity bit of corresponding group and two bit error are identified with help of received data in the group. When two bit is present in the data, received data in the groups is different from encoded data. Different possibilities of two bit error patterns given table x1 are detected and corrected as per decoding algorithm shown in fig.4. The possibilities of single, double and three bit errors are presented in table 1. The single and double error bits are corrected and some of three error bits also corrected but burst errors are not corrected by CAC code.

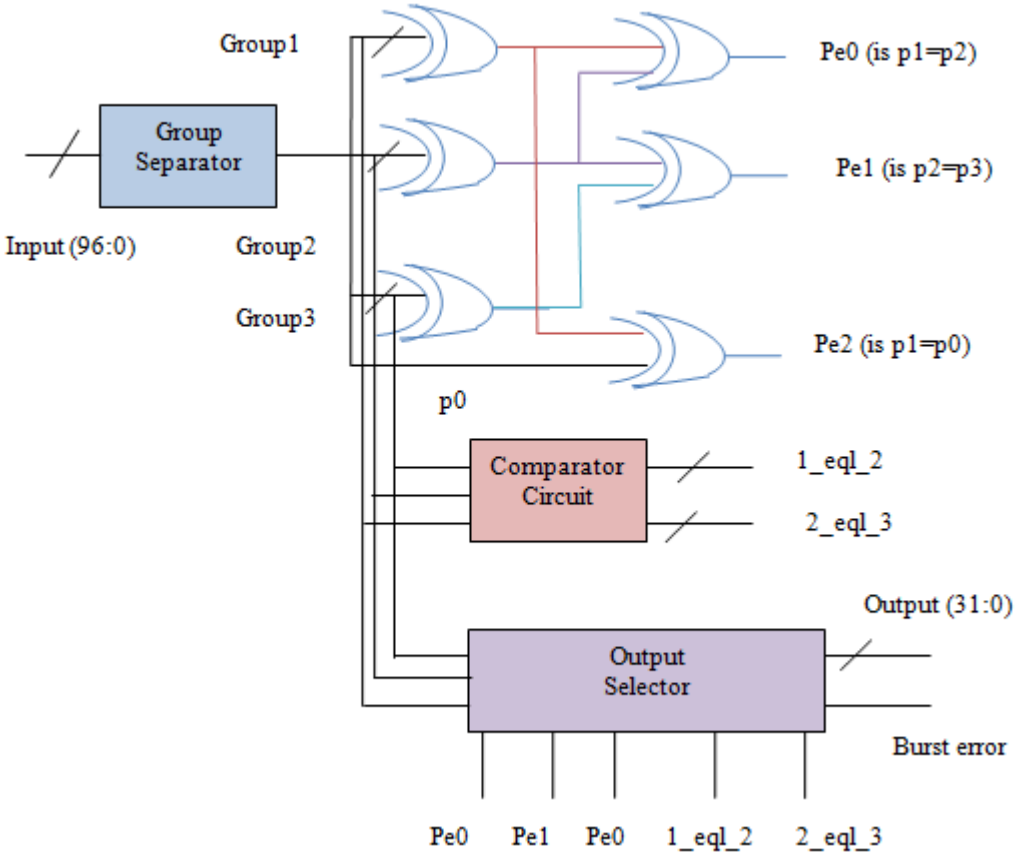

Fig. 4: decoding operation of crosstalk avoidance code for detecting erroneous bit

When burst error is detected by the decoding module, the Negative Acknowledgement (nack) is sent to the source port thereby re-transmission process starts from source to destination. From table x1, the possibilities of different error patterns are detected in the data packet. For detecting two bit error patterns, following different cases are considered.

Case (i) p1=p2 and p2≠p3

To identify the error-less group, parity of group1 (p1) is compared with p0. When p1=p0, group1 is selected as error-free otherwise group 3 is considered as error-less.

Case (ii) p1≠p2 and p2=p3

To find the error free group, parity of group 1(p1) is compared with p0. If p1=p0, group 1 is given as error free otherwise group2 is selected as error free.

Case (iii) p1≠p2 and p2≠p3

To select error free group, parity of group 1(p1) is compared with p0. If p1=p0, the group 1 is considered as error-less otherwise group 2 is selected as error-less.

Case (iv) p1=p2 and p2=p3

The error bit patterns shown in green colour considered in this group. This work cannot detect even parity bits there parities of three groups considered as same. In this case, two categories of error bits are selected. (1). Single error bit in three groups called as burst error. To detect burst error, if p1=p0 and p1=p2 otherwise error pattern is another category. (2) To select error free output, the data packets of group1, group2 and group3 are compared. If data packet of group1 is equal to group2 then group 2 is selected as error free otherwise, data packet of group2 and group3 compared again. If data packet of group2 is equal to group3, group 3 is selected as error free otherwise group 1 is considered as error free of two bit errors.

Table 1: different error bit patterns

	One bit error			Two bit errors						Three bit errors									
Group 1 (p1)	1	0	0	1	0	1	2	0	0	1	0	1	0	3	0	0	1	2	2
Group 2 (p2)	0	1	0	1	1	0	0	2	0	1	1	0	2	0	3	0	2	1	0

Group 3 (p3)	0	0	1	0	1	1	0	0	2	1	2	2	1	0	0	3	0	0	1	
	Correctable			Correctable						Correctable							Un-correctable			

Joint LPC and CAC

The Low Power Codes (LPC) is mainly used for reducing the power consumption crosstalk avoidance code. LPC is reducing the transition activity depending on hamming distance of original data packet.

This LPC technique implemented with Bus-Invert method (BI). BI method transfers either original data or inverted data based on condition thereby the input for CAC is either inverted or normal data [21].

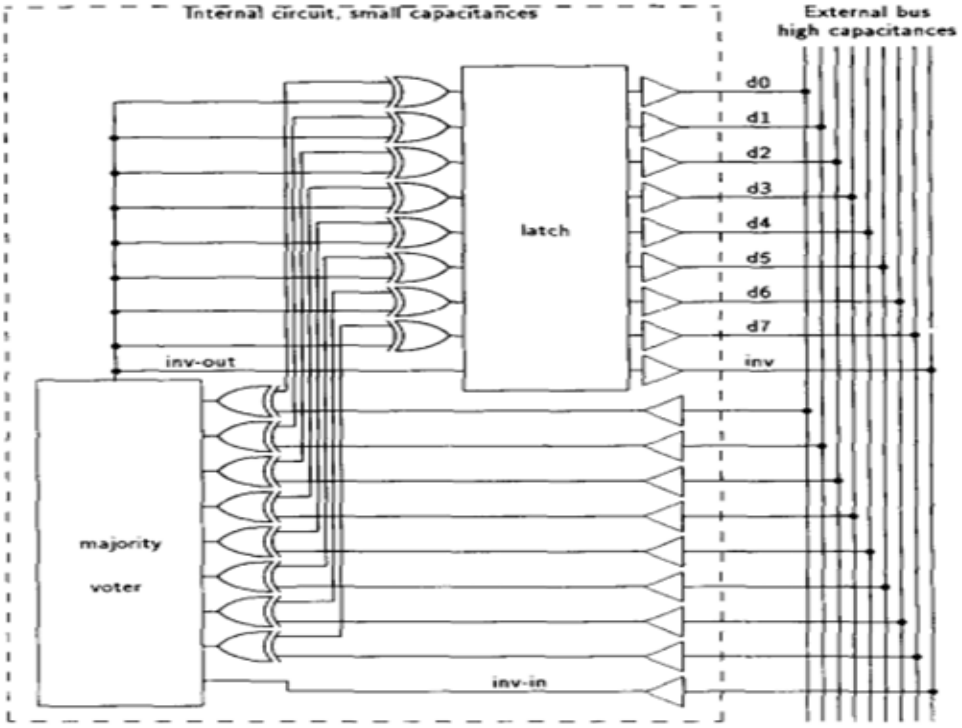

Fig. 5: Bus Invert method [21]

BI method is commonly used for reducing the power consumption when system consumes more power due encoding and decoding processes is involved. Fig.5 describes the BI method for 8 input data packet and 16 number of ex-or gates are used for invert. This method is mainly depending on majority voter circuit which is combination of full adders (FA). There is extra area and delay in this method because of ex-or gates and majority voter circuit but reduced power consumption. If hamming distance is larger than n/2, the data is inverted otherwise not inverted hence invert line in figure is concentrated more in the circuit. Based on this condition, the transitions activity of data packet is reduced hence the power consumption is reduced.

Reliability

The errors are increased with several noise sources in SoC interconnects. The Gaussian function is commonly used for probability of Bit Error Rate (BER) for single wire ε is given by

$$\varepsilon = Q\left(\frac{V_{dd}}{2\sigma_n}\right) \quad (1)$$

where V_{dd} is link supply voltage $\sigma_n$is standard deviation of noise. The eq. (1) considers that the errors in wire are independent but when technology is scaling down, the interconnect links are effected due to the coupling noise there by possibility of burst error increases. The error on wire effects neighbour wires but the effect is decreases with increasing distance of neighboring wires hence the effect is consider only beside wires and effect of other wires is negligible. The residual flit error rate is one of key parameter for evaluating the reliability of any coding scheme. The residual error is the complement of correctable errors present in the system hence probability is calculated by following eqn.

$$P_{res} = 1 - P_{corr} \quad (2)$$

where P_{res} is the probability of residual flit error rate and P_{corr} is the probability of correctable error rate. Because of Hybrid Automatic Request Re-transmission (HARR) is used in the technique, the probability of residual error calculated

$$P_{res} = P_{und} + P_{d-nc}P_{und} + P_{d-nc}{}^2P_{und} + .. \quad (3)$$

where P_e is probability of un-detectable faults and $P_{d\text{-}nc}$ is probability of detectable but not correctable faults.

The extra power consumption of this technique is calculated by

$$PW = PW_{encoder} + PW_{decoder} + PW_{link} \quad (4)$$

where $PW_{encoder}$ is the power consumption of encoder, $PW_{decoder}$ is the power consumption of decoder and PW_{link} is the power consumption of interconnection links. The power consumption of interconnection link depends on number of wires used for duplication of original data for encoding.

$$PW_{link} = C_{link}.W_L.\alpha.V^2.f_{clk} \quad (5)$$

Power consumption of interlink is directly proportional to C_{link} interconnect capacitance of wires, W_L is width of link, switching factor (α), link swing voltage (V) and clock frequency (f_{clk}). The strong Error Control Codes require higher interlink swing voltage for getting high reliability of scheme.

5. Performance Evaluation

The simulation and synthesis results are presented for the Joint Low Power-Crosstalk Avoidance Code (LP-CAC) NoC switch in terms of area, delay and power consumption. The proposed work is simulated in Xilinx software and implemented on Vertex-6(XC6VLX760) Field Programmable Gated Array (FPGA). The proposed work is implemented for 32 bit of original data which triplicates and encodes to the receiver. From Table 2-4, Area, Clock Frequency and Power Consumption are the metrics for 8, 16, 32 bit coding scheme. It is evident that the power consumption of joint LPC-CAC scheme is lesser than CAC scheme because of BI method is used for reducing the power consumption but area

utilization is increasing because of additional XOR and full adders. There is no much difference of power consumption when data packet is small (8 bit) but it is presenting much difference when data packet increases more (32 bit and on wards).

Table 2: Performance metrics of NoC switch with crosstalk avoidance code encoder and decoder

family	Number of Slice Registers	Number of Slice LUTs	Number of fully used LUT-FF pairs	Clock Frequency (MHz)	Power Consumption (mW)
8-bit	814	566	375	270.86	9.56
16-bit	952	636	453	181.42	47.42
32-bit	1858	1485	676	165.68	89.55

Table 3: Performance metrics NoC switch with encoder and decoder with low power module

family	Number of Slice Registers	Number of Slice LUTs	Number of fully used LUT-FF pairs	Clock Frequency (MHz)	Power Consumption (mW)
8-bit	823	635	440	270.86	9.40
16-bit	996	764	518	181.42	46.90
32-bit	1926	1599	1014	165.68	81.64

Table 4: Area and Delay results for Encoder and Decoder of CAC

family	Number of Occupied Slices		Number of Slice LUTs		Number of Bonded IOBs		Delay (ns)	
	Encoder	Decoder	Encoder	Decoder	Encoder	Decoder	Encoder	Decoder
8-bit	1	15	2	39	35	36	1.011	2.82
16-bit	3	24	2	42	67	68	1.53	3.15
32-bit	7	49	7	79	131	132	1.53	3.20

Table 5 presents comparison of different crosstalk avoidance schemes for 32 bit in terms of number of wires used, delay and power consumption. The results are described for codec module (encoder and decoder) of crosstalk avoidance code. It is evident that the codec module of joint low power-CAC is lesser than existing work because of low power code is using fewer transitions in the data packet to save the power consumption. This work is also requires lesser swing voltage to detect random burst error than JTEC [14] because of triplication of original data. JTEC [14] is corrects the two bit errors but the delay and power consumption are more than LPC-CAC. The proposed work is improved 11.7% in terms of power consumption than JTEC and maintaining the delay same. This work corrects three bit error and detects the random of burst error of three there by the reliability is improves than exiting work.

Table 5: Comparison of codec module of crosstalk avoidance code for 32 bit data packet

s. no.	Coding scheme	Data width	Number of wires used	Error detection	Error correction	Link swing voltage	Delay	Power (μW)
1	Hamming [17]	32	38	Double	Single	1.02	1+4λ	49.30
2	DAP [18]	32	65	Double	Single	1.02	1+2λ	16.22
3	Hsiao SEC-DED	32	39	Double	Single	1.02	1+4λ	51.60
4	CADEC [8]	32	77	Random and burst error of two	One bit and two bit errors	0.89	1+2λ	26.77
5	JTEC [14]	32	77	Random and Burst error of three	One bit and two bit errors	0.81	1+2λ	39.49
6	Joint LPC-CAC	32	97	Random and Burst error of three	One bit, two bit errors and some of three	0.61	1+2λ	34.86

The reliability of this switch is comparing with Un-coded, JTC [14] in terms of energy consumption and for this, the NoC switch is simulated for 32 times at Uniform Random traffic pattern. The each simulation shows less energy consumption even when number of identified errors is increasing. Fig.6 shows energy dissipation under the uniform traffic pattern for 8×8 mesh based NoC with 32 bit data used in the system. It inference that the LPC-CAC NoC is showing less energy consumption than Un-coded, JTC [14] because of the original data inverted based on hamming distance and then the data is encoding there by switching activity of encoded data is reduces there by the energy of interconnection wire reduces.

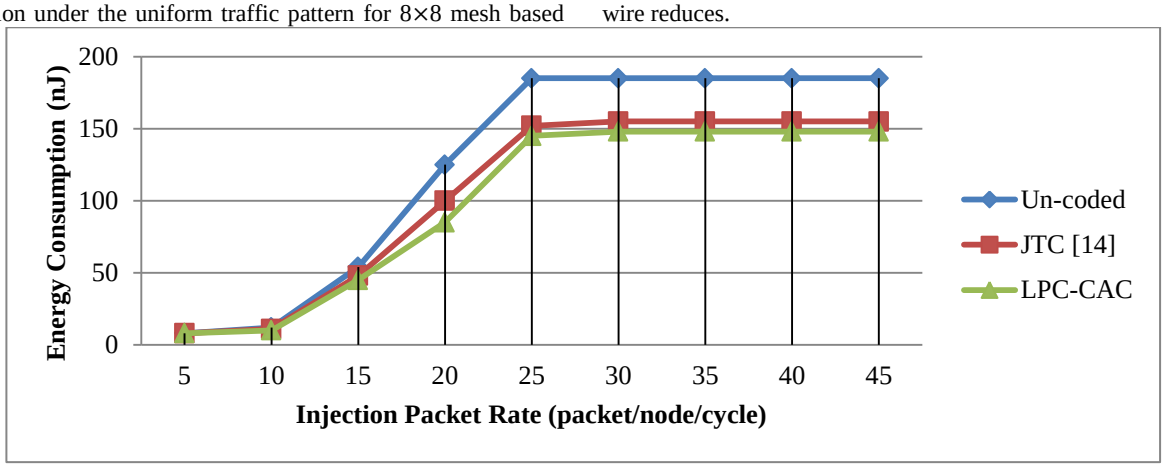

Fig. 6: energy dissipation of different techniques of 8×8 mesh based NoC

6. Conclusion

In this paper, the proposed Crosstalk Avoidance Code is presented for increasing reliability and decreasing wire delay of NoC switch. The encoder is using triplicates add parity bit to enhancing the

error correction capability and decoder is re-constructed the data with comparing received parities with sent parity bit. By this operation of codec module, this work detected and corrected of complete one bit error, two bit errors and some of three bit errors and also detected the random burst error of three. The Hybrid Automatic Re-transmission Request is used when burst error is detected by decoder module. This proposed work also using low power code for reducing the power consumption of interconnection wires. Bus-Invert method is used in low power code by reducing switching activity of wires. Hence, the proposed work is achieves the power optimization of interconnection wires and increasing the error correction capability. The proposed work presented 11.7% improvement in terms of power consumption and presents high reliability than JTEC. The energy dissipation of interconnection wires in proposed work is reduced 23.5% than un-coded schemes.

References

[1] L. Benini, G. De Micheli, "Networks on chips: a new SoC paradigm," IEEE Computer, pp. 70–78, 2002.

[2] International Technology Roadmap for Semiconductors. Semiconductor Industry Assoc. [Online]. Available: http://public.itrs.net

[3] Fu, B., Ampadu, P, "Error control for network-on-chip links," New York: Springer, 2012.

[4] Murali, S., Theocharides, T., Vijayakrishnan, N., Irwin, M.J., Benini, L., Micheli, G. De., "Analysis of error recovery schemes for networks-on-chips", IEEE design and Test of computer, vol. 22, pp. 434–442, 2005.

[5] Bertozzi D, Benini L, Micheli GD, "Error correction schemes for on-chip communication links: The energy- reliability tradeoff," IEEE Transactions on Computer-Aided Design of Integrated Circuits And Systems, vol. 24, no. 6, pp. 818–831, 2005.

[6] Duan, C., Tirumala, A., Khatri, S. P., "Analysis and avoidance of crosstalk in on-chip buses," IEEE International 9th Conference Hot Interconnects, pp. 133-138, August 2001. Stanford, CA

[7] Ganguly, A., Pande, P. P., Belzer, B., Grecu, C., "Addressing Signal Integrity in Networks on Chip Interconnects through Crosstalk-Aware Double Error Correction Coding," IEEE Computer Society Annual Symposium on VLSI, March 2007, Porto Alegre.

[8] Ganguly, A., Pande, P.P., Belzer, B., Grecu, C., "Design of low power & Reliable Networks on chips through joint crosstalk avoidance and multiple error correcting coding", Journal of Electronic Testing: Theory and Appl. (JETTA), vol.24, no.1-3, pp. 67–81, 2008.

[9] S. R. Sridhara, and N. R. Shanbhag, "Coding for System on chip Networks: A Unified Framework," IEEE Transactions on VLSI Systems, vol. 13, no. 6, pp. 655-667, June 2005.

[10] Rossi D, Metra C, Nieuwland AK, Katoch A, "Exploiting ECC redundancy to minimize crosstalk impact," IEEE Design and Test of Computers, vol. 22,no. 1, pp.59–70, 2005.

[11] Rossi D, Metra C, Nieuwland AK, Katoch A, " New ECC for crosstalk effect minimization," IEEE Design and Test of Computers, vol.22, no. 4, pp.340–348, 2005.

[12] Patel KN, Markov IL, "Error correction and crosstalk avoidance in DSM buses," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 12, no. 10, pp.1076–1080, 2004.

[13] B. Fu, P. Ampadu, "Burst error detection hybrid ARQ with crosstalk delay reduction for reliable on chip Interconnects," 24th IEEE International Symposicium on Detect Fault Tolerance in VLSI Systems, pp.440–448, 2009, USA.

[14] Ganguly, A., Pande, P., B Belzer., "Crosstalk-Aware Channel Coding Schemes for Energy Efficient and Reliable NOC Interconnects", IEEE Transactions on very Large Scale Integration Systems, vol. 17, no.11, pp. 1626–1639, 2009.

[15] Po Tsang Huang, Wei Hwang, "Self-Calibrated Energy-Efficient and Reliable Channels for on chip Interconnection Networks", Journal of Electrical and Computer Engineering, vol. 2012, pp.1-19, 2012.

[16] Maheswari M, Seetharaman G, "Design of a novel error correction coding with cross talk avoidance for reliable on chip interconnection networks," International Journal of Computer Applications in Technology, vol. 49, no. 1, pp.80–88, 2014.

[17] Yu, Q., Bo Zhang, Yan Li, Paul Ampadu., "Error Correction Integration scheme for reliable NOC", Proceedings of 2010 IEEE International Symposium on Circuits and Systems (ISCAS), pp.3893-3896, August 2010, France.

[18] Pande, P.P., Ganguly, A., Brett Feero, Belzer, B., "Design of low power & Reliable Networks on chip through joint crosstalk avoidance and forward error correction coding", Proceedings of 21st IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems, pp.466-476, 2006.

[19] Ashok Kumar K, P.Dananjayan, "A Survey for Silicon on Chip Communication", Indian Journal of Science and Technology, vol. 10, no.1, pp.1-10, 2017.

[20] Maheswari M, Seetharaman G, "Multi bit random and burst error correction code with crosstalk avoidance for reliable on chip interconnection links", Microprocessors and Microsystems, vol. 37, no.4–5, pp.420–429, 2013.

[21] M.R. Stan and W.P. Burleson, "Bus-invert coding for low power I/O", IEEE Transactions on VLSI Systems, vol.3, no.1, pp.49-58, 1995.