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Research paper

FPGA implementation of power on self-test towards combo card

R. Srivel [1] *, Dr. R. P. Singh [2] , Dr. D. Arokiaraj [3]

[1] Research Scholar, Department of Electronics and Communication Engineering Sri Satya Sai University of Technology & Medical Sciences, Sehore, Madhya Pradesh
[2] Research Supervisor, Sri Satya Sai University of Technology & Medical Sciences, Sehore, Madhya Pradesh
[3] Associate Professor, Department of Management Studies, Aurora's PG College, Hyderabad, India
**Corresponding author E-mail: rsrivel@gmail.com*

Abstract

The Combo Card is a legacy trunk and subscriber card which provides loop dialing, MAGNETO, FXS, FXO, E&M and SHDSL two wire ports. The Purpose of this Card is to Facilitate Voice and Data Services for the User in Small Deployment. This Module is going to be plugged into Line Card V3 and used in TDM Router. As an FPGA Engineers, Our main Focus is on FPGA part on this SERVICES CARD. We are Using Spartan-6 FPGA in this Project. The Name COMBO CARD isCame into Existence as we are Combining Many Interfaces viz., FXS, FXO, LD, E & M, Magneto, and SHDSL. In this study We are Dealing With Respect to FPGA by Using VHDL and Generating Clock and Sync Pulse 8.192 M Hz Generation for FXO and FXS, SHDSL Control Pin Mapping, Power on Self-Test With Respect to Clock Monitor and Generation of Reset Pulse 300us For all the Devices Connected to FPGA, So, that the Title FPGA Implementation of Power on Self-Test On Services Card Justifies.

Keywords: *COMBO CARD; FXS; FXO; LD; E & M; Magneto; and SHDSL.*

1. Introduction

1.1. Objective of the study

The Purpose of this Combo Card is to facilitate voice and data services for the user in small deployment. Our Objective as an FPGA Engineers is to generate clock and sync pulse generator for FXS and FXO, SHDSL control pin mapping, Power on self-test with respect to clock monitor and generation of the reset pulse for all the devices connected to FPGA [1].

2. Interfacing devices in combo card

2.1. Foreign exchange station

It is used to interface the telephone with supplies battery power and also provides dial tone as well as ringing voltage. A device that connects to such an interface contains a foreign exchange office (FXO) interface and could be a standard analog telephone or a private branch exchange (PBX) to receive telephone service.

- An FXS interface provides service at the "station" end of a foreign exchange line.
- Any telephone exchange is an example of an FXS, as is the telephone jack on the wall, though the term is rarely applied except in connection with foreign exchange service.

An FXS interface utilizes a line protocol, most commonly loop start, to detect when the terminating device (telephone) goes on-hook or off-hook and can send and receive voice signals.

2.2. Foreign exchange office

In telecommunications, exchange workplace (FXO) designates a phone-to-phone sign interface that generates the off-hook and on-hook indications (loop closure/non-closure) at the exchange station's (FXS) finish of a phone line. Analog phone-to-phone handsets, fax machines, and analog modems are FXO devices, though the term is never used except in reference to the exchange server.
Analog telephone handsets, fax machines, and analog modems are FXO devices, though the term is rarely used except in connection with foreign exchange service.
FXO interfaces are also available for computers and networking equipment, to allow these to interact directly with plain old telephone service (POTS) systems. These are commonly found in devices acting as gateways between local Voice over Internet Protocol (VoIP) systems and the public switched telephone network (PSTN). In a nutshell, an FXO device is any device that, from the point of view of a telephone exchange, appears to be a regular telephone. As such, it should be able to accept ringing signals, go on-hook and off-hook, and send and receive voice frequency signals. It may use loop start or ground start signaling. FXO channel units were invented and named in the middle 20th century for service at the "Office" end of an FX line via carrier system [21].

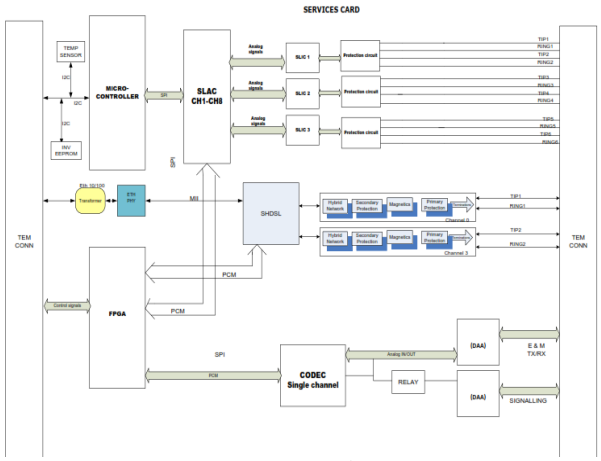


Fig. 1: Block Diagram of Combo Card.

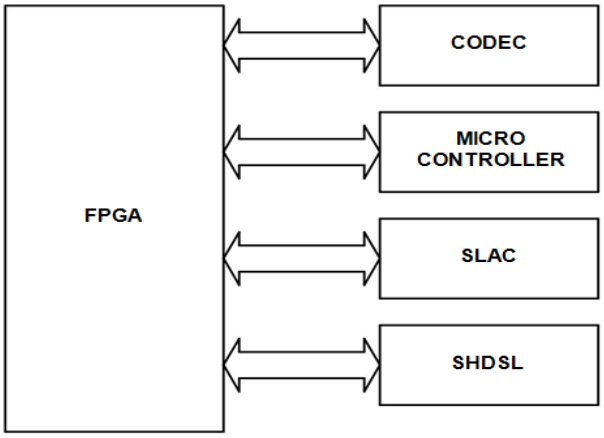


Fig. 2: FBGA Interfacing Device.

2.3. Magneto

A telephone magneto is a hand-cracked electrical generator that uses permanent magnets to produce alternate current from the rotating armature. In early telegraphy, magnetos were used to power instruments, while in telephony they used to generate electrical current to drive electromechanical ringers in telephone sets and on operator consoles.

2.4. E & M

E and M signaling is a type of supervisory line signaling that uses DC signals on separate leads, called the "E" lead and "M" lead, traditionally used in the telecommunications industry between telephone switches. Various mnemonic names have been used to memorize these letters, such as Ear and Mouth, the most common variation [22].
E&M was originally developed to allow PABXs in different geographic locations to communicate over an analog private circuit. Some digital interfaces such as Channel Associated Signaling also use versions of E&M

2.5. Loop dialing M signaling. E&M

Is considered an obsolete technology for new installations, which generally use Basic Rate (BRI) or Primary Rate (PRI) digital interfaces. The Loop Dialing Interface Shall support Loop Extension

3. Subscriber line audio processing circuit

The Next Generation Octal Subscriber Line Audio processing Circuit (SLAC) device, in combination with the SLIC device, implements a DSL friendly, with a high density of eight-transmission channels universal telephone for to make interface line with this idea this design made at a very cheap cost and high performance, fully software programmable line interface with worldwide applicability [23]. All AC, DC and signaling parameters are programmable via a microprocessor interface. The SLAC has an integrated test toolbox and uses VCP test primitives and host routine capabilities to resolve faults to the line or line circuit.

3.1. Features

- Optimized for Next Generation Broadband xDSL and triple play applications
- Eliminates transients that could cause CRC errors
- Best-in-class GR-844 equivalent testing capability
- Ideal for high density, medium and large line count applications
- API-compatible with VE790 Series designs
- The high-performance digital signal processor provides programmable control of all major line card functions
- DTMF and MODEM Tone Detection

3.2. Subscriber line integrated circuit

The SLAC device is considered as a next generation device which is DSL friendly and high-density of universal telephone line interface. This enables the design of a low cost, high performance, fully software programmable line interface with worldwide applicability. All AC, DC and signaling parameters are programmable. Additionally, the NGCC has integrated self-test and line-test capabilities to resolve faults to the line or line circuit.

3.2.1. Features

- Designed to minimize POTS transients, optimizing CRC performance for triple play applications
- Best-in-class GR-844 equivalent testing
- Fully validated test primitives and host routines
- Guaranteed performance parameters
- Optimized for best-in-class density
- The monitor of two-wire interface voltages and currents supports:
- Voice transmission
- Internal ringing generation
- Programmable DC feed characteristic
- Current limited and independent of battery
- Selectable off-hook and ground-key thresholds.

3.3. CODEC

The device of SLAC identifies the caller and Data access arrangement creates a medium between the data receiver and sender. implements all the voice functions necessary to properly terminate and monitor the customer premises side of a PSTN line and provide linear or G.711 A- or µ-Law encoded voice output over a standard PCM or GCI highway. The idea behind SLAC device is to use voice-enabled DSL modems to the lifeline POTS and also supports PBX. This device reduces system-level cost, space, and power by achieving a high level of voice integration and adds programmability of transmission and signaling features [24]. It is designed for the low cost, efficient utilization of power and simply designed.

3.3.1. Features

- In combination with a DAA, provides a complete phone line termination-to-digital interface solution.
- Fully programmable SLAC device
- Disconnect, Ringing signal, Line-in-use and Line polarity detection,
- Line supervision for parallel devices connecting to the subscriber line
- Minimal external discrete components required

- Compatible with solid state or transformer DAA interfaces
- High speed, pin-selectable PCM/MPI or GCI interface
- Microprocessor interface
- GCI interface option

3.3.2. DAA

LITELINK III is single-package silicon of the phone line interface (PLI) DAA which is used to invoice and data communication process that makes the connection between the low-voltage equipment and the high-voltage telephone networks. It provides a high-voltage isolation barrier, AC, and DC phone line terminations, and switch hook, 2-wire to 4-wire hybrid, ring detection, and on-hook signal detection. It can be used for the purpose of both the differential and the single-ended signal applications. LITELINK uses on-chip optical components and a few inexpensive external components to form a complete voice or high-speed data phone line interface [25]. It can also avoid isolation and always interface with these configurations. It includes the required high-voltage isolation barrier in a surface-mount SOIC package. The CPC5620 (half-wave ringing detect) and CPC5621 (full-wave ringing detect) build upon IXYS Integrated Circuits Division's LITELINK product line, with improved insertion loss control, improved noise performance, and lower minimum current draw from the phone line [2]. The new mode pin enables worldwide implementation.

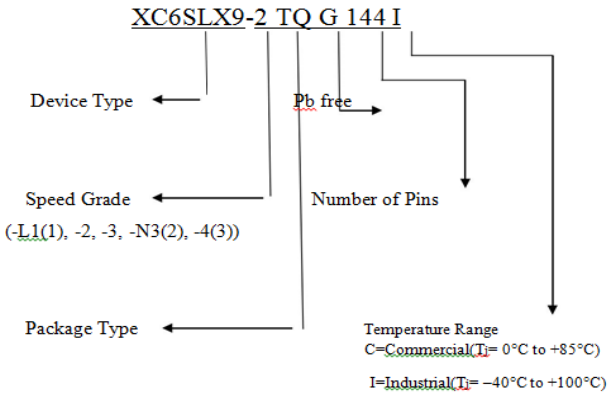


Fig. 3: FPGA Device Description.

3.3.3.1. Features

- Superior voice solution with low noise, excellent part-to-part gain accuracy
- 3 kVrms line isolation
- Data access arrangement (DAA) solution for modems at speeds up to V.92
- 3.3 or 5 V power supply operation
- Caller ID signal reception function
- Easy interface with modem ICs and voice CODECs
- Worldwide dial-up telephone network compatibility
- CPC5620 and CPC5621 can be used in circuits that comply with the requirements of TIA/EIA/IS-968 (FCC part 68), UL1950, UL60950, EN/IEC 60950-1 Supplementary Isolation compliant, EN55022B, CISPR22B, EN55024, and TBR21

3.4. SHDSL

The SHDSL Transceiver is designed to fulfill the ITU G. Shdsl. Bis standard as well as EFM standard.

3.4.1. Ethernet in first mile

Ethernet in the first mile (EFM) refers to using one of the Ethernet families of computer network protocols between a telecommunications company and a customer's premises [3]. From the customer's point of view, it can be a milestone for the efficient network "the first" mile, although from the access network's point of view it is known as the "last mile". For bringing the Ethernet packets directly from the Central Office Side (CO) to the end user (CPE: Customer Premise Equipment) Over voice-grade copper wires the Ethernet community standardized in IEEE 802.3-2004. Ethernet First Mile (EFM or Ethernet Internet) is a designed low-cost technology and also cost-cutting strategy over the traditional fiber leased lines, it also brings mission-critical connectivity which will be able to each even the small business/vendors too. EFM provides symmetrical bandwidth at speeds of up to 20 Mbps with no contention.

3.4.2. Features

- The chip provides a fully integrated solution to the Ethernet, ATM, Packets and TDM transport over 4, 2 or 1 SHDSL channels
- In compliance with:
- ETSI SDSL (ETSI TS 101 524 V 1.2.1)
- ETSI SDSL.bis (ETSI TS 101 524 V 1.2.2)
- ITU G.shdsl (ITU-T G.991.2)
- ITU G.shdls.bis (ITU-T G.991.2 (2004))
- ITU G.hs (ITU-T G.994.1)
- Integrated Controller for start-up and channel bundling (PAF, M-PAIR)
- Fully integrated RAM for Complete FW and bonding delay compensation
- Modes: – STU-C, STU-R, STU-C/R – Analog, digital and remote loopbacks
- Prepared for Near End Self-Cross Talk Cancellation with separate FW
- DSLAM: Packet over SHDSL Line-card

4. Spartan 6 FPGA (xc6slx9-2tqg144i)

4.1. General description

The Spartan-6 families provide leading system integration capabilities with the lowest total cost for high-volume applications. There are 13 member families which deliver the expansion of densities that ranging from 3,840 to 147,443 logic cells, with half the power consumption of previous Spartan families, and faster, more comprehensive connectivity. Built on a mature 45 nm low-power copper process technology that delivers the optimal balance of cost, power, and performance, the Spartan-6 is the family which offers more efficient, also dual-register 6-input as see in the table (LUT) logic and a rich selection of built-in system-level blocks. These include 18 Kb (2 x 9 Kb) block RAMs, second-generation DSP48A1 slices, SDRAM memory controllers, enhanced mixed-mode clock management blocks, Select IO™ technology, power-optimized high-speed serial transceiver blocks, PCI Express® compatible Endpoint blocks, advanced system-level power management modes, auto-detect configuration options, and enhanced IP security with AES and Device DNA protection.[4] These features provide a low-cost programmable alternative to custom ASIC products with unprecedented ease of use. Spartan-6 FPGAs offer the best solution for high-volume logic designs, consumer-oriented DSP designs, and cost-sensitive embedded applications. Spartan-6 FPGAs are the programmable silicon foundation which will be targeted on the Design Platforms that deliver integrated software and hardware components which enable these designers to more focus on the innovation as well as their development cycle begins tool produced by Xilinx for synthesis and analysis of HDL Designs enabling the developer to synthesize ("compile") their designs, perform timing analysis, examine RTL diagrams, simulate a design's reaction to different stimuli, and configure the target device with the programmer.[15] Xilinx ISE is a design environment for FPGA products from Xilinx, and is tightly-coupled to the architecture of such chips, and cannot be used with FPGA products from other vendors. The Xilinx ISE is primarily used for a circuit which will be synthesis and design efficient, ISIM or the Sim Model logic simulator is used for the system-level testing. Other components shipped with the Xilinx ISE include

the Embedded Development Kit (EDK), a Software Development Kit (SDK) and Chip Scope Pro [16].

5. Simulation and synthesis analysis results

5.1. UART

A UART (Universal Asynchronous Receiver/Transmitter) is the microchip which will be programmed to controls a computer's interface and also attached all the serial devices. Specifically, it provides the computer with the RS-232 Data Terminal Equipment (DTE) interface so that it can "talk" to and exchange data with modems and other serial devices. [5]

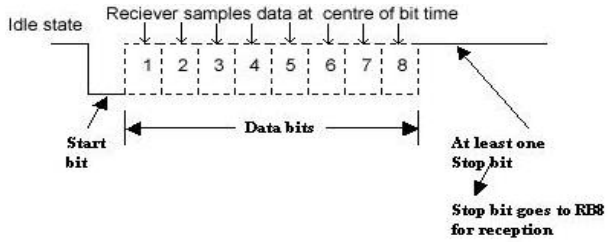


Fig. 5.1: UART Transmission.

In the above transmission, there are [8] data bits no parity, and 1 stop bit as shown in the Figure 7.1. Note that the LSB of the data word is transmitted first. No clock information is conveyed through the serial line. Generally transmission starts, when the transmitter and receiver must set of parameter in advance, that include the baud rate, also the number of data bits and stop bits, are used for parity bit. The commonly used baud rates are 2400, 4800, 9600, and 19,200 bauds. [6] We illustrate the design of the receiving and transmitting subsystems in the following sections. The design is customized for a UART with a 19, 200 baud rate, 8 data bits, 1 stop bit, and no parity bit.

5.2. UART transmitter subsystem

The UART transmitter is essentially a shift register that shifts out data bits at a specific Rate. The rate can be controlled by one-clock-cycle enable ticks generated by the baud rate generator. There is no oversampling in that UART receiver. Instead of introducing a new counter, the UART Transmitter usually shares the baud rate generator, and normally it receives the internal counter to track the enabling ticks. [7].

After assertion of the tx _ start signal, the FSMD loads the data word and then gradually progresses through the start, data, and stop states to shift out the corresponding bits. It signals completion by asserting the tx-done-tick signal for one clock cycle. [8]

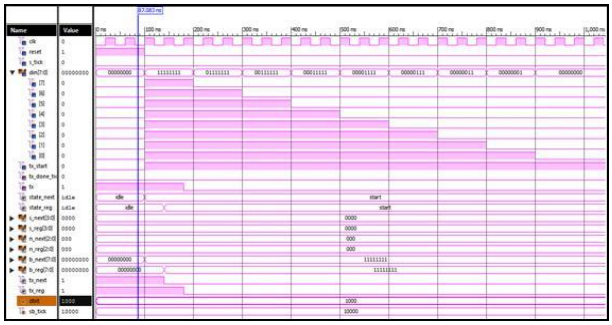


Fig. 5.2: UART Transmitter with Parallel Data Input.

5.3. UART receiving subsystem

The D-BIT constant indicates the number of data bits, and the SB-TICK constant indicates the number of ticks needed for the stop bits, which is 16, 24, and 32 for 1, 1.5, and 2 stop bits, respectively. DBIT and SB-TICK are assigned to 8 and 16 in this design. [9]

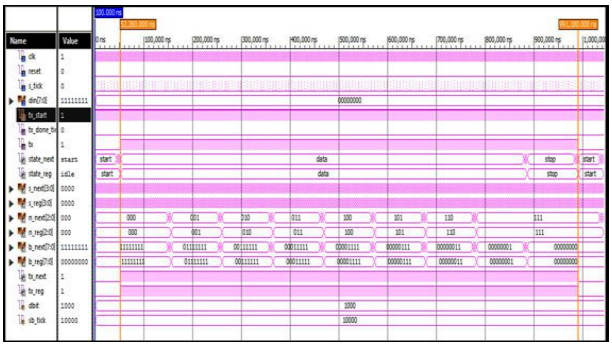


Fig. 5.3: UART Transmitter with Serial Data Output.

The receiving subsystem includes three major states, start, data, and stop, which represent the processing of the start bit, data bits, and stop bit. The S - Tick signal is the enable tick from the baud rate generator and there are 16 ticks in a bit interval. Note that the FSMD stays in the same state unless the S - Tick signal is asserted [10]. So there will be two counters are S and N registers. The s register keeps track of the number of sampling ticks and counts to 7 in the start state, to 15 in the data state, and to SB-TICK in the stop state. The N register keeps track of the number of data bits received in the data state. The retrieved bits are shifted into and reassembled in the b register. A status signal, Rx-done-tick, is included. It is asserted for one clock cycle after the receiving process is completed

5.4. Baud rate generator

It creates a signal frequency, which is exactly 16 times of the UART's baud designated rate. To avoid creating a new clock domain and violating the Synchronous design principle, the sampling signal should function as enable ticks rather than the clock signal to the UART receiver. [11]

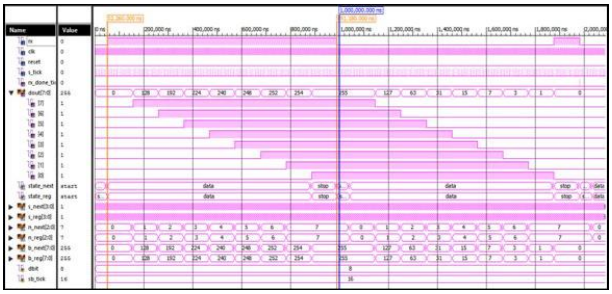


Fig. 5.4: UART Receiver with Serial Data as Input and Parallel Data as Output.

5.5. Reset and sync pulse generator

There are three clocks with respect to FPGA, viz., Reference Clock of 40.96 MHz, Local Oscillator 32.768MHz and Line Card of 32.768MHz. We are connecting these three clocks to FPGA Pins 121, 132 and 143. Shdsl_clk-input (40.96 MHz) refers 121 pin, local_ref_32mclk-input (32.768 MHz) refers to 132 pin and pll_ref-32mclk-input (32.768MHz) refers to 143 pin. [13]

Reference Clock will be constant and the two clocks local oscillator and line card clock will vary their clock frequencies, so that clock selection block is needed to select 32.768 MHz clock as an input to FPGA.

Fig. 5.5: Mod_163 Counter Max Tick.

Fig. 5.6: Mod_163 Counter Simulation.

For the 9600 baud rate, the sampling rate has to be 153600 (i.e., 9600*16) ticks per second. Since the system clock rate is 25 MHz, the baud rate generator needs a mod-I63 (i.e.25MHz/153600)counter, in which the one-clock-cycle tick is asserted once every 163 clock cycles. [12].

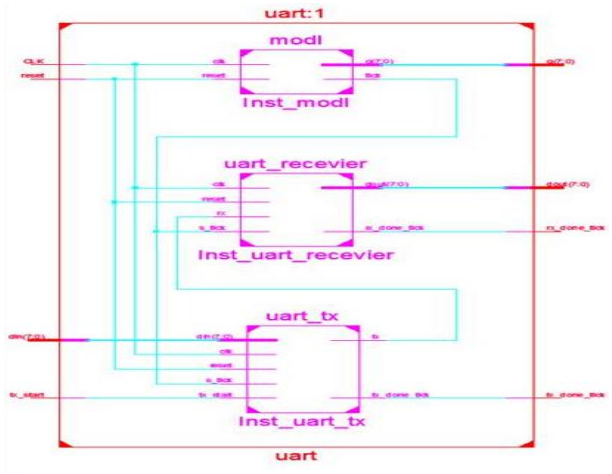


Fig. 5.7: UART RTL Schematic.

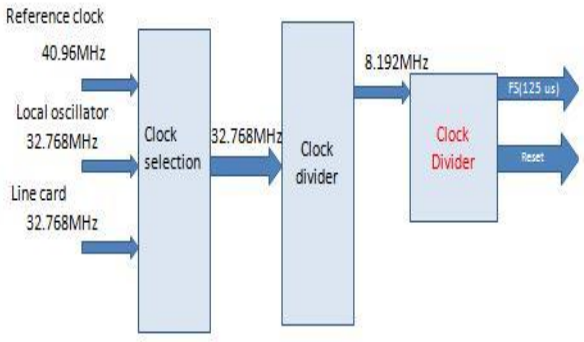
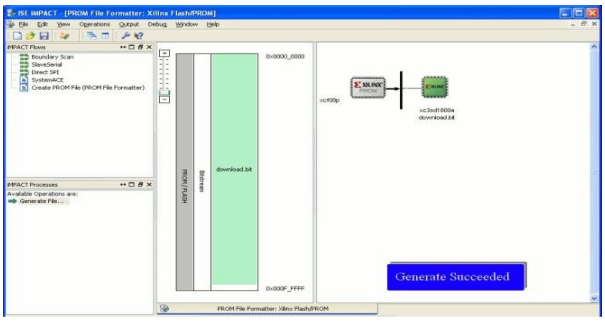


Fig.5.8: Reset and Sync Pulse Generator.



The Selected 32.768MHz out is connected to Clock Divider to get PCLK 8.192MHz and fs 125 us. These PCLK and fs outputs are given to FXO and FXS pins in FPGA. From PLCK reset of 300, US will be generated. [14]

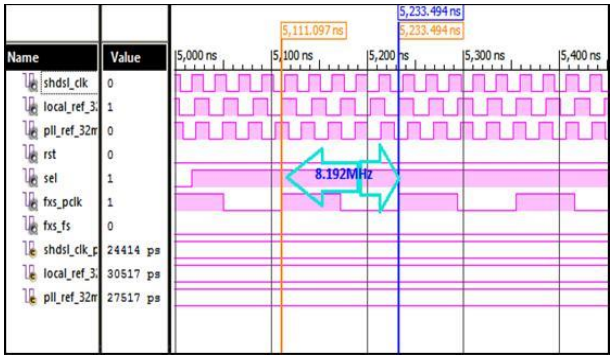


Fig. 5.9: PCLK 8.192 MHz.

From the available clocks (local _ ref and Pll _ ref) the clocks divider will be provided with a 32.768MHz frequency (30.517 ns) using an SEL line. The clock divider performs frequency division operation where 32.768MHz (30.517 ns) will be down to 8.192Mhz (122 ns).

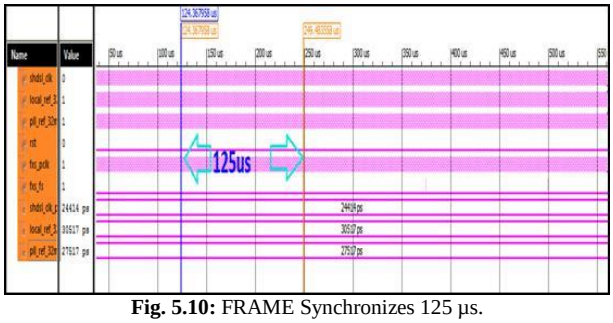


Fig. 5.10: FRAME Synchronizes 125 µs.

Using another clock divider circuit and 8.192Mhz as input we will get the output as 125µs.This is provided as FS (frame sync) for FPGA interfacing circuits

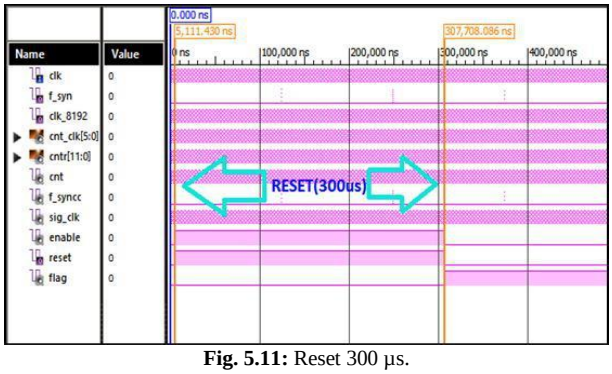
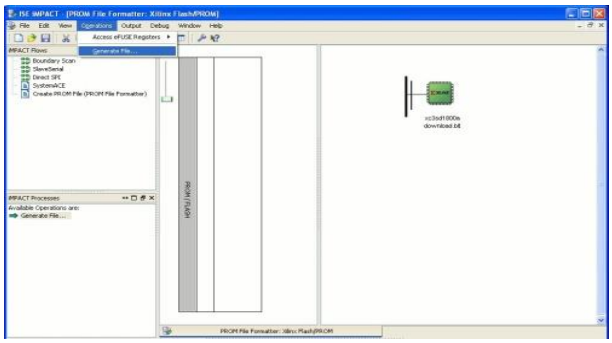


Fig. 5.11: Reset 300 µs.

Using the same circuit and 8.192MHz clock we can able to get the RESET pulse of 300µs

Hardware implementation in FPGA
Select "operations / generate file..." or double click "generate file..." from the iMPACT processes panel



You should see the following message in the main panel: generate succeeded.

6. Conclusion

This Project main aim is to provide data and voice services to the user in small deployment in one single subscriber card called combo card that consists of fully software programmable devices viz., Subscriber Line Audio Processing Circuit IC, Subscriber Line Integrated Circuit, Lite Link III DAA IC, FPGA and Micro Controller. The Microcontroller acts as Master and FPGA act like Slave. Interfacing the Programmable devices in the Combo Card with FPGA has done through Communication Protocols. The Communication from Microcontroller to FPGA is like Master in Slave Out and Master out Slave in. There are three clocks coming to FPGA one is from Line Card, Local Oscillator, and Reference Clock, We Selected 32.768 MHz Clock which is coming from line card by clock selection and divided the clock by 4 times by clock divider and generated 8.192 MHz and 125µs to give FXS and FXO and calculated total output power.

Table.1: Output Power

Clock	32.768 Mhz
Frequency	8.192 Mhz
Output Power	9 Mw

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