International Journal of Engineering & Technology, 7 (2.33) (2018) 767-770

International Journal of Engineering & Technology

Website: www.sciencepubco.com/index.php/IJET

Research paper

Design strategy for flying capacitor multilevel converter based on PSC-PWM

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Abstract

This paper presents flying capacitor multilevel converters. This is the new multilevel topology with the concept of phase-shifted carrier pulse width modulation which will generate the signals. This signal will generate by using phase-shift carrier with modulating signal. The execution of proposed structure of this technique is shown with the help of waveforms. The advantages of this proposed topology is shown in the simulation. All possible switching states are explained in the modulation strategy. The different performance of proposed topology is compared with other flying capacitor multilevel structures. Simulation result for all the switching states are explained with respective waveforms. Proposed topology is superior to the other flying capacitor multilevel structure from different standpoints. And mainly, it reduces the number of high frequency switches, the number of flying capacitor and at the same time it improves the quality of output voltage. The experimental setup is used to validate the modulation strategy and other theoretical findings.

Keywords: *DC-AC Converter; Flying Capacitor Multilevel; Multilevel Converter; Phase-Shift Carrier Pulse Width Modulation.*

1. Introduction

The industrial equipments were consuming high power due to the development of high power converter and switches. Then this problem can be solved by using multilevel converter. It has moderate voltage and current devices. Multilevel converter has improvement in voltage quality and switching frequency is low. So it has less switching loss and higher efficiency.

There are three types of multilevel converter. They are – cascaded H- bridge (CHB) converters, the neutral point clamped (NPC) and the flying capacitor (FC) converters. The main advantage of this converter is reducing components size and because of this it increase reliability. It has feature of transformer less operation, it attracted the attention of industry. Here, by using hybrid multilevel converter combination of dc link inverter and double flying capacitor multilevel inverter. The main advantages of this proposed system is reducing number of switches and capacitor than other system. By reducing number of switches and capacitor, it can reduce the size and cost of the converter at the same time it can improve reliability and efficiency. The basic operation of this topology is explained by varying frequency switches. The simulation and experimental result is shown.

2. Proposed structure

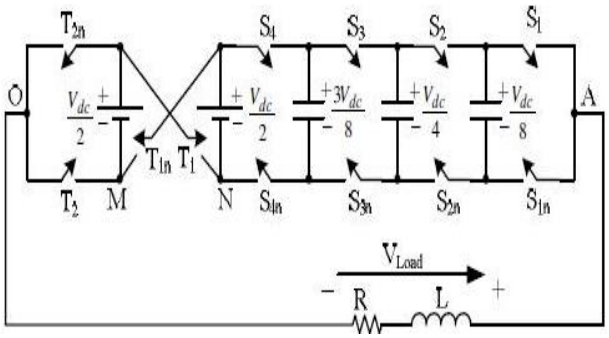

Fig. 1: Circuit Diagram of Proposed Structure

In proposed system, quadruple flying multilevel converter is used. It uses two switches, one is low frequency switch and another one is high frequency having capacitor and two switches at constant frequency. The switches used in proposed structure are IGBT and connected in anti-parallel direction. It has n number of cell and each cell consists of two switches and voltage. The voltage of capacitor m is mVdc/2n. T1 and T1n are line frequency switches operating in output frequency. T2 and T2n is low frequency switch which are thrice the line frequency switches. If it is single phase, then it needs two dc sources. If it is three phase, then we need six dc sources.

2.1. Working principle

The above diagram is the circuit diagram for proposed structure. In proposed system, it has four cells and each cell consists of two

switches. Therefore, totally we are using eight switches. We get output has step waveform with both positive and negative voltage peaks. The number of steps in the waveform depends on switches. The voltage waveform produces 2n+1 level. These levels are equally distributed in positive and negative voltage peaks. It uses two similar voltages with voltage amplitude of Vdc/2 and three flying capacitors with voltages Vdc/8, Vdc/4 and 3Vdc/8. This will produce an output voltage. The operation can be done by varying on and off state of switches in the cell. The line and low frequency switches also vary their state. By doing this, it will give 17 levels of voltage waveform.

2.2. Switching states

Table 1: Switching States of Proposed System & its Voltage

		States of switches	No. of
VAO	T2T1	S4 S3 S2 S1	redundant states
Vdc	1 1	1 1 1 1	1
+7Vdc/8	1 1	1 1 1 0/ 1 1 0 1/ 1 0 1 1/ 0 1 1 1	4
+6Vdc/8	1 1	1 1 0 0/1 0 0 1/ 0 0 1 1/ 1 0 1 0/ 0 1 0 1/ 0 1 1 0	6
+5Vdc/8	1 1	1 0 0 0/ 0 1 0 0/ 0 0 1 0/ 0 0 0 1	4
+4Vdc/8	1 1 0 1	0 0 0 0 1 1 1 1	2
+3Vdc/8	0 1	1 1 1 0/ 1 1 0 1/ 1 0 1 1/ 0 1 1 1	4
+2Vdc/8	0 1	1 1 0 0/ 1 0 0 1/ 0 0 1 1/1 0 1 0/ 0 1 0 1/0 1 1 0	6
+Vdc/8	0 1	1 0 0 0/0 1 0 0/ 0 0 1 0/0 0 0 1	4
0	0 1 1 0	0 0 0 0 1 1 1 1	2
-Vdc/8	1 0	1 1 1 0/ 1 1 0 1/ 1 0 1 1/ 0 1 1 1	4
-2Vdc/8	1 0	1 1 0 0/ 1 0 0 1/ 0 0 1 1/1 0 1 0/ 0 1 0 1/ 0 1 1 0	6
-3Vdc/8	1 0	1 0 0 0/0 1 0 0/ 0 0 1 0/ 0 0 0 1	4
-4Vdc/8	1 0 0 0	0 0 0 0 1 1 1 1	2
-5Vdc/8	0 0	1 1 1 0/ 1 1 0 1/ 1 0 1 1/ 0 1 1 1	4
-6Vdc/8	0 0	1 1 0 0/1 0 0 1/ 0 0 1 1/ 0 1 0 1/ 0 1 0 1/ 0 1 1 0	6
-7Vdc/8	0 0	1 0 0 0/ 0 1 0 0/ 0 0 1 0/ 0 0 0 1	4
-Vdc	0 0	0 0 0 0	1

In switching states, it has two low frequency and line frequency switches. And it also has number of switches used in cells. The switches in the cells are S1, S2, S3, S4 and S1n, S2n, S3n, S4n.
Above table show the various switching states. By changing the line and low frequency high and low we get some state of switches. That will generate the pulse and give approximate sinusoidal waveform.
Similar to FCM-based topologies, to preserve the flying capacitors voltages at desired levels modulation and control scheme is necessary. There are two major flying capacitor voltage balancing schemes they are natural balancing and voltage sensing.

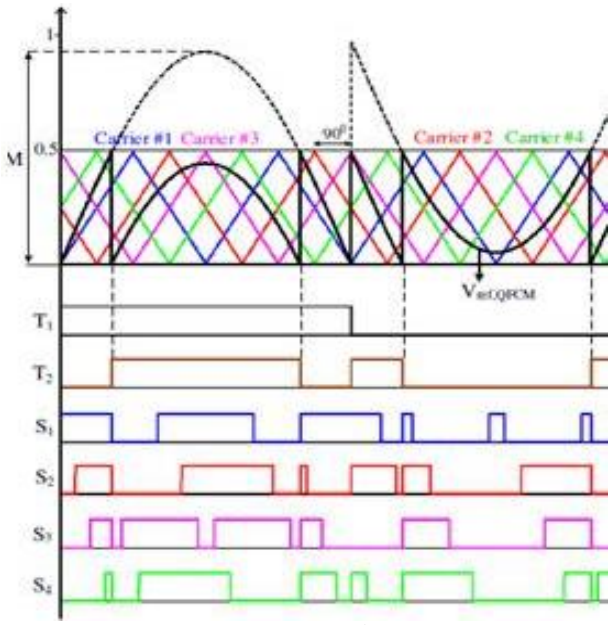

Fig. 2: (A) Modulation Strategy of Proposed Structure.

The natural balancing which utilizes the balance booster filters parallel to the output load in conjunction with PSC-PWM. The second method is to use voltage sensing circuits along with proper control scheme. This scheme is well known is both the converters like flying capacitor and cascaded H-bridge. The attractive features of PSC-PWM are uniform power losses, modularity and improved output frequency spectrum. Now lets us see about modulation strategy diagram
To explain the proposed modulation method, the desired output voltage reference signal, Vref, shown by dashed graph, and the modified reference signals, Vref,mdf and Vref,QFCM, shown by solid graphs in the same Fig., are defined as

$$Vref = M \sin(2pfot + d)$$

$$Vref, mfd = Vref - sgn(Vref)\ 2$$

$$Vref, QFCM = Vref, mdf + \frac{1 - sgn(Vref, mdf)}{4}$$

Where, M is modulation index and function sgn(x) is equal to 1 if x>0 and -1 if x<0.
By comparing reference signal and carrier signal of four cells it gives that waveform. For each carrier and reference signal comparison it gives different voltage levels. Here, we have model diagram of 17- levels which have shown in the below diagram. The positive cycle is denoted as +Vdc and the negative cycle is denoted as –Vdc. In below waveform we can only see the one cycle of waveform. When we connected this circuit to the load then, we will get continuous cycle like this.

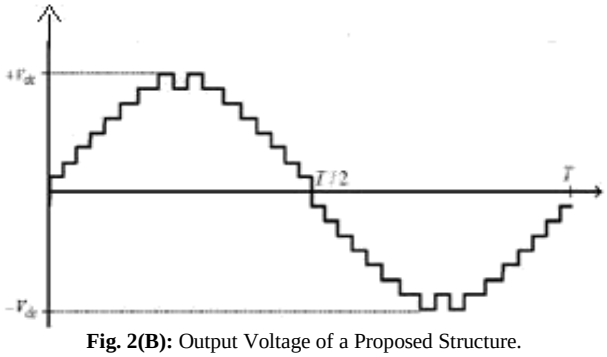

Fig. 2(B): Output Voltage of a Proposed Structure.

2.3. Comparisons of conventional FCM and proposed FCM

In this section, comparison is made between FCM topology and DFCM, QFCM topology. Here, the level used is Nlevel=2n+1 and peak output voltage is denoted as Vdc. The current rating of the switch is same for same family. Here, all the three converters are belonging to same family. QFCM converter has halved number of high frequency switches. The other two converters have same number of frequency. Flying capacitor is used instead of electrolytic capacitor because it provides smooth dc voltage but it relatively have high failure rate and short life time. Therefore, electrolytic capacitor is replaced by flying capacitor.
Flying capacitor will reduce cost as well as it improves its reliability. It is connected in series or parallel connection to get desired output voltage and current. This topology depends on voltage as well as current rating of the system. The proposed structure not only decreases the flying capacitor but also decrease the voltage rating. The total output voltage rating provides similar voltage levels.

Table 2: Comparison of Conventional FCM-Based Converter and QFCM Converter

Type of Multilevel Converter	No. of Cells	No. of LF Switches (A)	Blocking voltage of LF Switches (B)	Total Blocking Voltage of LF Switches (A*B)
FCM	2n	0	0	0
DFCM	N	2	Vdc	2Vdc
QFCM (n is even)	n/2	4	Vdc and Vdc/2	3Vdc

The output voltages level is calculated as,
N/2-1n/2-1

$$VQFCM = \sum vck = \sum k.Vdc/n = (n-2)/8Vdc$$

k=1, 2, 3, k=1, 2,
Where,
n=2, 3, 4, For DFCM
n=2, 4, 6, for QFCM
The proposed structure requires three flying capacitor voltages equal to Vdc/8, Vdc/4 and 3Vdc/8. And the voltages Vdc/8, Vdc/4, 3Vdc/8, Vdc/2, 5Vdc/8, 3Vdc/4 and 7Vdc/8 for seven flying capacitor. In proposed topology their will reduction in voltage ratings. Here, the dc sources are replaced by capacitor and also multiple dc sources are realized by transformer and rectifiers. The multiple dc source topologies can be potentially efficient, robust and reliable in renewable energy applications. The application areas where these converters may prove useful in FACTS controllers applications are identified. In FCM it have simple input transformer and both DFCM and QFCM have multi secondary input transformer.

3. Simulation results

In simulation result, it shows the waveform of the proposed system. The waveform is the comparison of both reference signal and carrier signal. Here, we have many waveforms related to this proposed structure. The output voltage has a staircase waveform with steps of 1250V. The Output voltage has THD 7.3% and output current have THD of 1.1 %. From the comparison, it conclude that it have more advantages than others.
The simulation results are based on the parameters given in table III. It shows the various parameter which is related to this simulation.

Table 3: Parameters of Proposed System

System Parameter	Value
DC sources voltage(Vdc/2)	5KV
Capacitance of flying capacitors	1000 µF
PSC-PWM carrier frequency(fc)	1250Hz
Fundamental output frequency(fo)	50Hz
Modulation index(ma)	0.95
Order of harmonic frequency for THD calculation	500
Load resistance and inductance (RL,LL)	20ohm, 40mH

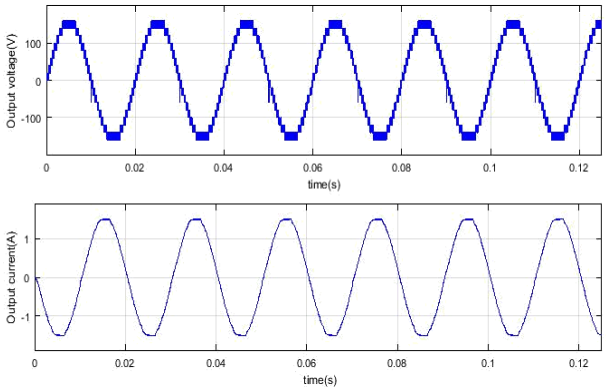

Fig. 3: Output Voltage and Load Current.

A 9-level QFCM converter and a 9- level DFCM converter are simulated and their output voltage quality is compared here. Both have similar carrier frequency is assumed for high-frequency switches of converters. The performance of the proposed MR-PSCPWM technique to regulate and balance the voltage of flying capacitors has been studied during both steady-state and transient-state conditions. The nominal flying capacitor voltages are 1250V, 2500V and 3750V. The load used in this topology is RL-load, the converter is in steady stat condition with time t=0.35sec. This time taken only for the value of modulation index is 0.95. If the value of modulation index is reduced then the time taken will also increased to t=0.46sec. so, we preferred the modulation index value near to one. The generated gate pulses are also some waveforms. For each switch it has different waveforms. Let's see one by one of the gate pulse from the modulating strategy. Totally, it has six gate pulses waveform. That means each phase have two pulses. Let us us some gate pulse of this proposed structure.
topologies required two additional LF switches operating at Vdc, and the proposed topologies requires two LF switches operating at Vdc plus two LF switches operating at Vdc/2. The THD of output voltage for 9-level QFCM is 15%and number of high frequency switches are [4]. The THD of output voltage for 17-level QFCM is 7.3%.

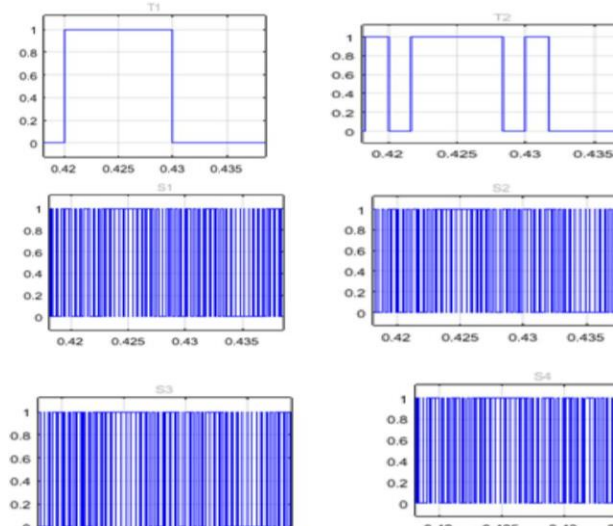

Fig. 4: Generated Gate Pulse Waveform.

The output of this proposed structure is shown in the below diagram. It have 17-level staircase type waveform with reduced harmonics distortion.

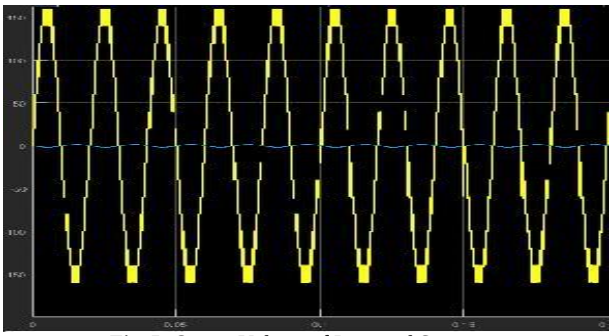

Fig. 5: Output Voltage of Proposed Structure.

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