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Research paper

FPGA implementation of 1000base-x Ethernet physical layer core

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Abstract

This paper introduces the field programmable gate array FPGA implementation of 1000BASE-X PHY Physical Layer for gigabit Ethernet over fiber optic cable. The implementation is achieved by developing VHDL model for all its building blocks including the physical coding sub layer, PCS, and the physical medium attachment, PMA. The VHDL code is simulated using XILINX ISE14.7 and synthesized on Xilinx Virtex6 FPGA chip. Measured results show that the designed and implemented Ethernet transceiver works successfully at 1.32 Gb/s, 2.5V supply with reduced power consumption.

Keywords:*Giga Ethernet;virtex6 FPGA;PHY; PCS; PMA;8B/10B Coding; Synchronization; PISO; SIPO.*

1. Introduction

The Gigabit Ethernet, GE innovation is an expansion of the 10/100-Mbps Ethernet standard. The physical layer describes how bits in a packet of Ethernet are transmitted over a communication link and specifies encoding and decoding techniques. For a MAC operating at a speed of 1Gbps, the Gigabit full Media Independent Interface GMII is utilized. GMII provides independent 8-bit wide for transmitting and receiving data paths. The GMII is operating at 125MHz.The physical layer PHY is partitioned in three sublayers; the physical coding sub layer PCS, the physical medium attachment PMA and the physical medium dependent sub layer, PMD[1]. The PCS and PMA sub layers are called the core of the physical layer. In PCS sub layer one utilizes encoding, decoding and synchronization state machine. So, in the transmitter (TX_PATH) side, one deals with how to encode the information during transmission and what are the rules to follow to encode them. Similarly, in the receiver side, one provides how to decode the information and what are the rules to follow to decode them. PMA sublayer serializes the code group for transmission as well as de-serializes the bits that received and forward them to PCS receiver. SERDES operates as parallel to serial converter in the transmitter side and the reverse in the receiver side [1]. In this paper a proposed hardware model for this physical layer is synthesized and simulated by XILINX ISIM simulator and the results obtained are presented. Many research contributions have been done to design different Ethernet systems by different languages and most of them are not focused on IEEE802.3Z standard (1000BASE-X). The transceiver proposed in [2], focus on the implementation of the DSP section of 1000BASE-T transceiver. 1000base-T (GE over Category-5 copper cabling) is not defined at a serial gigabit rate, it is defined over four unshielded twisted pairs UTP at 250Mbps per pair. 1000BASE-X proposes to use TBI (8b/10b) encoding whereas 1000BASE-T uses 4D-PAM5. So, the major difference between our design and the other in [2] is that it is compatible with existing 8b/10b.The authors in [3] provides the GE standard implementation results on the FPGA using Altera' s Stratix-II GX device. Implementation, verification and synthesis of the Gigabit Ethernet PCS is presented in [4], where it provides 1 GE signal transmission across UTP cable by using 5-level coding scheme. The PCS of this standard was simulated by using Verilog HDL. Design and implementation of data transmission via dual independent aurora channels on one Gigabit transceiver on FPGA virtex-5 utilizing aurora protocol is proposed in [5]. 8b/10b encoding SerDes circuit is considered in [6], it was designed by XILINX Verilog. In [7], coverage analysis of the 8b/10b encoder verification and 8b/10b encoder RTL code is simulated by Questasim.We introduce in our paper FPGA implementation of 1000base-x transceiver by VHDL language on XILINX virtex6 ML605(XC6VLX240T device, FF1156 package) FPGA that is a High performance embedded system with advanced serial connectivity, and we analyze our design results on chipscope by JTAG cable which is used to download the programming file (BIT file) from PC into the target hardware board. As well we simulate it on Xilinx ISE14.7 simulator. We propose 1 GB/s over fiber because of its advantages versus 1000base-T, due to its higher transmission speed, in addition to DC balanced data stream that proves the advantages of fiber optic connections that results from existing 8b/10b encoding. Therefore, one of the most significant purposes is to implement an 8B/10B Encoder/Decoder for Gigabit Ethernet in order to meet fast time to market requirements, its implementation is considered one of the most challenging parts of the design of this high-speed transceiver. The implemented 8b/10b coding is suited ideally for high-speed local area networks LAN and serial data links. For high performance receiver data recovery, the code has limited run length (no more than five successive zeros or ones), and guaranteed transition density. The special characters are useful in packet delimiters and a subset of them point to a unique commas that have bit pattern never repeats in the data string. Hence, it is used to define the packet boundaries in the receiving end. The additional rules which embedded in the design of this code permits the receiver for detecting most the transmission errors. In this paper an 8b/10b coding and serializer/deserializer

(SerDes) circuit has been analyzed and developed for high speed communication applications. After lots of simulation and application, the results indicate that 8B/10B code functions effectively and providing DC balanced bit stream for efficient SERDES operation which ensures that the proposed technique provided the better performance in terms of power and timing because SerDes enables the movement of a huge amount of point-to-point data while decreasing the complexity, power, cost, and board space usage compared with parallel data buses implementation. Parallel bus consumes much power and it is much difficult to route, which can be decreased by utilizing SerDes. Our paper is arranged as follows: Section two explains 1000BASE-X PCS/PMA core and its structure; Sections 3 and 4 present the simulation and synthesis results including discussions and the fifth section concludes the paper.

2. 1000Base-X PCS/PMA core

As shown in Fig. 1, the 1000BASE-X PCS/PMA core is partitioned into two major paths, one for the transmission and the other for the reception of 10 bit codes. Every path is then divided into functional blocks so; the overall 1000base-x pcs/pma core device block diagram is depicted in the Fig. 1. The core is clocked with the rising edge of the 125MHz (CLK_125MHz), both transmit and receive path use high performance phase locked loop PLL.

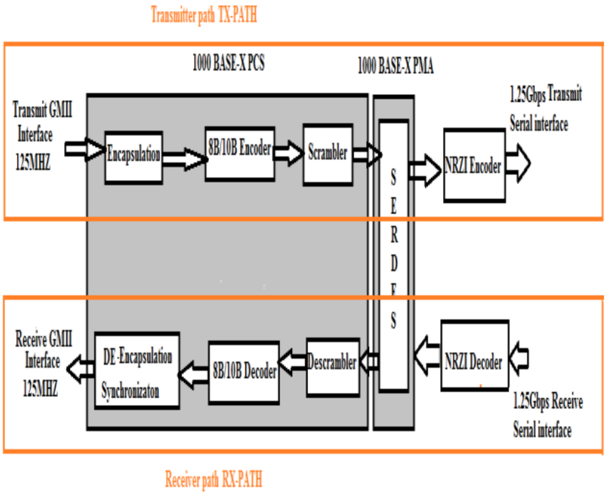


Fig.1: Block Diagram of 1000BASE-X Core.

We faced a problem while implementing this work on FPGA that we have to implement this design on available FPGA (Virtex-6 ML605).It is needed to use oscillator clock with 125MHZ which is not available on the FPGA board. There is only a socket crystal oscillator of 66 MHZ available on board (user clock) in pin “U23 s”. We suggest a proper solution to solve this problem, such that we achieved 1.32 GHZ by using parallel transmission over two lanes, where each lane operates at 660MHZ by using clock wizard (PLL) that Generates the CLK(660 MHZ) internally from 66.667 MHz clock using Xilinx clock wizard generator.Finally the data is transmitted over two independent channels as shown in Fig.2.

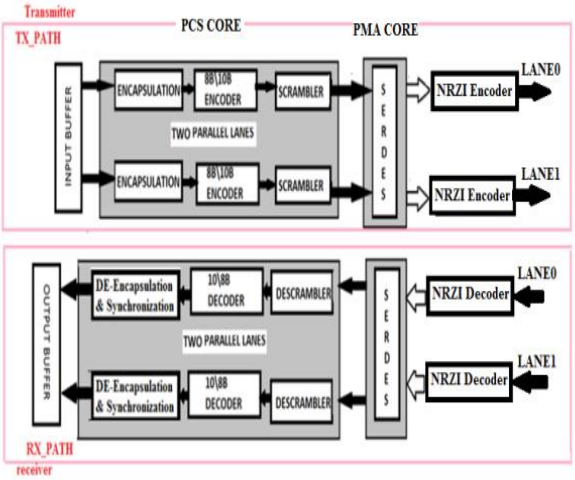


Fig.2: PCS\PMA Core over 2lanes.

2.1. 1000Base-X PCS/PMA core Transmitter

As is clear from Fig.1, PCS/PMA core transmitter includes frame Encapsulation, encoding schemes, scrambler, serializer and NRZI encoder. In the following sections, the functions of the building blocks of core transmitter will be described and its VHDL model will be designed.

Frame Encapsulation

The PCS follows a few simple rules to encapsulate the data transmitted by the MAC layer as shown in Fig. 3.It encrypts the first byte of every packet with a special code group, referred to as the /S/ code group. This code will not repeat in a normal sequence of transmitted data, and so it reliably indicates the starting of the frame. Following the /S/ code group, the Ethernet bytes are encoded using the 8B/10B coding rules. Every packet is terminated with a special code /T/. Packets contain an odd numbers of code groups (counting from the /S/ to the /T/). Between packets, the gap is filled with a two-symbol idle code group represented as /I/. The idle code is sent continuously between packets to adapt among the clock rates at each end of the link. When the PCS function receives a frame from the MAC with an error (error inserted during frame transmission),the PCS encodes the errors by sending an /E/ character.

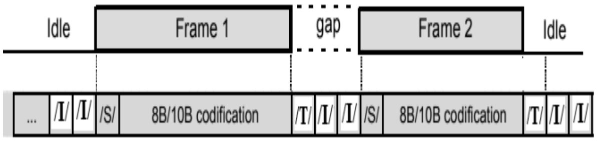


Fig.3: GE Packet after 1000Base-X Encapsulation.

8B/10B Encoding

The functional architecture of the encoder is depicted in Fig.4. Due to the quick advancement of communication technology, fiber communication becomes more popular for people due to its higher transmission speed, but high-speed fiber transmission brings a problem like unbalanced code flow so, an 8b/10b codec is designed, due to its low transmission error percent, DC balance function, with checking mistaken function through the transmission as well as special function (comma characters) which determines the beginning and the ending of each frame to achieve the synchronization. The 8b/10b coding transform a byte wide of data stream of random ones and zeros to DC balanced stream of 1s and 0s. While performing encoding operation one has to consider disparity rules. Data values are referred to in the form of DX.Y or KX.Y where D points to a data code and K points to a comma code. The X is the value of the five unencoded bits EDCBA and the Y is the value of the three unencoded bits HGF. The 8b/10b encoding architecture design consists of two sub-block codes, a 3b/4b (FGH<=>fghj), and a 5b/6b (ABCDE<=>abcdei) in addition to Running Disparity RD control. The encoded bits are transmitted with least significant bit LSB ‘a’ first and bit ‘j’ last [8]. Encoder, determines whether the data encoding or the comma encoding will be transmitted and produce the appropriate 6b and 4b codes, and determines whether the 4b and 6b codes that produced will require inversion or not as well, it defines if the transmitted encoding will flip the value of the running disparity (RD) or not, it enables long distances for transmission and more effective detection for errors, in addition to it makes synchronization of the incoming bits stream easier.

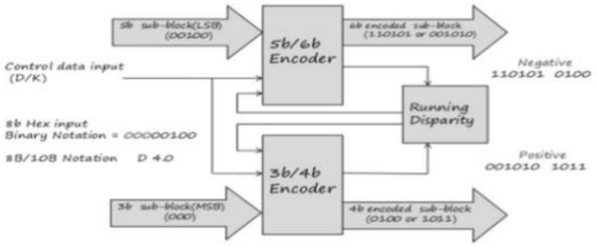


Fig.4: 8b/10b Encoder Architecture.

Disparity (RD)

RD is a technique utilized in digital communication in order tokeep a DC balance in digital transmissions. Disparity allows the receiver to detect the presence of errors that occurs over the transmission medium. RD is positive when zeros are less than ones that are transmitted, and negative when zeros more than ones are transmitted. RD is unchanged from the previous transmission if the code has an equivalent number of zeros and ones otherwise, it will be reversed [8].

8B/10B Encoder VHDL Model

The encoder functions which has been described above are modeled by VHDL and the model is depicted in Fig. 5.The encoder design includes three functions: The encoding function ENC_FUNC, is splited to 3b/4b and 5b/6b encoding schemes, the disparity generation (DIS_GEN), which defines the output disparity for every block depending on comma code K, disparity input (DIS_IN) in addition to the inputs (ABCDE FGH), and the S_GEN function that determines the control signal (S) which is needed for the encoding function. The main control for encoder module waits for the frame input to assert FRAME_IN signal to make signal assignments for the incoming data byte DATA_IN to variables AIN. HIN. This control also initializes the three building blocks in the encoding module with the signal start_enc and when the enc_func is finished, it will send enc_done to it then, the main control logic will assert the frame_out signal and will also provide the output variables AOUT…….to………..JOUT into ENCODED_DATA [0:9], to allow the next byte to be entered in the system.

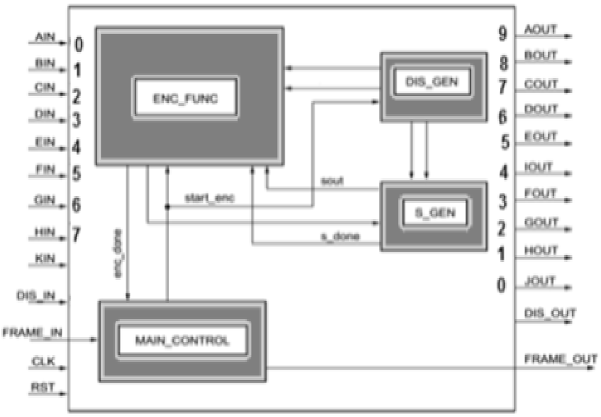


Fig.5:VHDL Model of 8b/10b.

Data Scrambler

Data scrambler uses a pseudo random binary sequence PRBS to randomize all information bits and in order not to transmit a long streams of ones or zeros. Scrambling also changes some essential components of the main message in order to make extraction of the message difficult at receiver that not equipped with a suitable descrambling device [9].We designed a self synchronized scrambler by linear feedback shift register LFSR with modulo-two addition as shown in Fig.6 .There is no necessity for the initial value, it is continuously running on all payload bits, we used scrambler with polynomial$x^7 + x^4 + 1$.

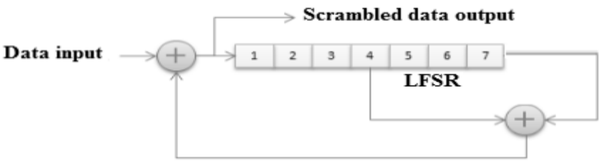


Fig.6:VHDL Model for the Data Scrambler.

Bit Serializer

It is the last module before actual transmission, its VHDL model is depicted in Fig. 7, we designed it as parallel input serial output shift register (PISO), whereas the scrambled data is applied in parallel form to parallel input pins(P0….P9) simultaneously then, it is read out from the register one bit by one bit (serial format).We used multiplexer to control between the inputs and the outputs by load signal. A serial bus can usually operate at a much higher data rate than a parallel bus so, in our design we utilized two clocks, a low speed for the parallel side and a high speed clock for the serial side. The data from the Bit Serializer is transmitted with the LSB transmitted first.

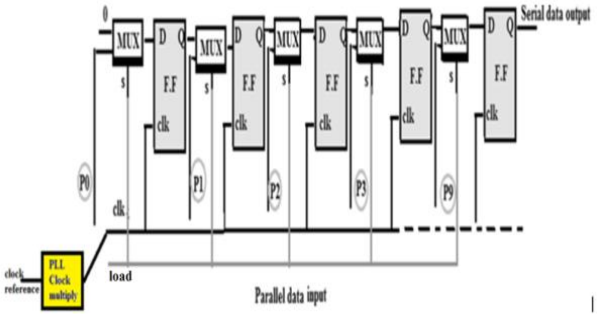


Fig.7:VHDL Model of the Bit Serializer.

Non Return to Zero Inverting NRZI Encoder

TTL binary information format are not transmitted directly over the channel. Line coding is utilized to convert the TTL format to a suitable transmission format. Most communication systems that using fiber optics, utilizes NRZI coding. In NRZI, a one is represented as a changing in state and a zero is represented as absence of a changing in state. Fig. 8 illustratesVHDL model of NRZI coding [9].

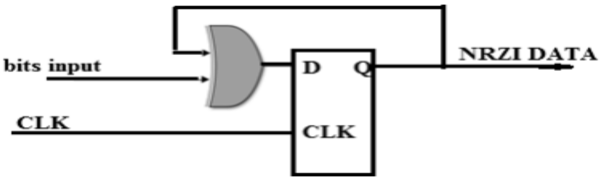


Fig.8:NRZI Line Coding VHDL Model.

2.2. 1000Base-X PCS/PMA Core Receiver

The receiver performs the inverse processes in the transmitter. The block diagram of the 1000Base-x PCS/PMA core receiver is depicted in Fig. 1together with the transmitter So, after line decoding of the received signal and converting it to TTL it will be deserialized where it is converted from serial to parallel form. Then the signal enters the descrambler after which it will be 10b/8b decoded. Finally the data will be synchronized, de-encapsulated and delivered to the GMII interface. In the following sections the building blocks of the receiver will be functionally described and then modeled in VHDL.

Non return to Zero Inverting NRZI decoder

NRZI decoder performs the reverse operation ofthe encoder in transmitter. It is designed by using Dflip flop and XOR gate as shown in Fig.9.

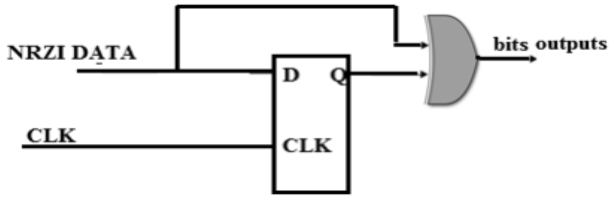


Fig.9:NRZI Decoder VHDL Model.

Bit Deserializer

Bit Deserializer performs the reverse procedure of the Bit Serializer unit in the transmitter, it is responsible for transforming the serial data into parallel data stream, no problem how they were encoded or scrambled. The LSB is received first [6]. We designed it as a serial input, parallel output shift register (SIPO) as shown in Fig.10.

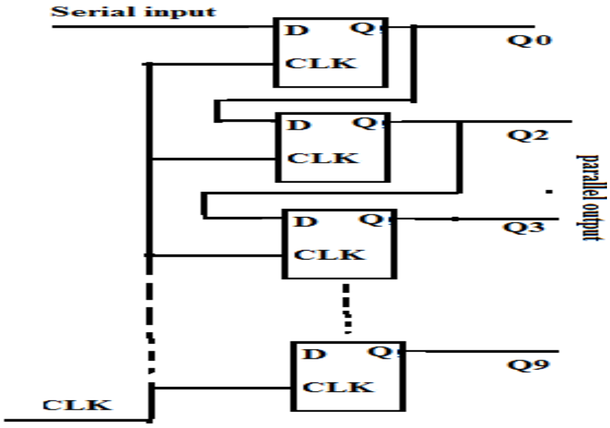


Fig.10: Bit DeserializerVHDL Model.

Descrambler

The descrambler has the same design of the scrambler and utilizes the same polynomial to recover scrambled data. We designed it by LFSR as shown in Fig.11.

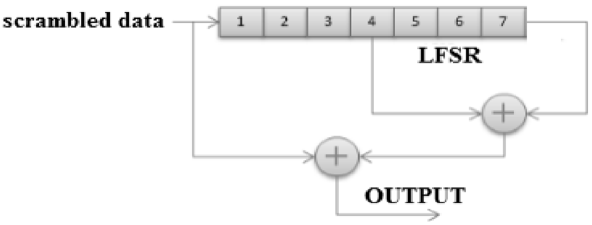


Fig.11:Descrambler VHDL Model.

10B/ 8B Decoding

The 10b/8b decoder does the disparity checking to ensure DC balancing and produces a decoded 8-bit stream of data, which is fed to the frame de-encapsulation function. In the output of the decoder, there are three status signals, k_code, valid code group and disparity error. The input code of the decoder with k_code is 1,or k_code is zero. If the input code of the decoder is existing in the code group table that specified by IEEE 802.3 clause-36, then that code group is a valid code group and generates a valid decoded data based on the input disparity else it is an invalid code. When the 10-bits code group has ones more than zeros or zeros more than ones then the disparity output must be flipped, and that 10-bits code group has no disparity error, when 10-bits code is neutral then the disparity output is equivalent to disparity input and that 10-bits code has no disparity error, otherwise it has disparity error [10].The VHDL model of decoder is shown in Fig. 12. The decoder design includes two main modules: the decoding function DEC_FUNC that defines the outputs AOUT to HOUT depending on the inputs ain to jin and errors check ERR_CHK that declares the ERROR flag for 10b/8b module. The two modules operate under the control of the main control block.

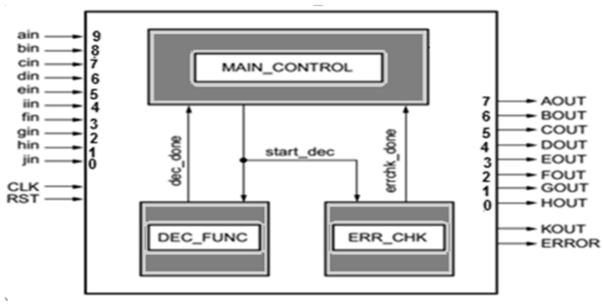


Fig.12:VHDL Model of Decoder.

The main control logic waits for frame input to ensure that the encoded data [9:0] is ready for the decoder module then, assigns the incoming data bits, to ain through jin. This block send start_dec signal to start the DEC_FUNC and ERR_CHK functions, when these modules finished, dec_done and errchk_done signals are resend to control logic at this time, it generates AOUT..KOUT outputs.

Synchronization

After the bits are successfully extracted, the receiver must search for a COMMA symbol K to determine where are the symbol boundaries. The Gigabit Ethernet transceiver equipment produce 8-bit comma character which enables the devices to word align the received data. The comma character pattern is like 00111XXX, where the X represent don’t care bits, these codes are specifically defined to enable clock synchronization. The comma pattern cannot be found in any code-group or within a concatenation of any combination of code-groups except for the code-groups /K28.5/, /K28.1/, and /K28.7/.The word alignment circuit of the transceiver is enabled and disabled by the COMMA_DETECT output signal from the encoder. The receiver scans the incoming stream of data for finding the comma characters, when it finds a comma it declares the COMMA_DETECT signal and aligns the received data (10 bits) with the rising clock edge. If the finite state machine FSM detects three successive comma characters without errors, it asserts SYNC output. The SYNC_FSM will return to search mode when four consecutive received codes are detected with code errors otherwise it remains in sync state [11].Synchronization process is accomplished by VHDL code that describe the FSM which shown in Fig.13.

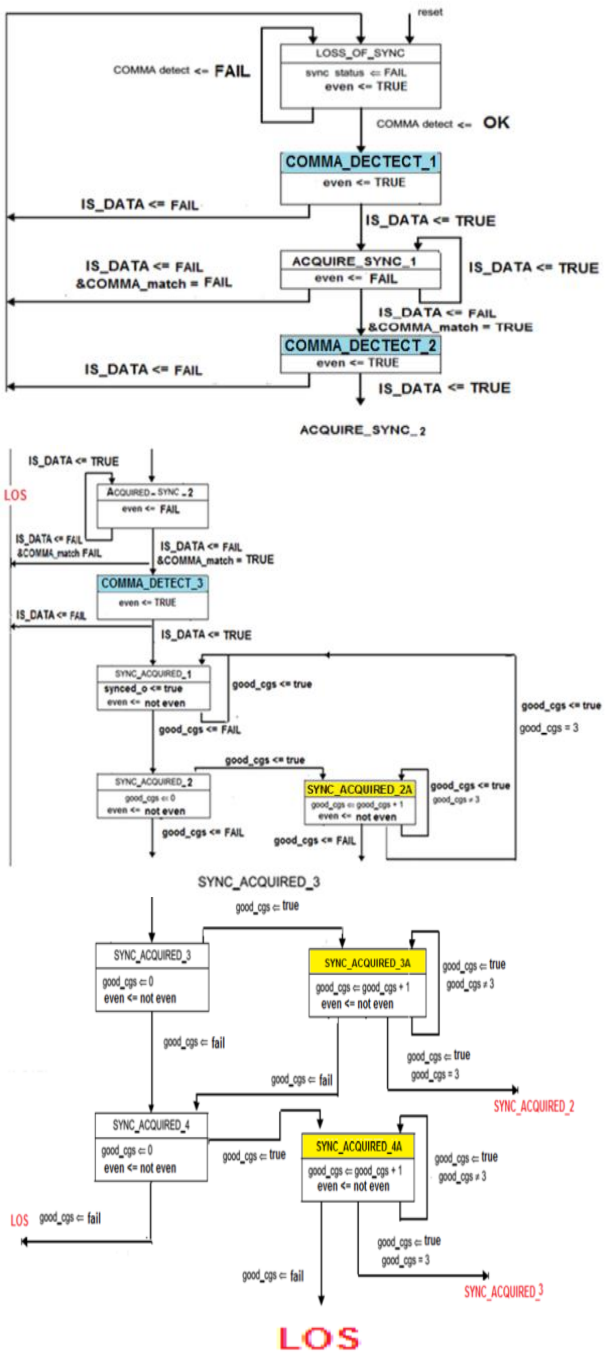


Fig.13: Synchronization Process FSM.

De-Encapsulation Process

It performs the reverse procedure of the encapsulation unit at the transmitter. Headers as well trailers are looked at the receiver and removed, to recover the data from the packets and passed on, if there are errors, discard the data or ask for retransmission.

3. Simulation Results

Simulation based method is widely used for debugging the FPGA design on computers, we simulated the code using XILINX ISE14.7 ISIM(VHDL/VERILOG) simulator. Simulation results of 1000 base-x pcs/pma core are shown in Fig. 14, and Fig. 15.

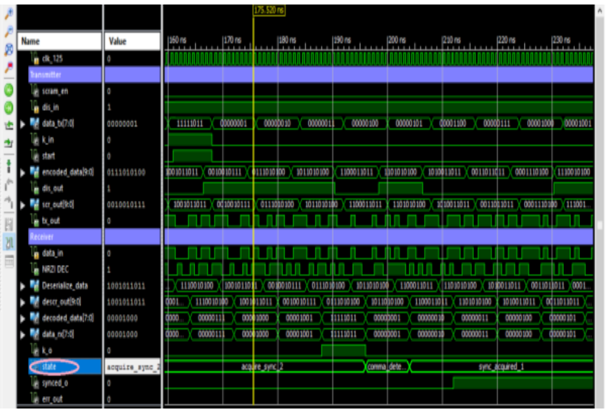


Fig.14: 1000base-X Core Simulationat Scrambler Enable (Scram_En ='0') and Input Disparity (Dis_In ='1' Or -Ve).

At Scrambler Enable (Scram_En ='1') and Input Disparity (Dis_In ='0' or +Ve), Respectively.

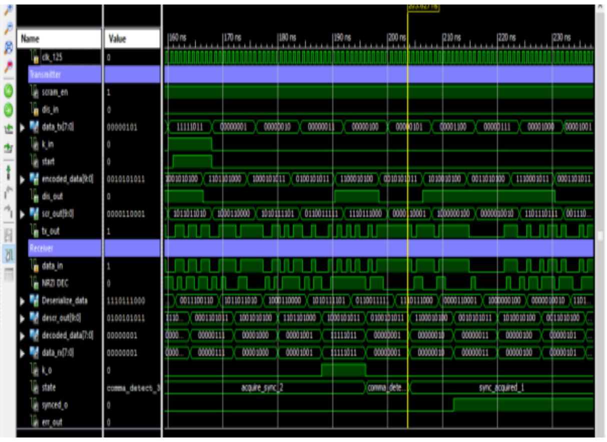
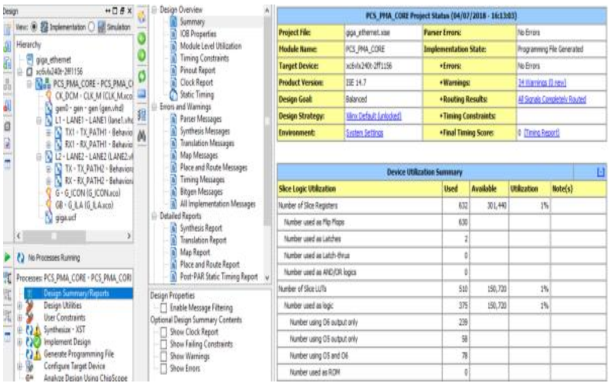


Fig.15:1000base-X Core Simulation at Scrambler Enable (Scram_En ='1') and Input Disparity (Dis_in ='0' or +ve).

Fig.14 and 15 show the simulation waveforms for the PCS and PMA. CLK_125 is the global transmitting clock. At the beginning, PCS resets the functions of transmitter and receiver. The transmitter and receiver are IDLE for a few clock periods. At the assertion of the transmitter enable signal, the PCS Transmitter sends out the control signal start /S/ before sending out the data frames corresponding to the data octet Data_tx[7:O]. On the receiver side, after the start /S/ was received, the receiver, receives the data frames. In the figures, it can be seen that, the data received (data_rx), of '01, 02, 03, etc' are the same as the transmitted data (data_tx), with no errors (err_out ='0') and achieving the synchronization (state = sync_acquired). The incoming data is encoded according to the disparity input (dis_in = 0 or 1) and are scrambled if scrambler enable is high. We notice that the exact output is determined by the RD, which is the difference between the numbers of transmitted 0s and 1s. If the current RD is (0 or 1), then the next 6b or 4b output will make RD either (0 or 1). For instance, if the input 5b data is 00001 and if RD = +ve, then the actual output signal is 100010, and RD becomes −ve because two more 0s are transmitted in this 6b word. On the other hand, if previous RD = −ve, then the output will be the complement, i.e., 011101, and RD switches to +ve. Accordingly, by this mechanism 8b/10b achieves long-term dc balance.

4. Synthesis Results of Core over Two lanes

The synthesis part was performed on Xilinx 14.7 ISE using FPGA(XC6VLX240T device, FF1156 package), and further testing was carried out using chipscope pro analyzer to verify the integrity of data. The device utilization report of 1000base-x PCS/PMA core implementation is shown in Fig.16.



PCS_PMA_CORE Project Status (04/07/2018 - 16:13:03)			
Project File:	giga_ethernet.xise	**Parser Errors:**	No Errors
Module Name:	PCS_PMA_CORE	**Implementation State:**	Programming File Generated
Target Device:	xc6vlx240t-2ff1156	**•Errors:**	No Errors
Product Version:	ISE 14.7	**•Warnings:**	34 Warnings (1 new)
Design Goal:	Balanced	**•Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	**•Timing Constraints:**	
Environment:	System Settings	**•Final Timing Score:**	0 (Timing Report)

Device Utilization Summary				
Slice Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Registers	632	301,440	1%	
Number used as Flip Flops	630			
Number used as Latches	2			
Number used as Latch-thrus	0			
Number used as AND/OR logics	0			
Number of Slice LUTs	510	150,720	1%	
Number used as logic	375	150,720	1%	
Number using O6 output only	239			
Number using O5 output only	58			
Number using O5 and O6	78			
Number used as ROM	0			

Fig.16: 1000base-X Core Design Summary.

The register transfer logic RTL schematic for the core over two lanes is depicted in Fig.17.

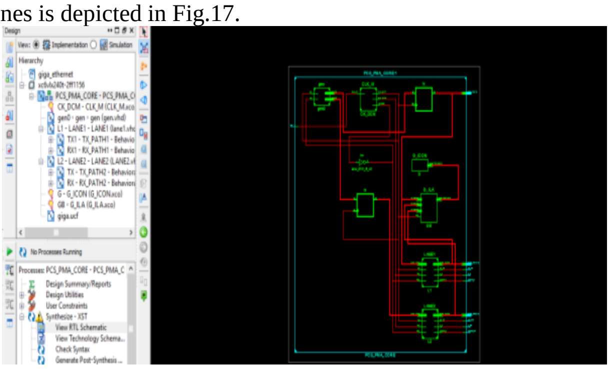
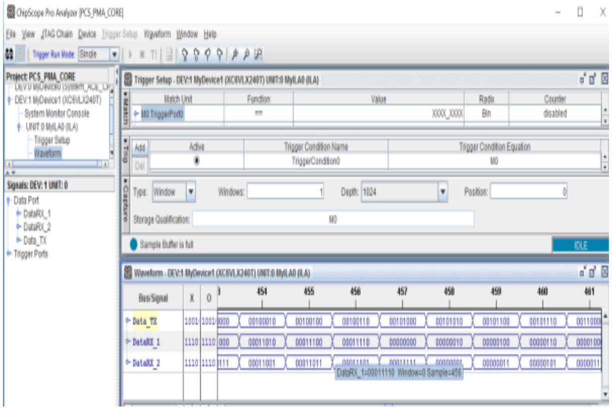


Fig.17:RTL Schematic of the Core over Two Lanes.

In the RTL view, we can see clearly the inputs and outputs of each block and also their interconnections. The chip FPGA verification has been done by using the chipscope pro analyzer Xilinx tool to verify that the transceiver works successfully such that the received data is the same as the transmitted data which is demonstrated in in Fig.18.



Trigger Setup - DEV:1 MyDevice1 (XC6VLX240T) UNIT:0 MyILA0 (ILA)

Match Unit	Function	Value	Radix	Counter
M0:TriggerPort0	==	XXXX_XXXX	Bin	disabled

Active	Trigger Condition Name	Trigger Condition Equation
●	TriggerCondition0	M0

Type: Window Windows: 1 Depth: 1024 Position: 0

Storage Qualification: M0

Sample Buffer is full IDLE

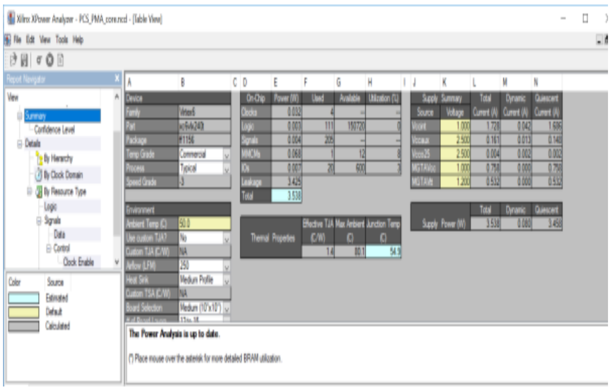
Waveform - DEV:1 MyDevice1 (XC6VLX240T) UNIT:0 MyILA0 (ILA)

Bus/Signal	X	0	454	455	456	457	458	459	460	461
Data_TX	1001	1001	00100010	00100100	00100110	00101000	00101010	00101100	00101110	0011000
DataRX_1	1110	1110	00011010	00011100	00011110	00000000	00000010	00000100	00000110	0000100
DataRX_2	1110	1110	00011001	00011011	00011101	00011111	00000001	00000011	00000101	0000011

DataRX_1=00011110 Window=0 Sample=456

Fig.18: Analyzed Results on Chipscope.

In this work, the timing and power analysis are also done; the power is obtained by Xpower Analyzer of Xilinx 14.7. The dynamic Power consumption of the designed transceiver is about 0.080 Watt from 2.5v supply as depicted in Fig.19.From the timing analysis,the delay of designed core from synthesis report of our design, is found to be 15.090 ns. Compared to [12], and [13], the proposed design shows improvement in the power consumption and the delay time. So it could be evaluated that, the proposed design has high speed and acceptable power consumption.



Xilinx XPower Analyzer - PCS_PMA_core.ncd - [Table View]

Device	
Family	Virtex6
Part	xc6vlx240t
Package	ff1156
Temp Grade	Commercial
Process	Typical
Speed Grade	-3

On-Chip	Power (W)	Used	Available	Utilization (%)
Clocks	0.032	4	---	---
Logic	0.003	111	150720	0
Signals	0.004	205	---	---
MMCMs	0.068	1	12	8
IOs	0.007	20	600	3
Leakage	3.425			
Total	3.538			

Supply Source	Summary Voltage	Total Current (A)	Dynamic Current (A)	Quiescent Current (A)
Vccint	1.000	1.728	0.042	1.686
Vccaux	2.500	0.161	0.013	0.148
Vcco25	2.500	0.004	0.002	0.002
MGTAVcc	1.000	0.758	0.000	0.758
MGTAVtt	1.200	0.532	0.000	0.532

Environment	
Ambient Temp (C)	50.0
Use custom TJA?	No
Custom TJA (C/W)	NA
Airflow (LFM)	250
Heat Sink	Medium Profile
Custom TSA (C/W)	NA
Board Selection	Medium (10"x10")

Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
	1.4	80.1	54.9

	Total	Dynamic	Quiescent
Supply Power (W)	3.538	0.080	3.458

The Power Analysis is up to date.

(*) Place mouse over the asterisk for more detailed BRAM utilization.

Fig.19: Power Analysis of PCS_PMA_CORE.

In [12], the author's presented1000BASE-T receiver simulated performance with different analog frontend designs. The power consumption is roughly 40 mW for 0.5 µm CMOS process and 98 mW for 0.18 µm CMOS process.In [13], an attempt was made to optimize the design for low power SerDes for wideband communication such as Ethernet applications. The architecture of the IC can be properly defined by the schematic design by using the cadence schematic editor. Fig.20, gives a comparison between the performance of designed transceiver and other designs in the literature [12] and [13]. We see that our design performance parameters are quite good with moderate power consumption and smaller delay.

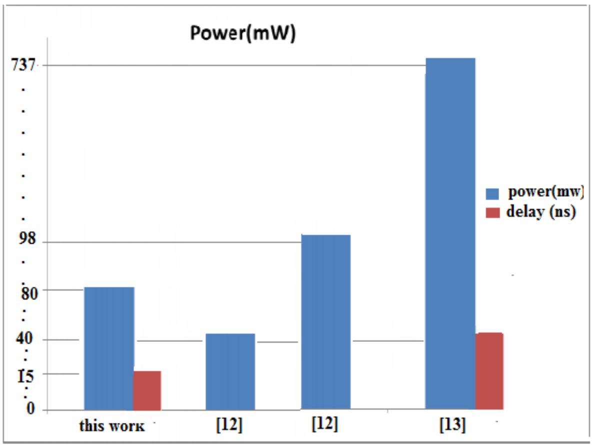


Fig.20: Comparison Study for Power and Delay Analysis.

5. Conclusion

Digital transmission is considered the main part of the digital communication networks. Local area networks reciprocate their information on digital carriers (Ethernet). This paper introduces the FPGA implementation of 1000BASE-X transceiver for gigabit Ethernet. The complete implementation of the transceiver is achieved by using VHDL code for all of the building blocks. All the parts of the transceiver are implemented and verified. Finally both the transmitted and received data are verified by using chipscope analyzer software. The timing and the power analysis are also assessed. The paper showed how a high speed device can be implemented on a lower speed FPGA and therefore open the way for software high speed interfaces.

Acronyms and abbreviations

FPGA	Field Programmable Gate Array
FSM	Finite State Machine
GE	Gigabit Ethernet
GMII	Gigabit Full Media Independent Interface
LFSR	Linear Feedback Shift Register
MAC	Media Access Controller Layer

NRZI	None Return To Zero Inverter
PHY	Ethernet Physical Layer
PCS	Physical Coding Sub layer
PMA	Physical Medium Attachment
PMD	Physical Medium Dependent Sub layer
PISO	Parallel Input Serial Output Shift Register
RD	Running Disparity
SERDES	Serializer/ De-Serializer
TBI	Ten Bit Interface
UTP	Unshielded Twisted Pairs Cable
VHDL	VHSIC Very High Speed Integrated Circuit Hardware Description Language

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