

# A genetic algorithm approach for global routing of VLSI circuits

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## Abstract

Very Large Scale Integrating (VLSI) design has the objectives of producing the layout for integrating circuits. The currently prevalent submicron regions require innovative, new physical design algorithms. Performance requirements have not seen before, become the significant features of such regions. The last ten years have been witnessing the feature of swelling success of Genetic Algorithms in their application to VLSI physical design. These algorithms are in spot light and the subject matter of study and examination. Routing problem is posed to a cost function which takes care of the total net length, the channel capacity exceedance and crosstalk. The Genetic algorithm is used for optimizing the cost function.

**Keywords:** Very Large Scale Integrating (VLSI), Genetic Algorithm (GA), routing, Macro cell, placer, graph edges.

## 1. Introduction

Currently, many millions of devices are contained in a Very Large Scale Integrated (VLSI) circuit. An important feature of the circuits is their complexity which has led to the imperative need for using Computer Aided Design (CAD) for their design.

VLSI CAD tools have the objective of transforming a high level system definition into a bunch of geometric for use in fabrication ensuring minimum size for IC.

This involves different stages of which physical design is an important phase. Physical design involves the transformation of structural design into mask geometry for the purpose of fabrication without any deviation from the basic design rules relating to the technology of choice. The different steps involved in the process of physical design are partitioning, floor planning, placement, routing and compaction. Each stage be optimizing while making the problem manageable for the subsequent stages.

System partitioning is the work of dividing a micro electronics system into individual ASIC's (Application Scientific IC's). Estimation of the sizes is a process involved in floor planning. The initial relative locations of the blocks are put in place in ASIC. Simultaneously space allocation for clock and power wiring decide on the location of the Input/ Output and power pads. The location of the logic cells within the flexible blocks is decided by placement and sets aside space considered necessary for the interconnect to each logic cell. Floor planning and placement are known for their close association. Sometimes they are constructed in a single CAD tool. Connection between the logic cells is accomplished by routing.

The goal of physical design is to produce a fully placed and routed chip which meets all delay, matching and other requirements in a small area as possible. A feature with physical design is extremely complex process. There have been developments in design styles over the several years, with the objective of reducing the complexity in the design process. These styles falls into two categories: viz., (i) Full custom and (ii) Semi custom layout styles.

Factors that influenced the type of chip, cost and the time involved in marketing are considering while making achieve of the layout.

### 1.1. Routing

The input to the routing phase is a placed circuit. Making the interconnections on the basis of a specified net list is the goal of routing. Routing is usually done in two ways, viz., two phase routing and area routing.

In area routing, the routing process is carried out in one phase. Nets are routed sequentially using algorithms like maze running and line search algorithms. Chronological factor feature the nets, where more constraints confront the nets routed later compared to those preliminary routed. This goes by the name "net-ordering problem". Rip up and re-route methods can help solving this problem which however is expensive.

In digital designs, routing often goes through two phase difference, viz., global routing and detailed routing. The former involves decomposition of an integrated circuit by inter connection network into network segments which get assigned to regions or channels.

This means the determination of an approximate path connecting the nets. It is a process on a higher level where it is defined as the routing of the nets is done the available routing regions. The results of global routing lead to a detailed router which turns out the actual geometries that connectivity requires.

As a general rule, a study of the Global Routing Problem (GRP) is made viewing it as a graph problem. The relative layout helps defining a routing graph, while the nets are routed on the graph. A Steiner tree problem in the networks is the best method for the search of route on the graph, Steiner tree problem generally recognized as a graph Steiner tree problem. However determination of a Steiner minimum tree is a NP- complete problem, explaining the reason for the large number of heuristics for practical applications.

In the concurrent approach, the formulation of GRP is done as a problem in optimization with a set of constraints. Genetic Algorithms (GA's) constitute an effective set of global search optimization methods that have demonstrated the ability to

produce palpable results on a wide range of problems. There has been a spurt in the application of GA's to general constrained optimizations in recent years.

## 2. Related works

In James cohoon et al, has forwarded a proposal which is Electronic Design Automation (EDA), which relates to the design and production of VLSI systems. Physical design is known to be a significant step in the creation of a VLSI circuit. Logical representation of the system under design forms the input to the physical design. The physical package lay out enables the optimal or near optimal realization of logical representation in the output. The problems in physical design including routing are usually combinatorial in nature with sizes of large problems.

The Field-Programmable Gate Arrays (FPGAs) routing nets problems are interconnected by a switch matrix and System-on-Chip (SOC) has reconfigurable arrays deals with Abdel et al, Finding a routing solution requires an improvement phase of an algorithm based on canonical formulation of the problem. This indicates the highly minimal feature of the routing algorithm in terms of the extent of work seen in the expansion to reach the solution. Improvement to this routing problem is possible, if the use is towards routing net; via- an extremely large switch matrix as an interconnect structure. So to overcome this limitation, a Genetic Algorithm can be used where the search area for the solution is quite large.

In the work [3], two new genetic algorithm based global routing algorithms using the concurrent approach for device level placement have been developed to solve the GRP. The GA is used to optimize the cost function formulated, which includes the overall length and a penalty function for the capacity exceedance of the channels. The router uses GA to construct the Steiner tree itself while optimizing the cost function. The channel congestion problem is taken care by the re-routing phase. Since cross talk is also a critical parameters in routing, In the present work the cost function which includes the overall length, the channel capacity exceedance and the cross talk is formulated. The function is optimized using the Genetic algorithm techniques.

## 3. Objective

The objective of this project is to implement a concurrent global router that is used to find paths for a set of multi-terminal nets within this routing space, such a router can also used for floor planning. One commonly used objective functions in global routing is reduction of total wire length to be minimum, thus minimizing the area, the other functions typically used are minimizing the longest length route, optimizing delays, cross talk etc. The objective function used in the present work is optimizing the cost function which takes care of the total wire length while meeting the channel capacity exceedance and crosstalk involved.

## 4. Methodology

1. To implement the Genetic algorithm based global router a program using object orientated has to be developed.
2. A placer which takes the Spice or Verilog net list and gives a placement has to be downloaded and worked with. The output of the placer is the input to the router to be developed.
3. A wire length estimation cost function that can explain wire length variations among nets, the channel capacity constraints as well as cross talk will be optimized using the Genetic algorithm.
4. The router will route a few benchmark circuits available.

## 5. Genetic algorithms

Genetic Algorithms (GA's) are optimizing algorithms and computerized search which work on the basis of the mechanics of natural genetics and natural selection.

Two processes are formed in the area by the Genetic Algorithms they are (i) Inheritance or the making over of features from first generation to the next and rivalry or survival of the fittest, wherein the worst features are eliminated from the individuals in the population.

Genetic Algorithms have the following advantages

1. They are adaptive with avidity to learn from experience, being its own or vicarious
2. They possess intrinsic parallelization
3. They are easy to parallelize even or a loosely coupled networks of workstations with much communication overhead.

Genetic Algorithms have their own features which makes them out from other optimization algorithms. The points of difference are:

1. Genetic Algorithms works on the basis of coding the parameter set and not parameters themselves.
2. The Genetic Algorithms search was done from a population of points, not on single point.
3. The Genetic Algorithms does not require computation of derivatives, which are required in gradient based algorithms.
4. Genetic Algorithms uses the probabilistic rule but not deterministic rules

### 5.1. Outline of the genetic algorithm

In the genetic algorithm initially, the current population of size M contains M-1 randomly generated individuals and a single individual consisting of the shortest route found for each net. The fitness of each given individuals is computed by routine evaluation. Fitness is rank-based, following a lexicographical sorting of the individuals using area as the primary criterion and wire length as the secondary criterion. Routine best of keeps closely follows the best individual ever found. Routine stop Criteria terminates the simulation when no further development has been noticed for consecutive S generations. A set of offspring formation of sizing M triggers each generation. Using standard one-point crossover, two offspring c1 and c2 are generated from parent's p1 and p2. Routine reduce returns the M fittest of the given individuals, and standard point wise mutation and standard inversion are then performed on each offspring. Routine optimize does simple hill climbing through execution of mutations sequence on the best individual, each of which improves the fitness.

generate initial Population;

evaluate (population);

best Individual = best Of (Population);

**while not stop Criteria() Do**

New Population = 0;

**For j=1 to M/2 Do**

select p1 and p2 from Population;

crossover (p1,p2,c1,c2);

Add c1 and c2 to New Population;

evaluate (PopulationU NewPopulation);

Population = reduce (Population U NewPopulation);

**For j=1 to M Do**

mutate (Population[j],Pm);

invert (Population[j],Pi);

evaluate (Population);

bestIndividual = bestOf (Population U bestIndividual);

optimize (bestIndividual);

solution = bestIndividual;

## 6. Problem specifications and formulation

Global routing involves the decomposition of an integrated circuit interconnection network into a number of segments followed by consignment of such networks to the channels or regions. i.e., it determines an approximate path which inter connects the nets. It is a process at a high level wherein definition of the routing of the nets is done over the available routing regions. The detail router is the destination for the global routing results. The actual geometries needed for connectivity are the products of the detailed router.

### 6.1. Problem specification

The input to the global router is a placed circuit. Routing space information is extracted from the placement. The global router finds paths for a set of multi-terminal nets within this routing space. An objective function commonly used in global routing is minimization of total wire length, thus minimizing an area. The other objective functions typically used are minimizing the length of the longest route, optimizing delays, crosstalk etc. the objective function used in the present work is optimization of total wire length without any channel capacity exceedance.

### Graph models for global routing

Global routing is usually investigated as a graph problem. A graph is built to reflect the routing space in the placement. The grid graphs are widely used in many routers, since they are simple, straightforward and best suited for the gate array design or sea-of-gates style. Nevertheless they are not suitable for global routing of macro-cell.

To model the macro-cell design style accurately, the floor plan are used to obtain the routing graphs directly. The cells are treated as obstacles and the routing problem is expressed regarding a weighted routing graph that exhibits the available routing area. Each routing region edge is earmarked a weight identical to the width or capacity. The pins of the nets are then mapped on to the graph. The global router task is to connect the pins of the nets without violating any capacity constraints. The frequently used graph models are the channel intersection graph and the channel free graph.

### Channel intersection graph

The channel intersection graph is used when the location of the pins on each cell are know. Each edge represents a channel (the empty rectangular space between adjacent modules) and each vertex is being similar to the intersection of two perpendicular channels. Each pin of the cell is mapped to the edge representing the nearest channel. The weights of the edges of the channel intersection graph reflect the channel width or the congestion. The channel intersection graph was illustrated in the Figure 1 and a routing tree that connects the terminals of a net.

### Channel free graph

The channel free graph model is used when the pin locations are not fixed. The pins are then assumed to be at the center of each cell. A graph is constructed with an edge between every two adjacent cells and the vertices located at the centers of each cell as shown are Figure 2. The edge lengths are based on the Manhattan distance or Euclidean distance between the centers. The capacity of an edge determines how many wires can run across the corresponding common segment between the two rectangles. It also accounts for the desired minimum spacing between the wires crossing the segment. With the channel free graph model, a global router can be used to determine the location of the pins. If some of the cells are fixed (pin locations are known) and others variable,

then a combination of both the channel intersection graph and the channel free graph can be used to model the routing graph.

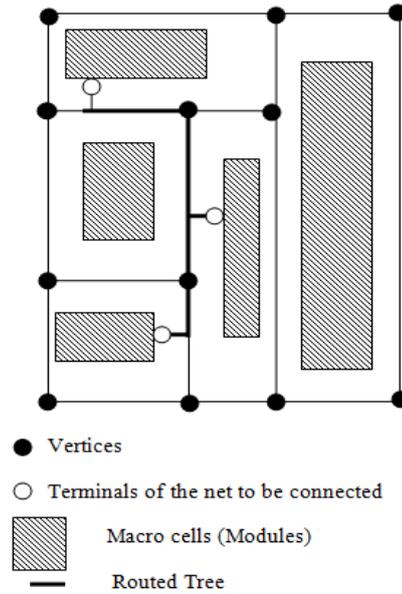


Figure. 1: The channel intersection graph

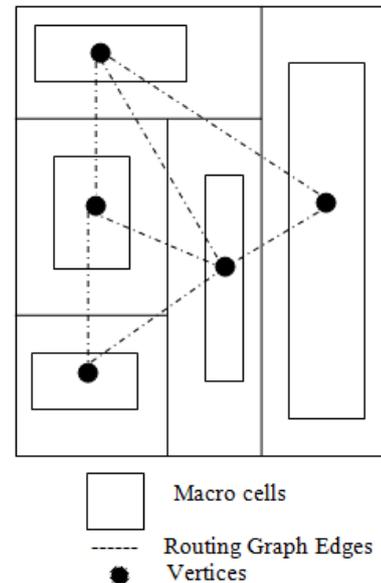


Figure. 2: The channel free graph

## 6.2. Problem Formulation

In the present global router, the cost function is formulated as follows.

$$\text{Cost} = \sum_{k=1}^n L_k + P \sum_{p=1}^m (\text{Occp} - C_p)$$

Where L is the no. of nets

m is the no. of exceeded edge

P is the penalty for exceedance of the channel

Occp is the occupancy of the edge p.

Cp is the capacity associated with edge p.

### Genetic algorithm based concurrent global routing

Two algorithms (ALG1 and ALG2), using genetic algorithm for Steiner tree generation and concurrent routing are formulated and implemented in an object oriented program. The Genetic Algorithm starts with a set of routes for each net as the initial population and as the generation progress; new routes are generated using crossover and mutation operators.

## 7. Conclusion

One of the common approaches to solve the concurrent global routing of macro cell layout based on genetic algorithm is generated. The Genetic Algorithm has the ability to produce a reasonable near optimum solution for all the problems within a moderate amount of time, and well suited as the basics algorithm for a Global router. On the other hand, if a near optimum solution is sufficient either the problem is very large or a reasonable limited run time is needed, the genetic algorithm presented here is the optimal solution of the possibilities considered.

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