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Research paper

Design of Low Power UWB CMOS Low Noise Amplifier using Active Inductor for WLAN Receiver

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Abstract

This paper presents a low power Low Noise Amplifier (LNA) using 0.18µm CMOS technology for ultra wide band (UWB) applications. g_m boosting common gate (CG) LNA is designed to improve the noise performance. For the reduction of on chip area, active inductor is employed at the input side of the designed LNA for input impedance matching. The proposed UWB LNA is designed using Advanced Design System (ADS) at UWB frequency of 3.1-10.6 GHz. Simulation results show that the gain of 10.74± 0.01 dB, noise figure is 4.855 dB, input return loss <-13 dB and 12.5 mW power consumption.

Keywords: *LNA , Common Gate, Ultra Wideband And Active Inductor.*

1. Introduction

The development of Wireless communication technology has increased the number of wireless applications. The growing demand for high data transfer rate wireless communication systems has attracted greatest interest to ultra-wideband (UWB) transceivers in industry. UWB wireless technology transmitted huge amount of data over a wide frequency spectrum for short distance low power applications. Due to the development of CMOS technology, UWB transceiver has attracted a lot of attention in system-on-chip applications [1,2]. LNA is the most critical block in an UWB receiver. Moreover, nearby radios cause increased adjacent blockers, creating severe cross modulation, inter- modulation, and desensitization. Therefore, achieving more linearity for a wide frequency spectrum is a design challenge for UWB transceivers. The weak RF signal received from the antenna is given to LNA which produces amplified signal with low noise. In LNA, noise figure plays a vital role in the overall system performance. Noise figure (NF) and bandwidth are dominated in the receiver. There is a trade-off exists between gain, noise figure and bandwidth. In wireless communications, ultra wideband RFIC receivers are designed using CMOS technology. CMOS technology is growing technology used for development of Radio Frequency Integrated Circuits (RFIC) due to advantages of compatibility with silicon based system on chip, size reduction and low cost. The frequency band of Ultra Wideband technology is between 3.1 GHz and 10.6 GHz for use in the indoor wireless applications.

Many papers discussed about the design of LNAs [3-5]. To increase the performance and impedance matching of LNA, on-chip inductors are used. However, area is an important constraint for design of circuits in SOC, but on-chip inductors occupy more area. The active inductor design is the replacement of on-chip inductor since it occupies less area and increase little power consumption. Some papers were focused on the design of LNA using active inductor [5,6]. In this paper, the design of UWB LNA using active inductor is designed.

2. LNA Design

Low Noise Amplifier is one of the most significant block in wireless receiver. LNA is an amplifier which is the significant part of RF receiver to amplify the weak received signals to the desired level with minimum noise. The LNA design includes three sections which are,

1. Input matching
2. Amplifier stage
3. Output matching

The block diagram of LNA is shown in Fig.1.

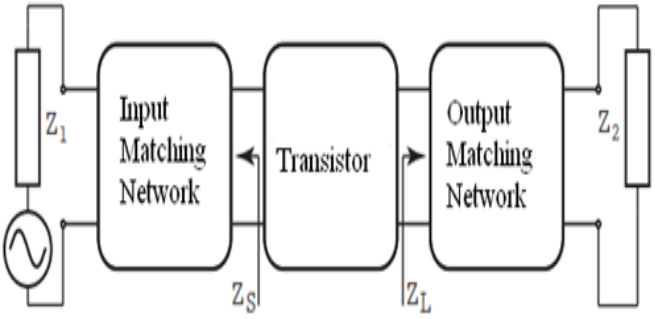

Fig. 1: Block Diagram of LNA Z_S and Z_L are the source and load impedances

2.1 Topology of LNA

The proper choice of circuit topology provides good trade-off between gain, noise figure, linearity and input impedance matching. In LNA, there are two common topologies widely used.

2.1.1 Common Source Topology

The common source (CS) amplifier is the topology in which the gate of transistor acts as an input terminal, the output is taken from drain terminal and the source is either grounded or given DC supply. The

structure of CS amplifier is shown in Fig 2. CS amplifier converts the input voltage into the current signal that is going to the load. The MOSFET's output resistance is neither high enough for a reasonable transconductance amplifier , nor low enough for a voltage amplifier. The major drawback is limited amplifier's high-frequency response. The voltage gain is boosted using transconductance feedback in CS amplifier. As the noise figure of CS amplifier has linear relationship with the operating frequency, noise figure increases when the operating frequency increased to the GHz range. CS amplifier consumes more power and degrades the linearity.

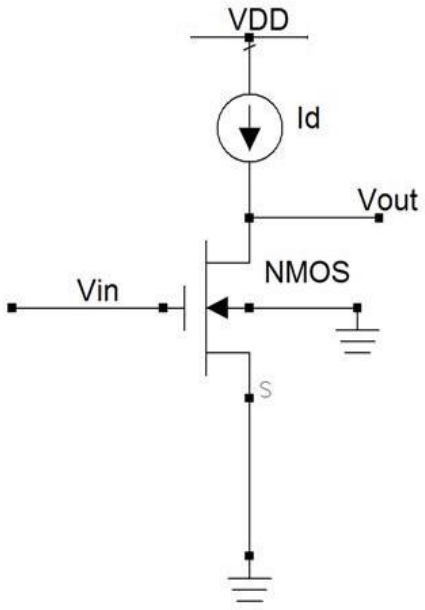

Fig. 2: Common source topology

2.1.2 Common Gate Topology

Common gate LNA (CGLNA) is a mostly used topology for wireless applications. CGLNA topology is very attractive for the UWB LNA design due to its low input impedance in a wide band frequency spectrum. In the common gate amplifier, the gate terminal is either grounded or given DC supply. The source terminal acts as the input while the drain terminal is the output. The CGLNA has minimum noise figure (NF) of 3 dB which is the drawback of this topology. CG topology gives excellent wideband impedance matching. The CGLNA has constant wideband input impedance matching, with no additional requirements, so that CGLNA saves area and avoids more on chip inductor's resistance losses. To provide a simple input matching network for wide bandwidth, a band pass filter is used in the CG-LNA to give better linearity, stability performance, low power consumption and better input–output isolation. CG-LNA is insensitive to PVT variations..The matching network plays an important role in providing proper input impedance matching. For input impedance matching, the bias current, overdrive voltage and aspect ratio are adjusted so that 1/gm is very close to Z0 (termination impedance).

The single transistor CG stage has achieved an adequate reverse isolation since there is no Miller effect. Current buffer or voltage amplifier are the applications of CG LNA.

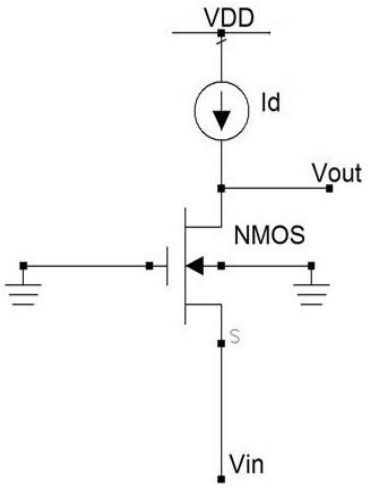

Fig. 3: Common gate topology

3. Design Methodology

Usually, the CMOS UWB LNAs use common-source(CS) and common-gate (CG) topologies to improve noise performance and input impedance matching network characteristics. In CS LNA, high Q_{match} is the main limitation for UWB matching .However, different input impedance matching techniques such as the resistive termination, inductive source degeneration, and current-reuse approach and shunt-series feedback are available for improving the input matching condition. In CG LNA, due to the advantage of parallel resonant network and the low Q_{match} , CG LNA provide better wideband behavior. The CG-LNA has more linearity, better input–output isolation, stability performance and low power consumption. The noise figure is not dependent of the operating frequency but it depends on the process parameters, device size and the input matching resistance of $1/g_m$. By setting the device transconductance to 50 Ω, the noise performance will be limited by the input matching condition. To improve the performance of CG-LNA , various techniques such as the resistive feed through, the g_m-boosting technique, and combined structure of CG–CS amplifiers were analyzed. The active inductors are preferred for input matching to passive ones due to its reduced area, power consumption, high tunability. Based on active inductor, some CMOS LNA architectures were proposed but does not have flat gain over the operating bandwidth so that these LNAs are not suitable for UWB applications.

1. g_m Boosting Technique

A gm-boosting technique is applied to CGLNA to improve the performance of proposed LNA. As negligible gate-induced noise in CG-LNA, thermal noise of transistor and noise current of the source transistor are considered as major sources that limits the noise performance. The power dissipation is reduced by sharing bias current of g_m-boosting gain stage with the CG amplifying stage.The g_m boosting mechanism is shown below in Fig 4.

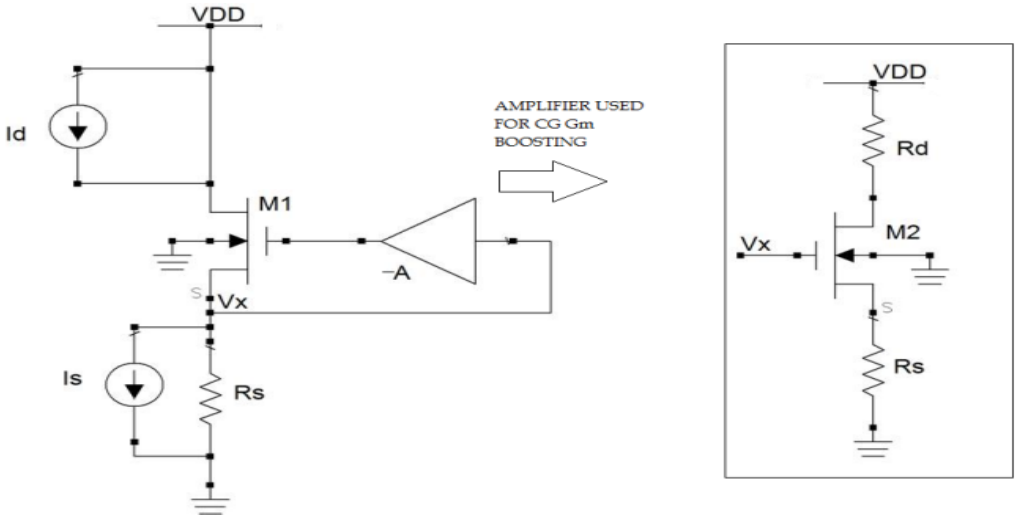

Fig. 4: CG LNA configuration with g_m boosting

2. Active Inductor

UWB LNAs use passive inductor for impedance matching and tuning purpose but it has major drawback of large silicon area. Active inductor is introduced for elimination of passive inductor. Active inductor has an important advantage of tunable frequency and consumes small silicon area. Thus the active inductors are preferred more than the passive one. Active inductor consists of CMOS transistors. Gyrator-based active inductors support large tunable self resonant frequency and more compatible with CMOS technology. The advantages of using the active inductor are low power consumption, reduce chip area, reduce complexity. The active inductor used in our proposed LNA is shown in Fig.5.

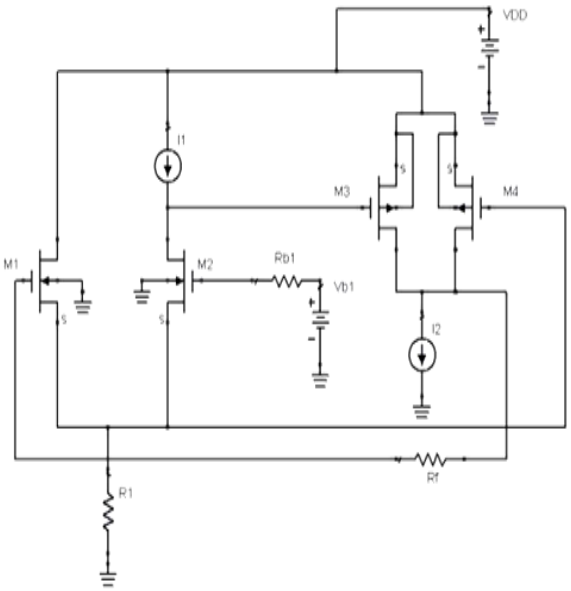

Fig. 5: Active Inductor Circuit

Two MOS transistors M1 and M2 forms the differential pair and provides positive transconductance gm1. The negative transconductance –gm2 is formed by the transistors M3 and M4. The parasitic capacitors are formed at nodes 2 and 3 by combining two gm blocks to produce an equivalent inductor. In active inductor circuit, the simple current mirror act as ideal current sources r. The noise current of M2, flows into node 2 and comes at node 3. Due to this, two fully correlated noise voltages at nodes 2 and 3 with opposite phases are created. These two voltages are again converted into current by M3 and M4. Around the resonant frequency, through proper matching of M3 and M4 AC currents, the noise contributed by M2 is cancelled at the input. While the inphase signal voltages at nodes 2 and 3 which result in constructive addition at node 1.The impedance of the active inductor can be obtained by performing small signal analysis which is given by,

Table 1: Design Parameters

Transistors [W/L] [μm/μm]	Resistors [Ω]	Capacitors [F]	Current [mA]	Voltage [V]
M1= 45/0.18	R1=50	CB1=20p	I1=0.15	VDD=1.8
M2= 45/0.18	Rf=120	CB2=20p	I2=2.04	VB1=0.7
M3= 20/0.18	RB1=5k	CB3=20p		VB2=0.7
M4= 20/0.18	RB2=9k	CB4=10p		VB3=0.9
M5=125/0.18	RD=321	COUT=10p		VB4=0.654
M6=125/0.18	RB3=12k			
M7=64 /0.18	RB4=15k			
	RL1=325			
	RL2=750			

$$Z_{in} = \frac{\frac{S}{C_1} + \frac{g_3}{C_1 C_3}}{s + sA + sB}$$

where,

$$A = \frac{g_3}{C_3} + \frac{g_1 g_3 C_2}{g_m C_1 C_3} - \omega^2 \left(\frac{C_2}{g_m}\right)$$

$$B = \left(\frac{g_{m1} g_{m2} g_{m3} + g_{m1} g_{m4} g_3}{g_m C_1 C_3}\right)\left(\frac{g_f}{g_4 + g_f}\right)$$

4. Proposed LNA

The proposed LNA, has three stages, (i) Active inductor (Input Impedance Matching), (ii) g_m boosted CG LNA stage, (iii) Gain Stage. The functions of different components of the circuit are , i) the active inductor circuit is used for input impedance matching, ii) the common gate transistor M_6 provides frequency independent noise factor and iii) cancels the miller effect which leads to good isolation to output signal, the common source transistor M_5 with resistor R_D forms the inverting transconductance with a factor of $A=g_{m5}R_D$ without increasing the bias current and transistor size.The resistors R_{B2} and R_{B3} and coupling capacitors C_{B2} and C_{B3} constitute the bias network of M_5 and M_6. The second stage is the common source transistor (M_7) gain stage to increase the power gain.UWB band width needs a flat gain over the wide frequency range. The resistor R_{L1} has been added to improve the bandwidth and provide a smooth gain. The noise sources of first stage are thermal noise of

R_D, R_{L1}, M_5 and M_6 and in second stage the thermal noises are from M_7 and R_{L2}. The design parameter values are shown in Table.1

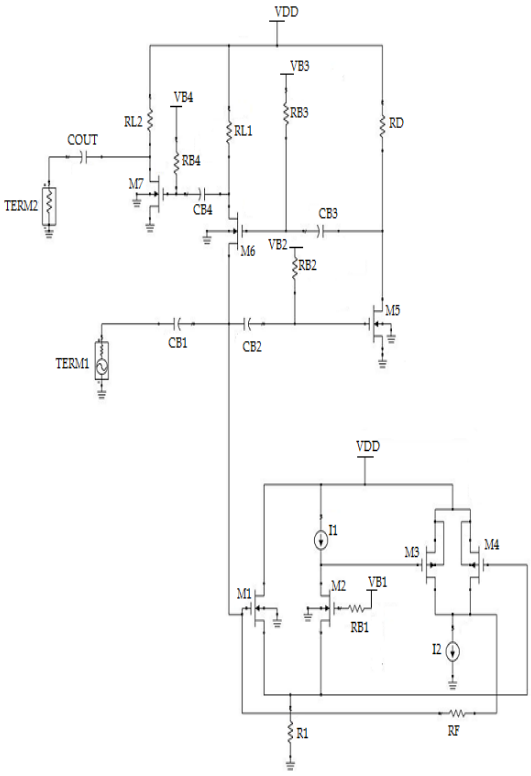

Fig. 6: Proposed g_m boosted CG LNA

5. Simulation Results

The proposed LNA is simulated using ADS software. The simulated results of gain, input return loss, noise figure and minimum noise figure are shown in Fig.7,8,9 and 10.

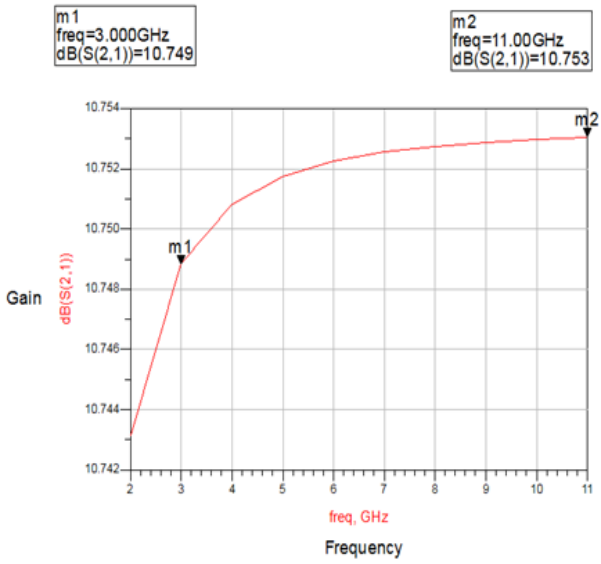

Fig. 7: Gain of proposed LNA (S_{21})

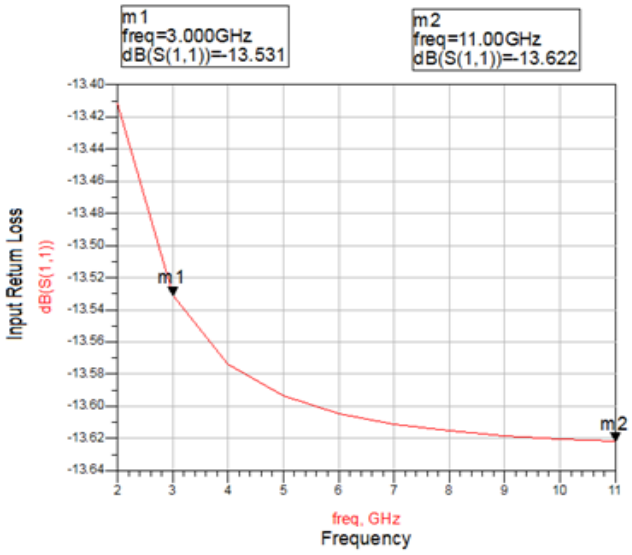

Fig. 8: Input return loss (S_{11})

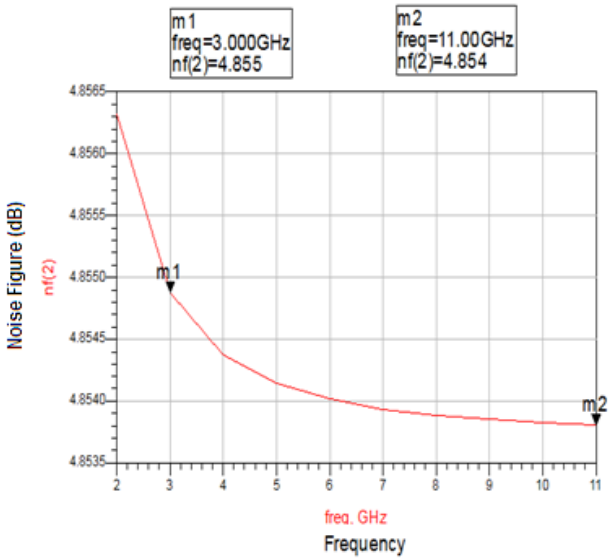

Fig. 9: Noise Figure

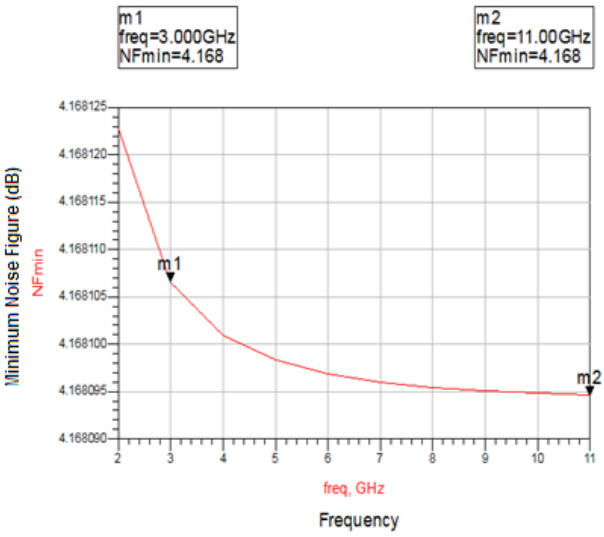

Fig. 10: Minimum noise figure (NF_{min})

From the simulated graphs we obtain the values of Gain(S_{21}) as 10.74 $\pm$ 0.01dB, Noise figure (NF) as 4.855- 4.854 dB, value of return loss is <-13 dB and minimum noise figure is 4.168 dB. The simulated graphs show that parameters such as Gain, Input return loss, noise figure are flat over the UWB frequency range of 3.1GHz to10.6 GHz. The comparison of our proposed work with previous work is shown in the table below Table 5.2

Table 2: Comparison of proposed LNA with published work

Ref	[3]	This work
Data	Simulated	Simulated
Technology	0.18µm	0.18µm
Power supply(V)	1.8	1.8
NF(dB)	4.56-4.7	4.855-4.854
S_{21}(dB)	12.1$\pm$0.7	10.74$\pm$0.01
S_{11}(dB)	< -9.5	< -13
P_{diss}(mW)	13.6	12.5

From the Table.2, the power consumption is reduced in the proposed work.

6. Conclusion

The proposed LNA has used CG structure with g_m boosting technique to improve the performance of the CG LNA and overcome its drawbacks. The use of active inductor for input matching helps to reduce area, power consumption of the circuit when compared to passive inductors. The proposed LNA shows a flat gain, over the desired frequency range. The proposed LNA has a lower power consumption when compared to its previous work. The gain of the proposed LNA is about 10.74$\pm$ 0.01 dB, noise figure is 4.855 dB, input return loss <-13 dB and power consumptiom is about 12.5 mW.

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