



# Modified Cascaded H-Bridge Multilevel Inverter using Trinary DC source

Anuja Prashant Diwan<sup>1\*</sup>, N. Booma Nagarajan<sup>2</sup>, T.Murugan<sup>3</sup>, S.Ashrafudeen<sup>4</sup>, G.J. Jenito Paul<sup>5</sup>

<sup>1</sup>Assistant Professor, <sup>2</sup>Professor, <sup>3,4,5</sup>Final year Student  
Dept. of Electrical and Electronics Engineering  
Jerusalem College of Engineering, Chennai, India  
\*Corresponding Author E-mail: adiwana\_p@yahoo.com

## Abstract

In this paper, single phase nine level cascaded multilevel inverter using trinary voltage source is described. Normally for getting nine level MLI output, four H-Bridges are required. But in proposed method, nine level output is achieved by using two H-Bridges only. Performance of Multilevel inverter is improved by using modular switching pattern. This method reduces the number of switches to the half and thus reduces switching losses. Since the number of levels at the output voltage is increased, Total Harmonic Distortion (THD) gets reduced significantly. This presents simple configuration is simple and can be controlled easily. MATLAB-SIMULINK is used to validate the results of proposed technic, simulation is carried out using. The proposed method has been exhaustively compared with classical cascaded H-Bridge topology.

**Keywords:** Total Harmonic Distortion, Cascaded Multilevel Inverter, Trinary DC Source

## 1. Introduction

For the past few years, voltage-source fed multilevel inverters have come out as a effective solution for the applications of high power dc-to-ac conversion (Rectification applications)[1]. Multilevel inverter (MLI) consists of multiple input dc levels structure and power semiconductor switches to obtain a staircase waveform. Voltage stress on each switch is less than operating voltage magnitude. [2]. The MLI has advantages like , less dv/dt stress at load, possibility of fault tolerant operation, improved THD etc. [3]. There are basic three topologies of MLI; diode-clamped MLI, flying-capacitor MLI, and cascaded H-bridge cell MLI[4]-[8]. Out of these three strategies, cascaded H-bridge has drawn maximum attention because of the advantages like, less number of Components, increased reliability as well as scalability. In MLI, the output waveform goes nearer to sinusoidal waveform, if the number of levels is increased. By inserting H-bridges, the number of levels is increased. But it has disadvantage: as the number of components gets increased, circuit become complex and cost gets increased.

To overcome these drawbacks, MLIs using cascaded transformers are studied [9]-[11]. Using cascaded transformers, galvanic isolation between source and load is achieved. However, use of transformer decreases the power conversion efficiency, also increases the weight, size and cost of the system. To overcome these drawbacks, we propose a cascaded Multilevel Inverter using H-Bridge which uses a Trinary DC input source without a transformer. Control analyses for systems [12-14]. The proposed topology is simple and easily controllable. The operation is explained in detail. Also, the paper also presents the comparison of proposed method with the classic H-Bridge cascaded MLI. Results are validated using MATLAB-SIMULNK simulation.

## 2. Trinary Multilevel Inverter Concept

In this part, the structure and the working principle of proposed topology is described in detail.

Fig. 1 shows a circuit diagram of a 9-level cascaded multilevel inverter with H-Bridge using Trinary DC source input. Circuit diagram is similar like classical cascaded H-Bridge MLI, except the input DC sources. One voltage source is Vdc and the other is 3Vdc. Using these 2 voltage sources, the required 9 levels: -4Vdc, -3 Vdc, -2 Vdc, -Vdc, 0, Vdc, 2Vdc, 3Vdc, 4Vdc are synthesised. The lower inverter is used to generate a fundamental output voltage with three levels and the upper inverter is used to add or subtract one level from the fundamental wave to generate a 9-level stepped output voltage. The algebraic addition of the individual H-bridge inverter is the resultant output voltage. Thus, the expression for output voltage can be written as,

$$V_{out} = V_{o1} + V_{o2} \quad (1)$$

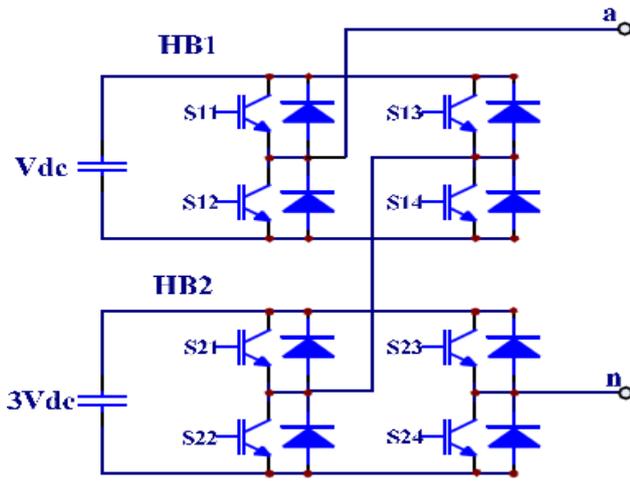


Fig. 1: MLI using Trinary DC source

In this method, n is the number of H-Bridges used. Each H-bridge is supplied by the separate DC sources with multiple of 3. And the individual voltage output of the specific level is equal to

$$V_n = 3^n, \text{ where } n=1, 2, 3, \dots \quad (2)$$

Table 1 shows the switching sequence to generate 9-level output.

Table 1: Switching sequence of 9-level output for MLI

$V_{out}$	S11	S12	S13	S14	S21	S22	S23	S24
4Vdc	1	0	0	1	1	0	0	1
3Vdc	0	1	0	1	1	0	0	1
2Vdc	0	1	1	0	1	0	0	1
Vdc	1	0	0	1	0	1	0	1
0	0	1	0	1	0	1	0	1
-Vdc	0	1	1	0	0	1	0	1
-2Vdc	1	0	0	1	0	1	1	0
-3Vdc	0	1	0	1	0	1	1	0
-4Vdc	0	1	1	0	0	1	1	0

As per the switching sequence, Fig. 2 shows the different modes of operation of the proposed topology to synthesis 9-level output voltage waveform.

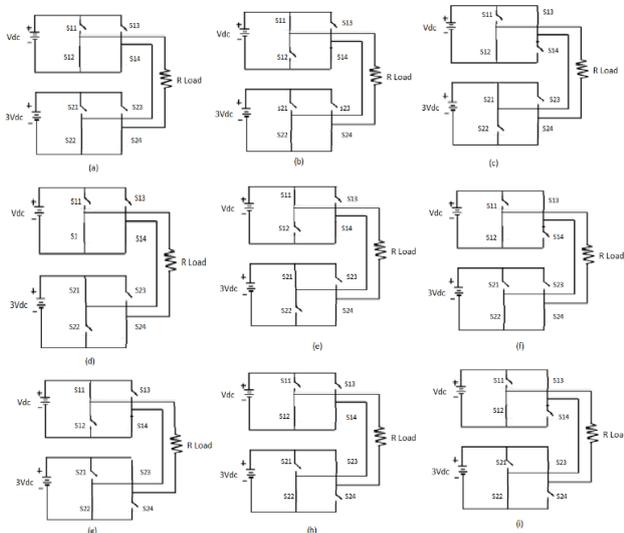


Fig. 2: Trinary DC fed MLI operation modes : (a) 0 (b) Vdc (c) 2Vdc (d) 3Vdc (e) 4 Vdc (f) -Vdc (g) -2Vdc (h) -3Vdc (i) -4Vdc

### 3. Simulation Results

Simulation study of the system is done using MATLAB-SIMULINK Fig. 3 shows the Simulink model of the 9-level Trinary MLI.

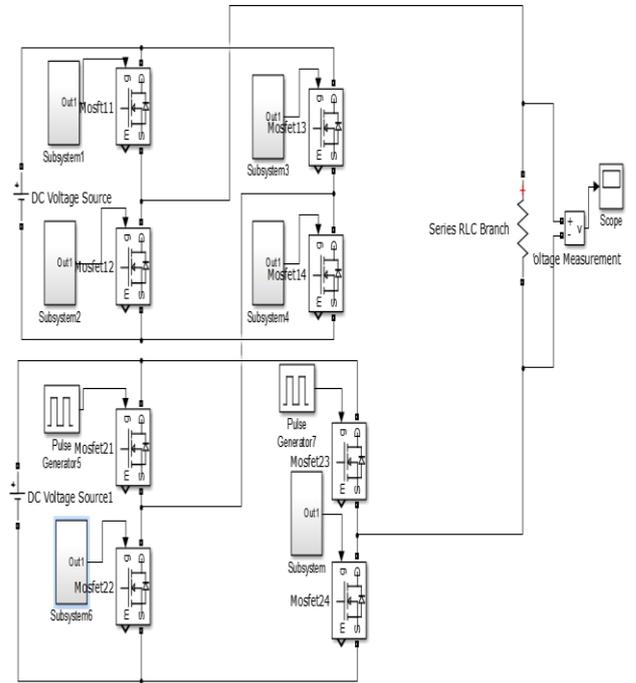


Fig. 3: Simulink model of 9-level Trinary source MLI

Considering the switching pattern, Switching pulses are generated using pulse generator:

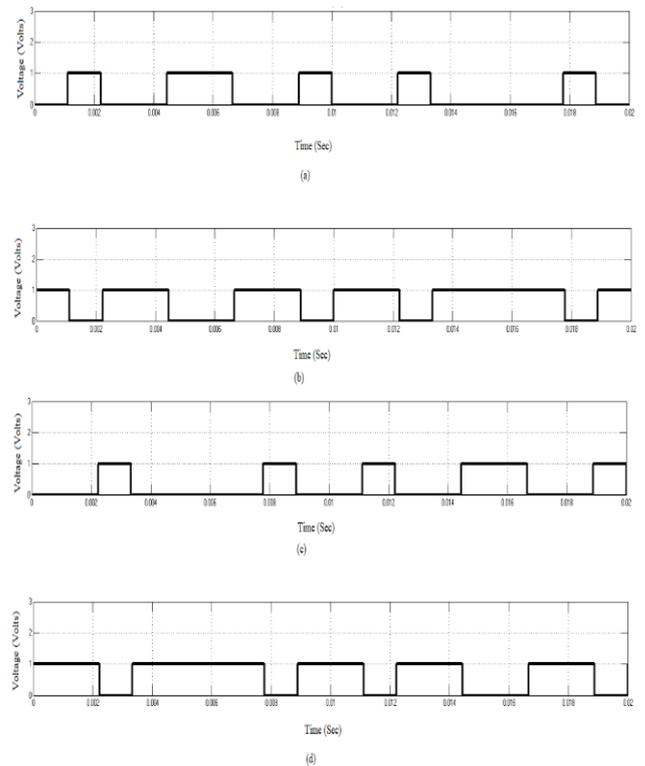
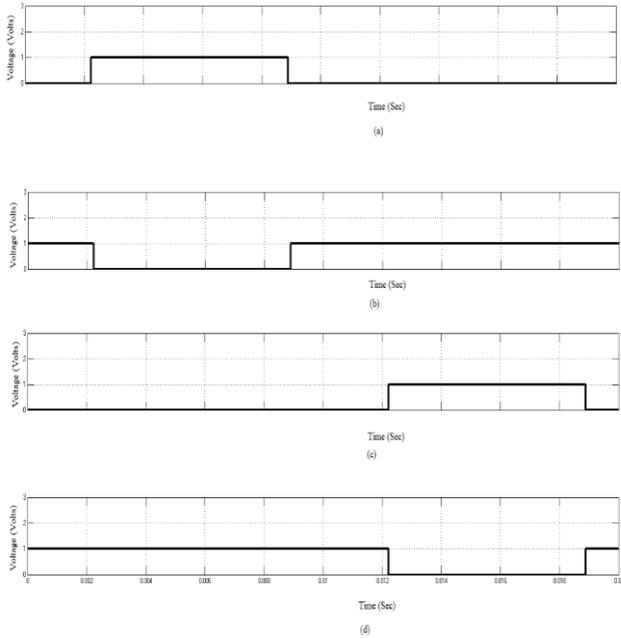


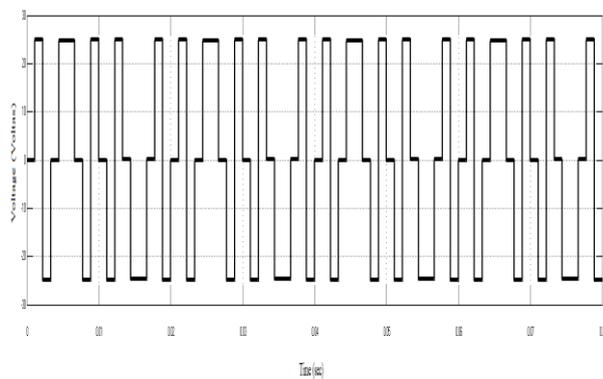
Fig. 4: switching signal for Upper Inverter (a) SW11 (b) SW12 (c) SW13 (d) SW14



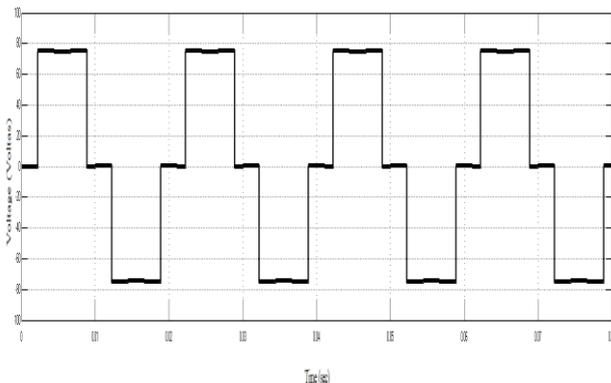
**Fig. 5:** Switching signal for Lower Inverter (a) SW11 (b) SW12 (c) SW13 (d) SW14

MATLAB – SIMULINK is used to simulate the circuit and to validate the results of proposed method. The load used for testing is purely resistive. It can be seen that the lower inverter generates three levels of output voltage and upper inverter add or subtracts one level from the fundamental voltage to generate 9-level output voltage. Fig. 9 shows the FFT analysis of nine level inverter output.

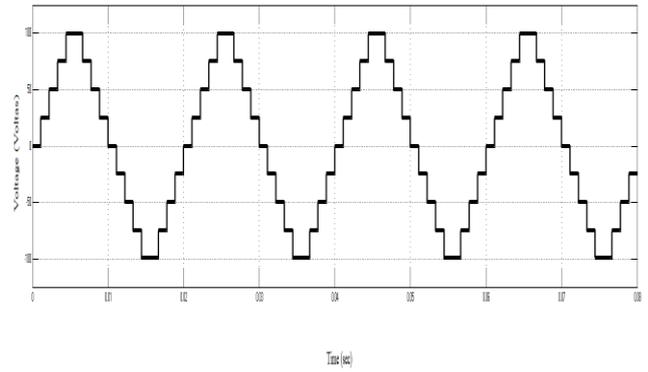
The following values are used in the simulation:  
 $V_{dc}=25V$ ,  $R$  (load) =100 ohms



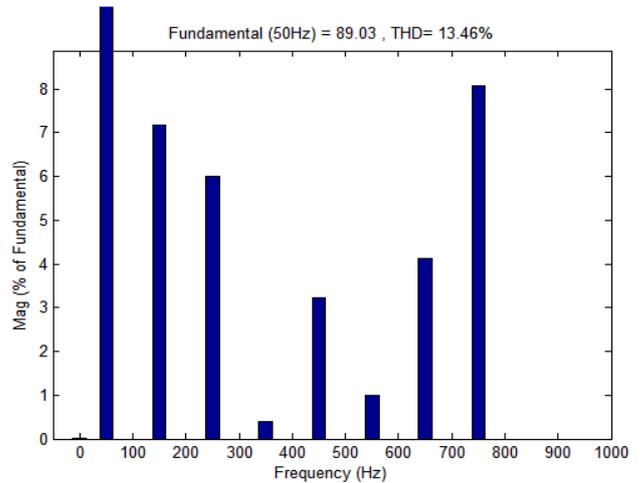
**Fig. 6:** Output of Upper Inverter



**Fig. 7:** Output of Lower Inverter



**Fig. 8:** Output Voltage of MLI



**Fig. 9:** FFT spectrum of Output Voltage

**Table 2:** Shows the comparison of the proposed method over the classical cascaded H- Bridge 9-level multilevel inverter

Parameters	Conventional cascaded MLI	Proposed Trinary DC-fed MLI
No. of H-Bridges	4	2
No. of switches used	16	9
Switching loss	More	less
Size of the system	Bulky	compact
Cost	More	less
Total Harmonic Distortion	13.41%	13.46%

From the data presented in above table, it can be observed that, using Trinary DC-fed cascaded MLI can generate good quality (almost same THD percentage) waveform with less number of components.

### 4. Conclusion

The proposed cascaded H-Bridge multilevel inverter using Trinary DC source can generate more number of output voltage levels with minimum number of devices. Thus the inverter proposed here can be used to generate output voltage waveform near to sinusoidal waveform with better quality. As the number of voltage levels are more, total Harmonic Distortion is reduced. It is observed that the proposed topology produces output voltage having 13.46% THD. As the number of switches are less, the complexity in the circuit is minimised to the large extent. Also, the switching losses are reduced and thus the overall efficiency is increased. As the 9-level output is generated by using only 2 H-Bridges, as compared to 4 as required in case of classical

cascaded MLI, overall size and the system cost is reduced to large extent. Thus it is very easy to increase the output voltage levels by adding H-Bridges in the existing unit so that THD can also be decreased to a very low value.

## References

- [1] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. Franquelo, B. Wu, J. Rodriguez, M. Perez, and J. Leon, "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553–2580, Aug. 2010.
- [2] G. Buticchi, E. Lorenzani, and G. Franceschini, "A five-level single-phase grid-connected converter for renewable distributed systems," *IEEE Trans. Ind. Electron.*, vol. 60, no. 3, pp. 906–918, Mar. 2013.
- [3] J. Rodriguez, J.-S. Lai, and F. Zheng Peng, "Multilevel inverters: A survey of topologies, controls, applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.
- [4] L. G. Franquelo, J. Rodriguez, S. Kouro, R. Portillo, and M. A. M. Prats, "The age of multilevel converter arrives," *IEEE Ind. Electron. Magazine*, pp. 28–39, 2008.
- [5] J. Rodriguez, J. S. Lai, and F. Z. Peng, "Multilevel Inverters: A survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.
- [6] J. S. Lai, and F. Z. Peng, "Multilevel Converters-A New Breed of Power Converters," *IEEE Trans. Ind. Appl.*, vol. 32, no. 3, pp. 509–517, May/June, 1996.
- [7] M. H. Rashid, *Power Electronics Handbook*, Academic Press, 2001, pp. 539–562.
- [8] L. M. Tolbert, F. Z. Peng, and T. G. Habetler, "Multilevel converters for large electric drives," *IEEE Trans. Ind. Electron.*, vol. 35, pp. 36–44, 1999.
- [9] F. S. Kang, S. J. Park, M. H. Lee, C. U. Kim, "An efficient multilevel synthesis approach and its application to a 27-level inverter," *IEEE Trans. Ind. Electron.*, vol. 52, no. 6, pp. 1600–1606, 2005.
- [10] F. S. Kang, S. J. Park, C. U. Kim, T. Ise, "Multilevel PWM inverters suitable for the use of stand-alone photovoltaic power system," *IEEE Trans. Energy Conversion*, vol. 20, no. 4, pp. 906–915, 2005.
- [11] F. S. Kang, "A modified cascade-transformer-based multilevel inverter and its efficient switching function," *Electric Power Systems Research*, vol. 79, pp. 1648–1654, 2009.
- [12] R. Kalaivani, K. Ramash Kumar, S. Jeevanathan, "Implementation of VSBSMC plus PDIC for Fundamental Positive Output Super Lift-Luo Converter," *Journal of Electrical Engineering*, Vol. 16, Edition: 4, 2016, pp. 243–258.
- [13] K. Ramash Kumar, "Implementation of Sliding Mode Controller plus Proportional Integral Controller for Negative Output Elementary Boost Converter," *Alexandria Engineering Journal (Elsevier)*, 2016, Vol. 55, No. 2, pp. 1429–1445.
- [14] P. Sivakumar, V. Rajasekaran, K. Ramash Kumar, "Investigation of Intelligent Controllers for Variable Speed PFC Buck-Boost Rectifier Fed BLDC Motor Drive," *Journal of Electrical Engineering (Romania)*, Vol. 17, No. 4, 2017, pp. 459–471.
- [15] M. Rajesh, Manikathan, "ANNOYED REALM OUTLOOK TAXONOMY USING TWIN TRANSFER LEARNING", *International Journal of Pure and Applied Mathematics*, ISSN NO: 1314-3395, Vol-116, No. 21, Oct 2017.
- [16] T. Padmapriya and V. Saminadan, "Inter-cell Load Balancing technique for multi-class traffic in MIMO-LTE-A Networks", *International Journal of Electrical, Electronics and Data Communication (IJEEDC)*, ISSN: 2320- 2084, vol. 3, no. 8, pp. 22–26, Aug 2015.