International Journal of Engineering & Technology, 7 (1.1) (2018) 660-663

International Journal of Engineering & Technology

Website: www.sciencepubco.com/index.php/IJET

Research paper

A novel design of high performance1-bit adder circuit at deep sub-micron technology

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Abstract

In this paper, the design of hybrid 1-bit full adder circuit using both pass transistor and CMOS logic was implemented. Performance parameters such as power, delay, and PDP were compared with the existing designs such as complementary pass-transistor logic, transmission gate adder. At 0.4V supply at 22nm technology, the average power consumption is 1. 525 uW was found to be extremely low with moderately low delay 90. 25 ps and PDP found to be 0.137 fJ. The present implementation has very good improvement in terms of delay, power and power delay product when compared to the existing hybrid 1-bit full adders. Also the number of transistors has been reduced to 13 where as the existiing hybrid full adder circuit has 16 transistors. The proposed circuit was implemented using mentor graphics tool in 45nm, 32nm and 22nm technologies with different supply voltages.

Keywords: *Hybrid logic; Power Consumption; Delay; Transistor Count; PDP.*

1. Introduction

The high requirement for very large and ultra large-scale implementations has been increased due to high usage of portable electronic devices like cell phones, laptops etc. leads to low power delay characteristics. Since full adders play an important role in almost all the circuits applications many researches are being made regarding this full adder [1]- [3]. Different logic styles are grouped together for the formation of Hybrid full adder circuit. The different designs which have been reported till now are divided in to following categories which are static and dynamic. Static style is found to be more reliable and simpler with less power requirement when compared with dynamic style but the area requirement on chip is more than that of dynamic style [3], [4]. Different logic styles such as dynamic CMOS logic [4], complementary metal-oxide- semiconductor (CMOS) [3], CPL [5], [6], and TGA [7], [8] are the basic logics used in the design of Hybrid 1-bit full adder circuit. Different logic styles are grouped together for the overall performance of the circuit. Strength against voltage scaling and transistor sizing are the advantages of CMOS and high capacitance at the input and using buffers [3] is the disadvantage of CMOS. Similarly, CPL has the advantage of good voltage swing and its disadvantage is that CPL is not a good application for low-power application due to the continuous changing of the intermediate nodes i.e. more switching power, there is an increase in the transistor count and input overloading is occurred. However, the disadvantage of CPL that is the voltage degradation is completely overtaken by TGA [9]- [12]. The three modules of full adder that is shown in the diagram is implemented using the above circuits using the above logics. These three modules indicate XOR, SUM, CARRY.The XOR module is designed using the transmission logic and CMOS logic. The SUM and the CARRY module is designed using Transmission logic. The main theme of this paper is to reduce values of the performance parameters like delay, power, power delay product by simulating under 45nm, 32nm, 22nm technology using mentor graphics tool. The power consumption and delay were eventually reduced in the proposed circuit i.e. 45nm, 32nm, and 22nm technologies when compared to the other CMOS full adder circuits. The average power using 45nm technology is 3.125 uW and the delay was 120.45 ps. Similarly for 32nm technology the average power was found to be 2.025 uW and delay as 110.23 ps and coming to the 22nm technology the average power was 1.525 uW and delay 90.25 ps.

2. Proposed hybrid 1-bit full adder

In the modern and high-performance applications these days there is a high requirement to match the required output. To achieve this the complexity of the circuits and the operating frequency have been improved. There is also a huge demand on the low power building blocks as the number of portable electronicdevices are increasing. Due to this there is a need for the existence of long lasting batteries. Not only battery but there is also a requirement in the increase of speed, decrease in power consumption and delay in the circuit. The major factor that is considered while designing this hybrid full adder circuit is the power-delay product. While executing any operation the power-delay product is used for calculating the energy consumed by that device. There are advantages and disadvantages while designing the proposed hybrid adder circuit using different logic functions. Numerous logic styles in a circuit supports the execution perspective of one to the detriment of other. The frequently used logic styles to design a full adder are

CMOS, CPL, TFA. The logic styles which will be using more than one logic styles are called as hybrid logic styles. To achieve the improvement in the performance of the adder features from different logic styles are mixed and will be considered in the design. The 1- bit hybrid full adder circuit is shown in the Fig. 2. The proposed design also consists of features from different logics styles. The proposed design consists of three different modules or blocks which shown in the Fig. 1. Block 1 is represented with an XNOR circuit, Block 2 is represented with a CARRY circuit, Block 3 is represented with a SUM circuit. The output through the CARRY circuit is represented with C_{out}. The output of the SUM circuit is represented with SUM.

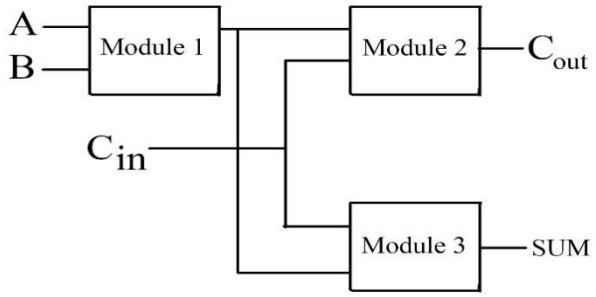

Fig. 1: Block Diagram of Full Adder.

To reduce the circuit delay, energy, transistor count the circuit has been designed in an efficient manner.

a) XNOR block (Modified)

There is a proportionately huge delay in the full adder circuit which is caused by the XNOR module. So, in this proposed design the XNOR module has been improved and the number of transistors has been reduced which is three. When compared to the normal XNOR circuit this changed XNOR circuit will be offering a high speed but with a small amount if increase in power which reduces the circuit delay. The XNOR module is shown in the Fig . 3.

b) SUM Generation module

The SUM generation block in the proposed design is same as the normal hybrid full adder design. This block consists of following PMOS transistors (MP6 and MP5) and NMOS transistors (MN6 and MN7). The SUM is implemented using the second level XNOR circuit using the PMOS an NMOS transistors. The SUM generation block is shown in Fig .4.

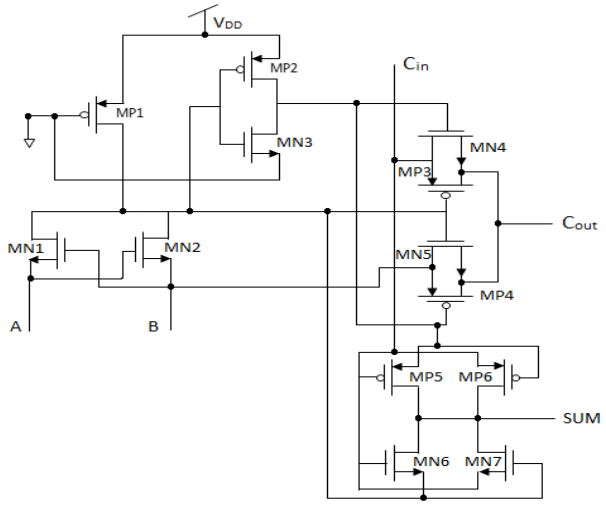

Fig. 2: Proposed Hybrid Full Adder Circuit.

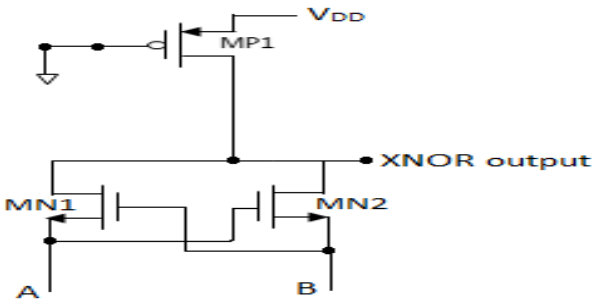

Fig. 3: XNOR Module.

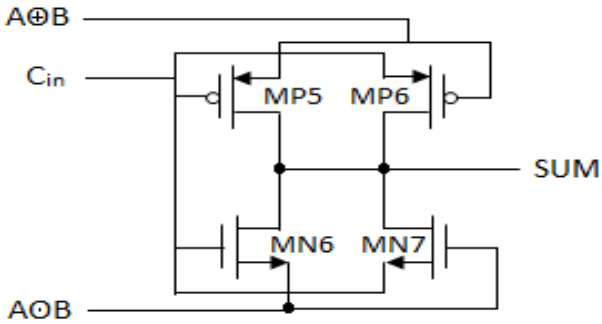

Fig. 4: SUM Generation Module.

c) CARRY Generation Block

In the proposed full adder circuit, the carry generation block is same as the design in the general hybrid full adder circuit. This block contains an inverter and a pair of transmission gates. The inverter is made up of MP2 and MN3. The transmission gates are made up of MP3 and MMN4, MP4 and MN5. The circuit delay is reduced by propagating the input signal through the single transmission gate MP3 and MN4. The usage of the transmission gates reduces the delay in the carry signal. The carry generation block is shown in the Fig. 5.

3. Operation of the proposed hybrid full adder circuit

The complete diagram for the proposed full adder is shown in the figure- 4. There are three different logics which have been used to design the proposed circuit. Those three blocks are as follows: 1. XNOR module 2. CARRY generation module 3. SUM generation module. The XNOR module is designed using four transistors which are mainly NMOS transistors. As the voltage V_{ss} is applied to the gate terminal of the transistor MP1 it is always in the ON state i.e. permanently in the ON state. To the source terminals of the transistors MN1 and MN2 the inputs A and B are connected. The three transistors namely MP1, MN1 and MN2 are used to perform the logic of the XNOR module. The input of the SUM generation module (module 3) and the CARRY generation module (module 2) is taken from the output of the XNOR module respectively. The module 2 consists of an inverter which is used as a buffer in between the input and output.

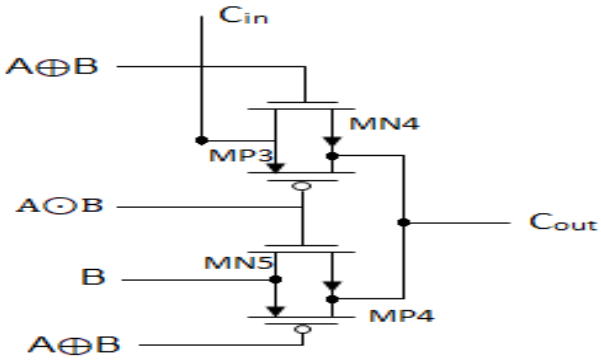

Fig. 5: CARRY Generation Module.

For the efficient operation of the block 2 and block 3 an inverter is used which helps in preventing the loading effect between those blocks. The buffered inverter is used as feed to the carry block. To minimize the propagation delay and for the fast changing in the logics the carry module is made using two transmission gates. A secondary staged XNOR module is used in the SUM block to generate the SUM output. From the table II the generation of the C_{out} is shown as follows:

Table 1: Aspect Ratios of Transistors

Transistor	45 nm W (nm)	L (nm)	32 nm W (nm)	L (nm)	22 nm W (nm)	L (nm)
MP1	120	45	80	32	55	22
MN1,MN2	90	45	64	32	45	22
MP2	120	45	80	32	55	22
MN3	90	45	64	32	45	22
MP3,MP4	120	45	80	32	55	22
MN4,MN5	90	45	64	32	45	22
MP5,MP6	120	45	80	32	55	22
MN6,MN7	90	45	64	32	45	22

If A is equal to B, then C_{out} is equal to B;
Else, C_{out} is equal to C_{in}.

The above condition states that if A is equal to B is checked by the XNOR gate then either the output C_{out} is equal to the input B or the output C_{out} is equal to the input C_{in}. These two conditions are implemented using the two transmission gates which are present in the CARRY generation block. The first condition which is C_{out}=B is implemented using the two transistors MP3 and MN4. The second condition which is C_{out}=C_{in} is implemented using the transistors MP4 and MN5. The aspect ratios of different transistors are shown in Table I.

4. Simulation results

The Recommended Hybrid Full Adder circuit of 1 -bit is implemented and simulated using the 45nm, 32nm and 22nm technologies and the results are compared with other likely full adders implemented using the same technologies. The comparison is shown in the below table II. The Key Factors like PDP (Power delay Product) is less for the circuit which is recommended in this paper and the other issues like delay and number of transistors are also minimized. The recommended Hybrid Full Adder of 1 bit is implemented using 13 transistors which is less when compared to other. The recommended Hybrid Full Adder of 1 bit is implemented using 13 transistors which is less when compared to other likely full adders implemented using same technologies. As the Propagation Delay of the implemented 1 Bit Hybrid Full Adder is Very less, The Power Delay Product of the implemented Hybrid one-bit Full Adder is also reduced as shown in the table II.

Table 2: Delay, Power, PDP Values Comparison of Proposed and Alternative Logic Styles

Design	*45nm*			*32nm*			*22nm*		
	Delay (ps)	*Power (uW)*	*PDP (fJ)*	*Delay (ps)*	*Power (uW)*	*PDP (fJ)*	*Delay (ps)*	*Power (uW)*	*PDP (fJ)*
TFA	149.236	3.5401	0.528	70.8125	5.6504	0.401	77.878	4.352	0.338
CMOS	203.66	3.242	0.660	705.41	4.559	0.3219	213.37	1.768	0.377
TGA	142.74	5.325	0.671	121.105	5.006	0.6052	102.80	3.908	0.401
Hybrid Adder	126.55	3.29	0.469	165.96	2.245	0.372	172.64	2.015	0.347
Present Work	**120.45**	**3.125**	**0.376**	**110.23**	**2.025**	**0.223**	**90.25**	**1.525**	**0.137**

Graphical representation of pdp for different full adders is shown in below Fig. 6.

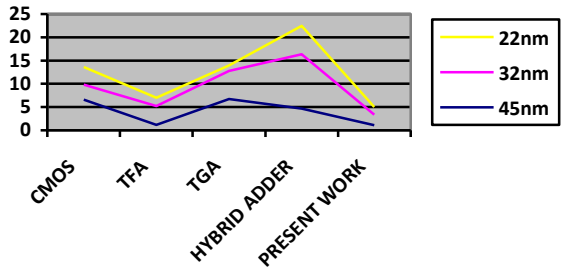

Fig. 6: Power-Delay Product Comparison of Different Full Adders.

a) Calculation of Average Power Consumption

The Calculation of Power Consumption depends on two criteria's that is static and dynamic power consumption which is defined as the average Power Consumption of the circuit. Dynamic Power Consumption is most Crucial while calculating Power Consumption and this is generated because of the continuous charging and discharging of the Capacitor. The Dynamic Power of the recommended one-bit Hybrid Full Adder is calculated and it is measured as 1.525 uW. The Major part of the power consumption of the circuit is consumed by XNOR Block, the huge Power Consumption of XNOR block is because of unavailability of inverter as an input of XNOR and the PMOS transistor is turned on completely.

b) Propagation Delay Calculation

Adder which is used as Key Block in the Implementation Of 1-Bit Full Adder systems, the entire speed of those systems Depends on the Adder Delay. The Speed of the Adder is calculated by the lengths of the Input Signals given to the circuit and in our circuit the speed depends upon the carry signal which is given as input. In the recommended 1bit Hybrid Full Adder input signal length is minimized by managing any of input signal A or B or either by managing the input carry. The delay Comparison of different full adder designs in shown in below Fig 7.

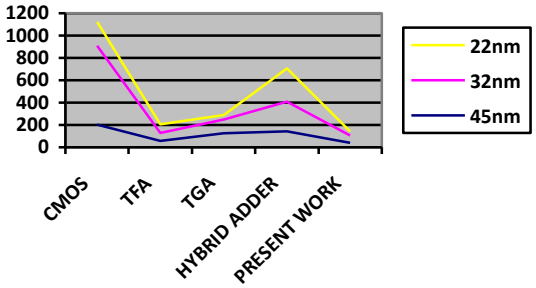

Fig. **7:** Delay Comparison of Different Full Adders.

The 1-bit hybrid full adder's simulation waveform is shown in Fig. 8.

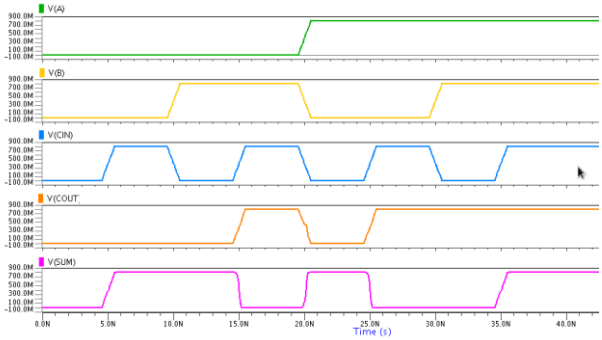

Fig. 8: Simulation Results of Proposed H Ybrid1-Bit Full Adder.

5. Conclusion

We have illustrated a new 1-bit hybrid full adder in this paper**.** The simulation was done using Mentor Graphics tool with 45nm, 32nm and 22nm technologies**.** The recommended 1-bit hybrid adder is compared with the likely full adder designs like CMOS, TGA, TFA and other existing hybrid full adder of 16 transistors**.** The Results which we get by simulating the Recommended Hybrid 1-Bit Full Adder clearly shows the decrease in the Power Delay Product by comparing with the earlier simulated results**.** In the Recommended Hybrid full adder, the number of transistors is reduced in XNOR Block, which further reduces the delay**.** Hence the Hybrid full adder which is implemented in this paper shall be used in the device applications with less power consumption and high-speed**.**

Acknowledgement

The authors would also like to thank Koneru Lakshmaiah Education Foundation, Vaddeswaram, Guntur, India for providing the necessary computing facility and tools**.**

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