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Research Paper

Neural network controller based sequential switch cascaded H-bridge multilevel inverter

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Abstract

This paper presents a novel cascaded multilevel inverter structure with reduced devices. This structure is termed as sequential switch cascaded multilevel inverter. The basic asymmetrical hybrid circuit is described and is capable of generating 17 voltage levels. The various modes of deriving 17 levels are explained and the proposed topology is compared with existing topologies in various aspects. Neural network controller can be used to generate the gating pulses. The algorithm can be trained online by using back propagation algorithm and also an algorithm to determine the number of levels, maximum voltage ratings and power loss is explained. The simulation can be done by MATLAB Simulink.

1. Introduction

The scope of multilevel inverters has received more attention because of their high power handling capacity and they can be successfully implemented in medium and high power applications. Recently multilevel inverters are popular in most of power electronic applications due to its high power handling ability, modularity, and superior harmonic characteristics. An array of power semiconductor devices and dc voltage sources are used to generate stepped voltages. Also they are capable of producing output with high quality, reduced harmonics and switching losses. Among three basic types of multilevel inverter namely diode clamped, flying capacitor (FC), cascaded H-Bridge (CHB), the CHB topology uses reduced number of power switches. And to produce high voltage levels two switching configuration are used. They are termed as symmetrical and asymmetrical configuration. In asymmetrical switching by properly introducing the dc voltage proportions successfully the number of components can be reduced with increase in output voltage level.Asymmetrical cascaded MLI with trinary dc sources produce high number of levels than binary switching. Currently researchers concentrating on developing new structures of cascaded multilevel inverter to reduce number of power components [1]-[3]. The basic symmetrical topology presented in [4] requires (2X+1) output levels for X number of H-Bridges.

The major drawback of this symmetrical structure is its increased number of components for higher levels as it uses same dc voltages for all H-Bridges. A new symmetrical multilevel inverter has been presented in [5] that use single and double source sub multilevel units. The series and parallel combinations of switches reduce the total conducting switches in each level.

An asymmetrical configuration with series/parallel conversion of sources presented in [6].This topology is implemented with multi output boost converter. The drawback is when number of level increases the variety of dc sources increases. In article [7] asymmetrical cascaded H-Bridge with different switching frequency for different H-Bridges has been presented. The capacitor voltage balancing technique is also discussed but increases the voltage stress on each conducting switch. Modular Multilevel Converter (MMC) configuration presented in [8],[9] can be easily extended to higher levels but it requires large number of switches. And also neutral point clamped (NPC) technique introduced in1981 uses series connected capacitors at the input side. The main problem is capacitor voltage balancing [10],[11].

Various algorithms in determining values of sources have been presented in [12]. A trinary based algorithm is presented in [13] that needs minimum components and also many structures were developed to reduce number of switches , driver units, dc sources , maximum voltage rating. In [14]-[16] fundamental structure have been developed but number of switches and voltage rating of switches are high. A new topology is presented in [17] and three algorithms have been explained that reduces the number of components used. But here the variety of dc sources increases. A fundamental topology based on developed H- Bridges presented in literature [18] use unidirectional switches and also an algorithm to determine voltage rating, number of sources to analyze cost of the inverter is presented. An asymmetric topology with less number of main switches has been presented with concentration on THD reduction [19],[20]. In asymmetric switching with binary hybrid multilevel inverter produces higher number of levels than symmetric type [21].

In this paper a fundamental topology of multilevel inverter structure which uses reduced number of switches, dc sources. The basic unit is capable of generating seventeen voltage levels and this structure can be extended to higher number of levels.

The Insulated Gate Bipolar junction Transistor (IGBT) with antiparallel diode combination is used as switch. This sequential switch cascaded multilevel topology is compared with existing topologies presented in literature [10]-[18] in various aspects such as maximum blocking voltage, number of dc sources and number of IGBTs. The performance of the inverter is checked with

MATLAB Simulation. Asymmetrical MLI, Interline Dynamic voltage restorer are discussed in [33-37]. Dc-dc converters using controllers [22-32].

2. Proposed Sequential Switch Cascaded Multilevel Inverter

Fig. 1 shows the basic sequential switch cascaded multilevel inverter (SSCMLI). It consists of six unidirectional switches (S_{u1} , S_{u2} , S_{u3} , S_{u4} , S_{un} , S_{um}) and two bidirectional switches (S_{b1} , S_{b1}) , four dc sources (V_{d1} , V_{d2}) connected with load. Two dc sources in same leg has same value. The insulated Gate Bipolar Junction Transistor (IGBT) with antiparallel diode is used as switch. The fundamental unit can be extended to higher number of levels by increasing the number of bidirectional switches in each leg

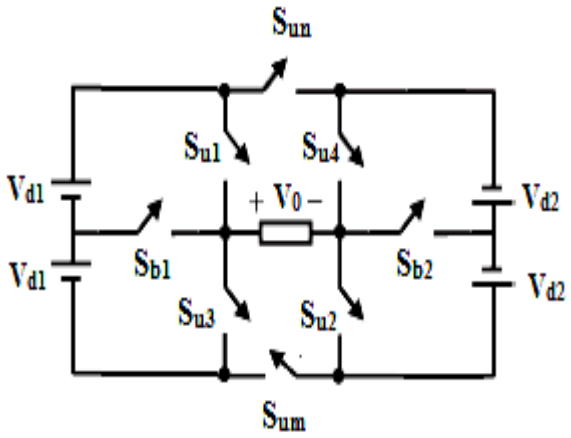

Fig. 1: Proposed basic sequential switch cascaded MLI

The basic unit is capable of generating 17 levels. The various modes of operation for generating all voltage levels is given in fig 2(a)- fig 2(q). During mode-I the conducting switches are S_{un}, S_{u1} and S_{b1}.Here the subscript 'u' represents the corresponding switch isunidirectional and 'b' represents bidirectional switch. The output voltage at the end of mode-I is $V_0= V_{d1}$. The switches S_{un}, S_{u3} and S_{b2} conducts,$V_0= V_{d2}$ during mode-II. In mode-III, the switches S_{un}, S_{un1} and S_{u2} are conducting and output voltage is $V_0=2V_{d1}$ .when the switches S_{un}, S_{u3} and S_{u4} are conducting the output voltage is $V_0=2\ V_{d2}$.During mode-V, the switches S_{un}, S_{b1} and S_{b2} are conducting, $V_0=(V_{d1}+V_{d2})$. In mode –VI, the switches S_{u1}, S_{un} and S_{b2} are turned on to give output voltage $V_0= (2V_{d1}+V_{d2})$.
During mode VII the switches S_{b1}, S_{u4} and S_{un} are conducting and voltage across load is $V_0=(V_{d1}+2\ V_{d2})$. During mode VIII the conducting IGBTs are S_{u1}, S_{u4} and $V_0= (2V_{d1}+2\ V_{d2})$. From mode-I to mode-VIII, the output levels are positive and from mode-IX to mode-XVII the output levels are negative. In order to avoid short circuit the switches in the same leg cannot be turned on at the same time. Thus the switches S_{u1} and S_{u3} should not be turned on at the same time. Similarlythe closing of switchesS_{u4} and S_{u2} at the same time should be avoided and also the simultaneous turn on S_{un} and S_{um} must be avoided. In order to get maximum levels in the output unequal dc voltages are chosen such that the dc sources in the same leg are same but different legs are different. The basic proposed unit can be connected in m number of series connected units to generate more number of levels. For example the value of series connected basic unit is taken as two it is possible to extract 81 levels in the output.

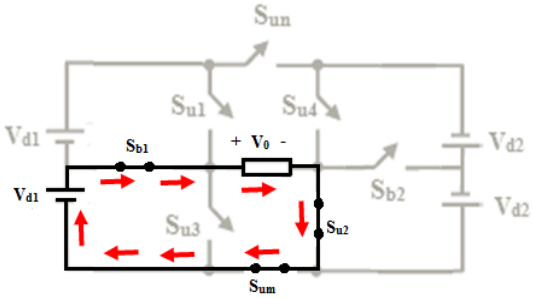

Fig. 2(a): Mode-I ($V_0= V_{d1}$)

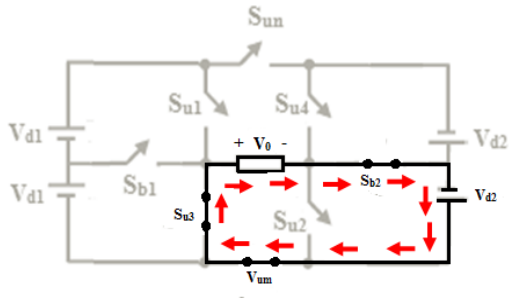

Fig. 2(b): Mode-II ($V_0= V_{d2}$)

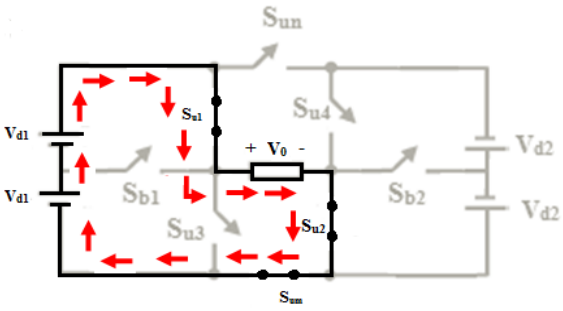

Fig. 2(c): Mode-III ($V_0=2\ V_{d1}$)

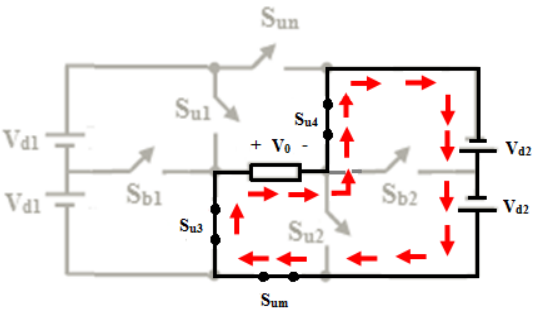

Fig. 2(d): Mode-IV ($V_0=2\ V_{d2}$)

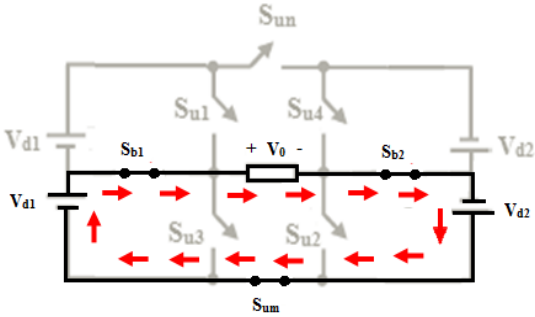

Fig. 2(e): Mode-V ($V_0=(V_{d1}+V_{d2})$)

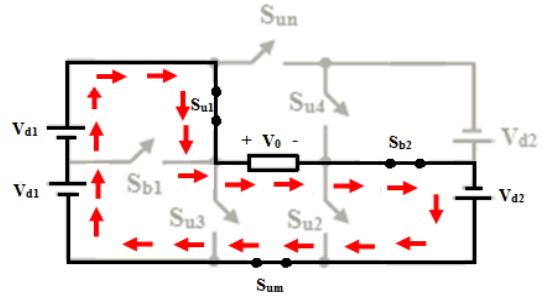

Fig. 2(f): Mode-VI (V_0= ($2V_{d1}$+V_{d2})

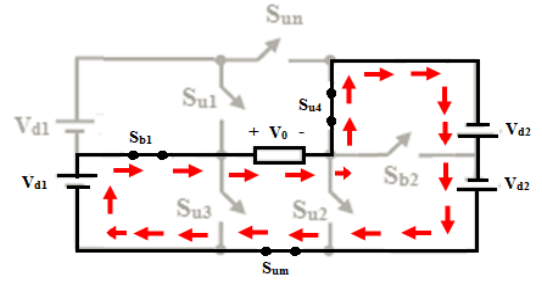

Fig. 2(g): Mode-VII (V_0=(V_{d1}+2 V_{d2})

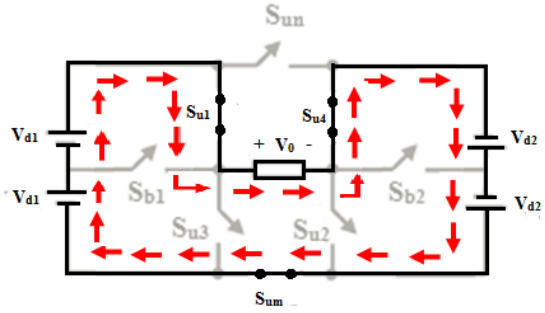

Fig. 2(h): Mode-VIII (V_0=($2V_{d1}$+2 V_{d2})

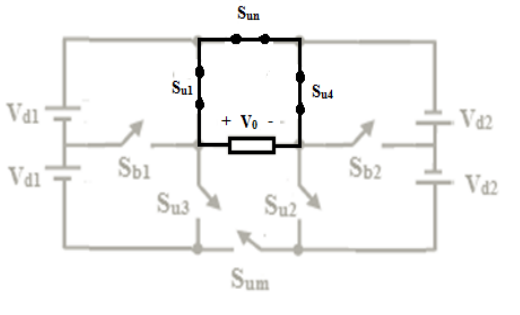

Fig. 2(i): Mode- IX (V_0=0)

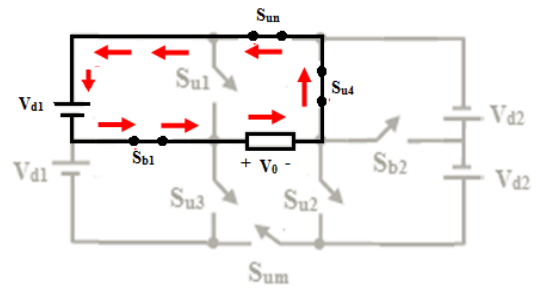

Fig. 2(j): Mode-X (V_0= - V_{d1})

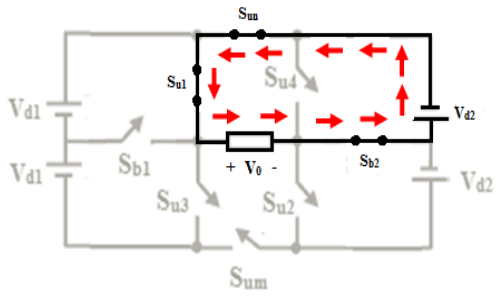

Fig. 2(k): Mode-XI (V_0= - V_{d2})

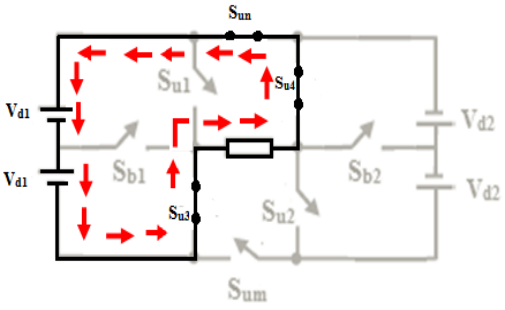

Fig. 2(l): Mode-XII (V_0= -2 V_{d1})

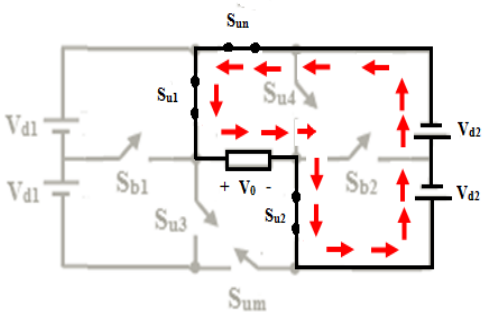

Fig. 2(m): Mode-XIII (V_0= -2 V_{d2})

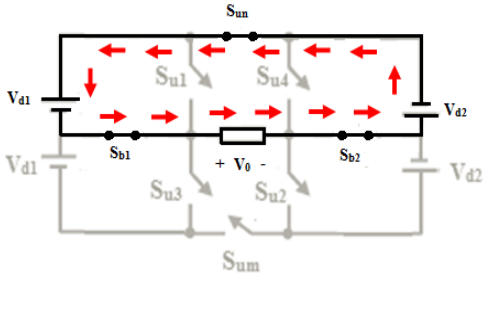

Fig. 2(n): Mode-XIV (V_0= -(V_{d1}+V_{d2}))

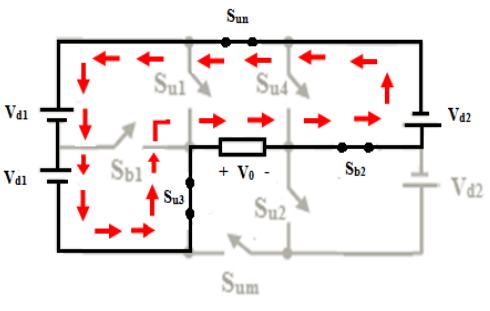

Fig. 2(o): Mode-XV (V_0= -($2V_{d1}$+V_{d2})

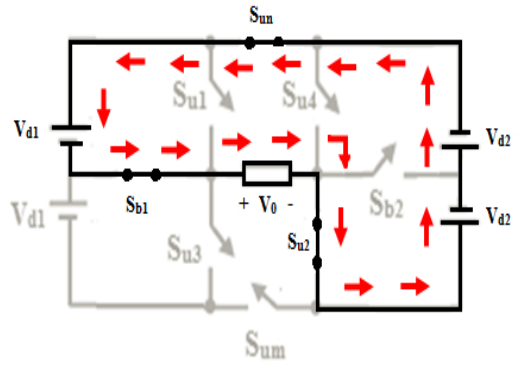

Fig. 2(p): Mode-XVI (V_0= -(V_{d1}+2 V_{d2}))

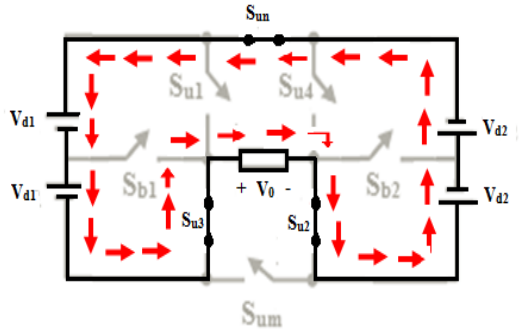

Fig. 2(q): Mode-XVII (V_0= -(2V_{d1}+2 V_{d2})

Table-I summerizes the switching states of sequential switch cascaded multilevel inverter.Here 0 represents switch is in open condition and 1 represents switch is in closed position. In order to get zero output voltage either the switching combination S_{u1}, S_{u4} and S_{un} or S_{u2}, S_{u3} and S_{um} are used. For obtaining positive voltages the switching combination must contain S_{un} as one of the switch and to obtain negative voltage levels the switching combination should contain S_{um} as one of the switch. When the switch is open the current through the switch is zero and when switch is closed, the maximum current is equal to the load current.

Table 1: Output Voltage And Switching States of the Inverter

Switching states								
S_{u1}	S_{u2}	S_{u3}	S_{u4}	S_{b1}	S_{b2}	S_{un}	S_{um}	V_o
0	1	0	0	1	0	0	1	V_{d1}
0	0	1	0	0	1	0	1	V_{d2}
1	1	0	0	0	0	0	1	2 V_{d1}
0	0	1	1	0	0	0	1	2 V_{d2}
0	0	0	0	1	1	0	1	(V_{d1}+V_{d2})
1	0	0	0	0	1	0	1	(2V_{d1}+V_{d2})
0	0	0	1	1	0	0	1	(V_{d1}+2 V_{d2})
1	0	0	1	0	0	0	1	(2V_{d1}+2 V_{d2})
1	0	0	1	0	0	1	0	0
0	0	0	1	1	0	1	0	- V_{d1}
1	0	0	0	0	1	1	0	- V_{d2}
0	0	1	1	0	0	1	0	-2 V_{d1}
1	1	0	0	0	0	1	0	-2 V_{d2}
0	0	0	0	1	1	1	0	-(V_{d1}+V_{d2})
0	0	1	0	0	1	1	0	-(2V_{d1}+V_{d2})
0	1	0	0	1	0	1	0	-(V_{d1}+2 V_{d2})
0	0	1	1	0	0	1	0	-(2V_{d1}+2 V_{d2})

3. Algorithm to Find Magnitudes of Dc Voltages & Maximum Voltage Rating

In this topology the dc voltage on each leg is same. The dc voltages on leg 1 is V_{d1} and leg 2 is V_{d2} which ia obtained from following equations

$$V_{d1} = V_{dc} \tag{1}$$

$$V_{d2} = (n_b + 2)V_{dc} \tag{2}$$

Where n_b represents number of bidirectional switch on each leg. The maximum output voltage V_{om} is given by,

$$V_{0m} = (n_b + 1)(V_{d1} + V_{d2}) \tag{3}$$

In general,

$$V_{dm1} = (2n_b^2 + 8n_b + 7)^{m-1} V_{dc} \tag{4}$$

$$V_{dm2} = (n_b + 2)V_{dm1} \tag{5}$$

The total number of level (N_l) can be found as

$$N_l = (2n_b^2 + 8n + 7)^m \tag{6}$$

The number of IGBTs are

$$N_{IG} = m(4n_b + 6) \tag{7}$$

The number of driver units are

$$N_D = m(2n_b + 6) \tag{8}$$

The number of sources are calculated as follows,

$$N_s = m(2n_b + 2) \tag{9}$$

In order to analyze cost of the inverter an important parameter is considered which maximum voltage rating on switches.

$$MVR_s = MVR_{us} + MVR_{bs} \tag{10}$$

Where MVR_{us} and MVR_{bs}represents maximum voltage rating of unidirectional switches and bidirectional switches respectively. MVR_s total maximum rating of switches. MVR_{us} is calculated as follows,

$$MVR_{us} = V_{sun} + V_{sum} + V_{su1} + V_{su2} + V_{su3} + V_{su4} \tag{11}$$

Where V_{sum},V_{sun},V_{su1}, V_{su2},V_{su3} ,V_{su4} are values of corresponding voltages on switches S_{un},S_{um}, S_{u1},S_{u2},S_{u3},S_{u4} respectively.

$$V_{sum} = V_{sun} = (n_b + 1)(V_{d1} + V_{d2}) \tag{12}$$

$$V_{su1} = V_{su3} = (n_b + 1)V_{d1} \tag{13}$$

$$V_{su2} = V_{su4} = (n_b + 1)V_{d2} \tag{14}$$

Using the above three equations

$$MVR_{us} = 4(n_b + 1)(V_{d1} + V_{d2}) \tag{15}$$

The maximum voltage rating of bidirectional switches can be found as,

$$MVR_{bs} = (V_{d1} + V_{d2}) \tag{16}$$

The switch is comprised of an IGBT with diodes.. Hence while calculating losses (conduction and switching) parameters related to IGBT and diode are considered. The conduction losses for IGBT and Diode are calculated as follows,

$$P_{con}IGBT(t) = \left[V_I + R_I i^{\mu}(t)\right] i(t) \tag{17}$$

$$P_{con}D(t) = \left[V_{di} + R_{di} i\ (t)\right] i(t) \tag{18}$$

The average conduction loss of inverter is

$$P_{con} = \frac{1}{2\pi}\int_0^{2\pi} \left(N_I(t) P_{con}IGBT(t) + N_D(t) P_{con}D(t)\right) dt. \tag{20}$$

Where $N_I(t)$ and $N_D(t)$ represents number of conducting IGBTs and diodes at instant t
The switching loss is given by

$$P_{SWI} = f\sum_{S=1}^{N_S}\left(\sum_{j=1}^{N_{on,S}} E_{t,on,Sj} + \sum_{j=1}^{N_{off,S}} E_{t,off,Sj}\right) \quad (21)$$

Where

$$E_{t,off,S} = \int_0^{t,off} v(t)i(t)dt. = \frac{1}{6}V_{SW,S}\,It_{off} \quad (22)$$

$$E_{t,on,S} = \int_0^{t,on} v(t)i(t)dt. = \frac{1}{6}V_{SW,S}\,I't_{on} \quad (23)$$

$E_{t,off,s}$, $E_{t,on,s}$ are energy loss during turn off and turn on. $N_{on,S}$ and $N_{off,S}$ represents number of turn on and turn off of switch S in one fundamental cycle. The total loss is given by

$$P_{loss} = P_{con} + P_{SWI} \quad (24)$$

4. Neural Network Controller

The appropriate switching angles of PWM inverter for a given modulation index can be generated by using NN. While using ANN controller it is necessary to train the NN either online or offline. During online training the weights and biases can be changed which is more suitable for nonlinear conditions [19]. But in offline training the weights and biases are fixed. There are two types ofcontrol algorithms can be used. They are forward propagation algorithm and backward propagation algorithm [18]. A typical multilayer NN consists of an input layer, a middle layer, and an output layer. Here NN has single input layer, one hidden layer and n output layer. The output of the neuron is represented by,

$$\chi = \beta\,(W_0\sum_{i=1}^{k}(W_i + Y_i)) \quad (25)$$

Each of the input signal flows through gain or weight. All these input weighted signals are accumulated by the summing node and then passes to the output through transfer function. The transfer function normally used will be sigmoid, inverse-tan, hyperbolic, or Gaussian type.
The expression for transfer function (sigmoid) used here is given by

$$\beta_1(y) = \frac{1}{\left(1+e^{-\mu x}\right)} \quad (26)$$

The Gaussian transfer function is expressed as

$$\beta_2(y) = e^{-\left(\frac{(\mu-\omega)}{\beta_1}\right)^2} \quad (27)$$

Back propagation algorithm is most commonly used in many applications. The figure 2 shows training of ANN for selective harmonic elimination. Modulation index is given as input and switching angle is taken as output. The output is represented by

$$\theta_i = \beta_1\left(\sum_{j=1}^{i} V_{ij}\beta_2(m, w_j)\right) \quad (28)$$

The steps in training algorithm can be summarized as follows,
– Assign arbitrary weights to the hidden layer and output layer. Input layer is assigned with unity weight.
– Modulation index is given as input and back propagation error has been determined by
$E = V_t - V_o$
– The weights can be changed based on the propagation error. the change in weight is given by

$$\Delta w = \delta\, V_o E \quad (29)$$

and δ , E represents learning rate and error.
– The new weights are determined as $w = w + \Delta w$
– The training process has been repeated until the error has reduced to least value.

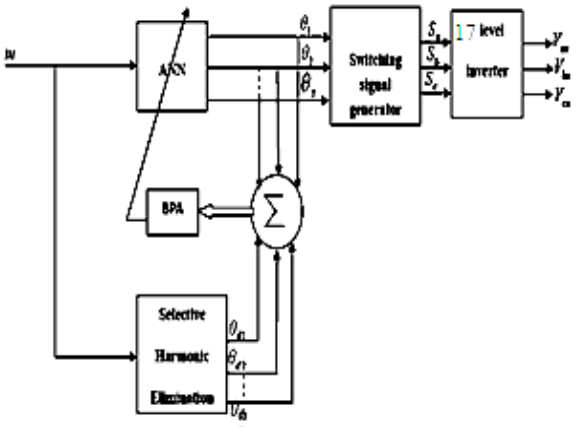

Fig. 3: Block diagram of neural network controller

5. Simulation Results

The simulation can be done by using MATLAB Simulink software. The performance of the proposed SSCMLI can be tested by simulation. Fundamental switching technique is used to generate the gating pulses of the inverter. The values of dc sources are V_{d1}=25V and V_{d2}=75V and outputfrequency is 50 Hz.The load is R-L with values of R=110Ω and L=45 mH. The output voltage is indicated in fig (5)

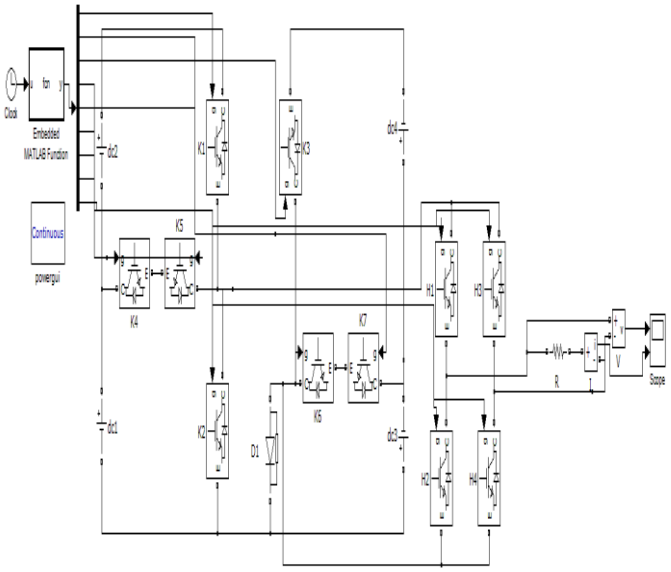

Fig. 4: Simulation diagram of proposed SSCMLI

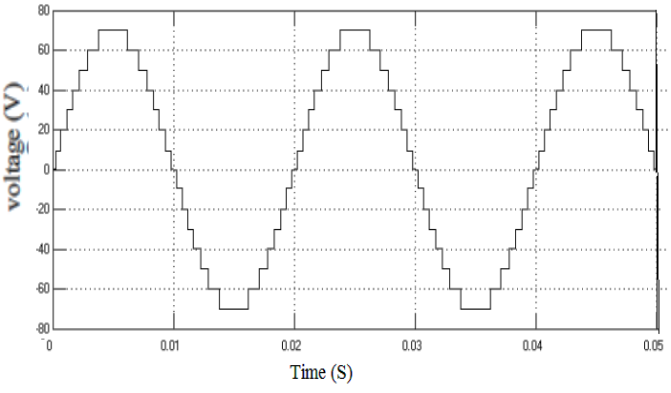

Fig. 5: SSCMLI Output voltage

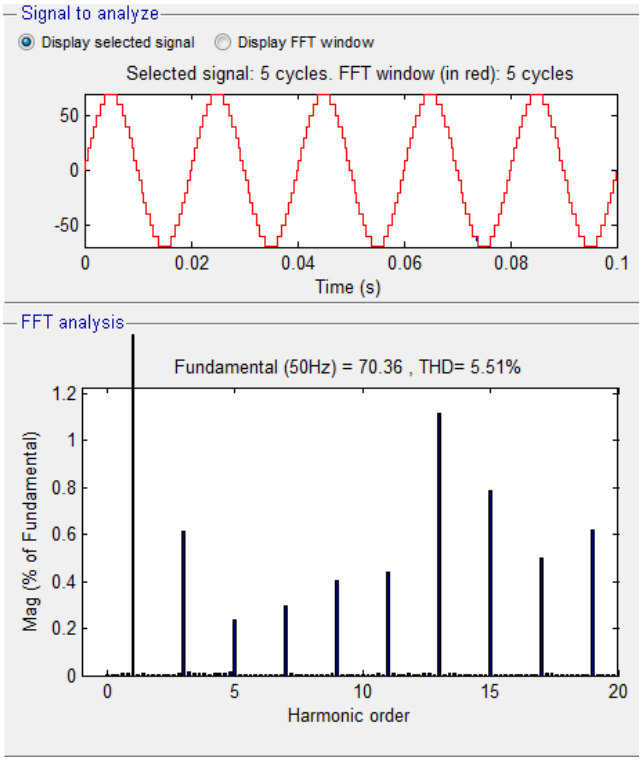

Fig. 6: FFT Analysis of proposed SSCMLI

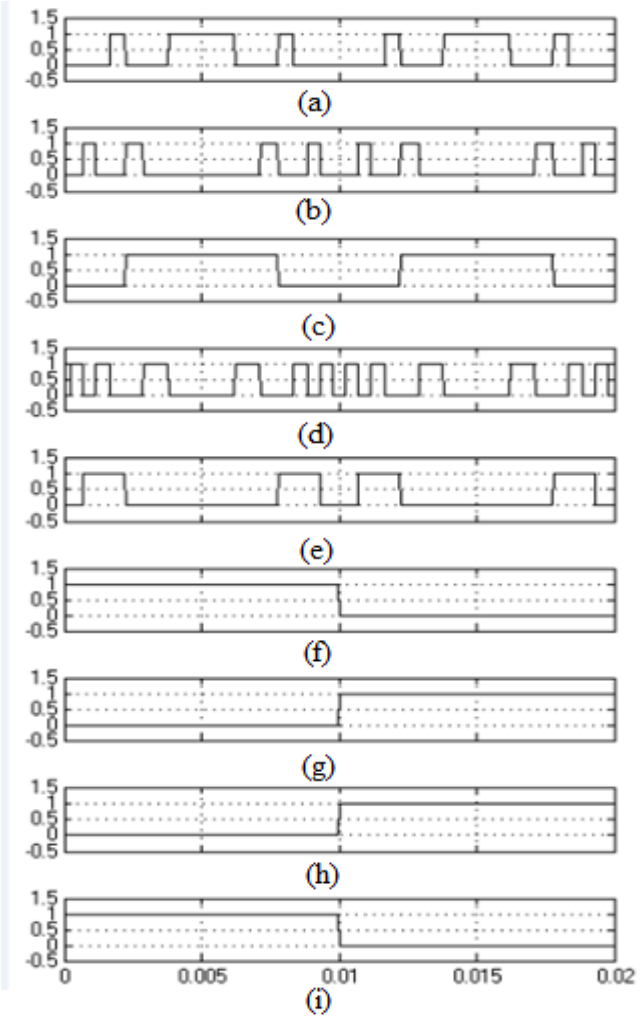

Fig. 7: Switching pulses of switches (a) switch S_{u1} (b) switch S_{u2}(c) switch S_{u3} (d) switch S_{u4} (e) switch S_{un} (f) switch S_{um} (g) switch S_{b1} (h) switch S_{b2}(i) switch S_{u1}

6. Conclusion

A novel structure of cascaded multilevel inverter is proposed. In this paper it is termed as sequential switch cascaded multilevel inverter (SSCMLI).The fundamental unit is a 17 level inverter. The structure can be extended to high number of levels. The gating signals are generated by neural network controller and back propagation algorithm is used to train the controller online.An algorithm to find the number of levels number of main switches, blocking voltages across the switches, power loss, number of DC sources and number of driver circuit has been proposed. The proposed SSCMLI requires 6 unidirectional switches, two bidirectional switches and four DC sources. The simulation result shows the performance of the SSCMLI for various load changes and change in modulation indices. The inverter has less voltage harmonic distortion which is 5.51%.

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