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Research Paper

Efficient high throughput decoding architecture for non-binary LDPC codes

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Abstract

This article, deals with efficient trellis inbuilt decoding architecture for non-binary Linear Density Parity Check (LDPC) codes. In this decoder, a bidirectional recursion is embedded to enhance the layered scheduling and decoding latency, which in turn is used to minimize the number of iterations compared to existing techniques. Consequently, it is necessary to increase the throughput for improving the efficiency of the system. In addition, a compression technique is implemented for reducing the requirements of memory and the area. Trellis based decoder was used to reinforce the check node processing. The proposed decoder for LDPC codes yields high throughput when compared to other similar decoders presented in preceding works. The designed architecture was implemented using Cadence Virtuoso software. This decoder provides a throughput of about 39.21 Mb/s at clock frequency of 190MHz.

1. Introduction

In today's modern era [3], communication has entered into day to day lives in various forms. Communication is the method of exchanging information in form of message, information between sender and receiver. Therefore, various technologies are developed for increasing long range communication and automatic data processing equipment. High throughput and effective data transmission with minimum error rate is needed for the design. Following, a lot of error controlling techniques have been introduced for error detection and correction. LDPC (Linear Density Parity Check) is one kind of techniques used. LDPC codes are good enough with high potential to support decoder that exhibit parallel operation. In mobile communications, the channel decoder should have the ability to assist different code rates and automatic error correction capability. To design efficient multimode decoder, closeness among different modes are identified, analyzed and designed as reusable hardware devices to increase the flexibility of entire architecture. These features are incorporated into a fully parallel architecture adopted in multimode LDPC decoder designs. LDPC codes are employed in order to control the errors. Furthermore, it is appropriate for implementations in decoder that that show a substantial utilization of parallelism. Moreover, Trellis modulation scheme is a used for efficient transmission of data over a band limited channels which is widely used for application with high throughput and better error controlling techniques. Hence, a trellis dependent decoding architecture for non-binary LDPC (Linear Density Parity Check) code was designed.

2. Related Works

In this article, non-binary LDPC codes are preferred than binary low density parity check (LDPC) codes because of high coding gain. Binary LDPC codes fail to achieve near-capacity performance in small or medium code length. Hence, decoding architecture is designed for non – binary LDPC codes. Injae et al[1], brings out a low-power low-density parity check convolutional code (LDPC-CC) decoder. This design combines several memory banks into single memory bank in order to diminish the power consumption. Wang et al[2] discussed about the incorporation of new parallel interleave techniques for turbo decoder. It utilizes quadratic permutation polynomial (QPP) interleaver for the cross MAP (XMAP) parallel decoding and symbol-based serial MAP (SMAP). In [6], Davey et al introduced aq-ary Sum-Product algorithm (QSPA). The algorithm is appropriate for non binary LDPC codes. This algorithm is suitable for implementation in probability domain. QSPA is an extension of SPA (sum Product Algorithm) for binary codes. QSPA algorithm is difficult to implement in log domain because it is easily affected by quantization effects and needs complex multiplication operation. Wymeersch et al[7] , proposed implemented QSPA in the log domain and named as Log-QSPA. In this algorithm, multiplication process is replaced by addition which in turn eliminates the normalization factor. In log QSPA, each and every check node processing is carried out by Brute force technique. From the results, it is inferred that when the check node is high, the check node processing in log QSPA is still considered to be a tedious task. In [8] author utilized Fast Fourier Transform (FFT) in QSPA implementation, therefore it is named as FFT-QSPA, even though this algorithm reduces the complexity but still it requires improvement for multiplication operation in the probability domain. algorithm reduces the complexity but still it

need multiplication operation in the probability domain. Songand et al [9], proposed a mixed –domain implementation of FFT QSPA. This approach utilizes look up tables for the exponential and logarithmic values. But major drawback of this algorithm is, it is superior only when the size of the look up table is very small. To avoid complexity, Min-Sum algorithm [10] and the Min-Max algorithm [11] were proposed. However, these algorithms can reduce complexity and memory requirements but does not provide high throughput and deteriorates from loss in error rate performance. In [12], QSPA algorithms are used for three serial non-binary LDPC decoders. In [13], EMS decoder was designed for non - binary LDPC codes utilizing Minimum – sum algorithm. This decoder was mainly designed to address the memory problem as well as to minimize the decoding iteration. Lin et al [14], presented a parallel architecture to benefit variable and check node processing units. In [15], VLSI architecture was designed for non-binary LDPC decoder. In this approach, symmetric properties and intrinsic shifting of QC-LDPC codes are manipulated to decrease the difficulties in routing as well as to reduce the area of memory. In [16], path construction approach was introduced to maximize the process with minimum complexity. In[17], Ueng et al discussed the efficiency of permutation network integrated into the decoding architecture. In Zhang et al[18], introduced iterative hard reliability-based majority-logic decoding (IHRB-MLGD) algorithm. IHRB algorithm brings off a substantial coding gain with less overhead. Chen et al[19], demonstrated the iterative soft-reliability-based (ISRB algorithm for non-binary LDPC codes. This architecture results in good error performance and fast convergence. Controller analysis for non-linear system has been reported [20-29].

This paper is organized as follows: Section III describes the design of trellis decoding architecture for LDPC codes, Section IV deals with results and discussion and section V includes Conclusion.

3. Trellis Decoding Architecture

In this article, trellis based decoding architecture was designed to overcome the drawbacks of existing Max Log QSPA [5]. The existing methods use complex multiplication process and are easily affected by quantization effects. In the designed architecture, the complex multiplication process is replaced by the addition process in ADD – PPN modeling for NBC (Non Binary Code) operation. It comprises of message compression and decompression for area reduction. The check node processing is reformulated by including forward and backward recursion. All these features are incorporated into decoding architecture to yield high throughput, flexibility, less operating frequency with reduced number of iterations and complexity.

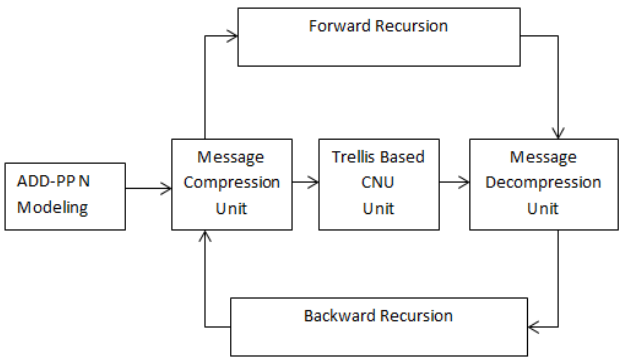

Fig. 1: Block diagram of trellis based decoding architecture

3.1. ADD – PPN Modeling

In this section, the decoding architecture for ADD-PPN (Add – Permutation Polynomial) modeling for LDPC codes is presented. The proposed ADD-PPN architecture modeling consists of permutation network, multiplexers, adders and flip flop for efficient execution of recursion steps.

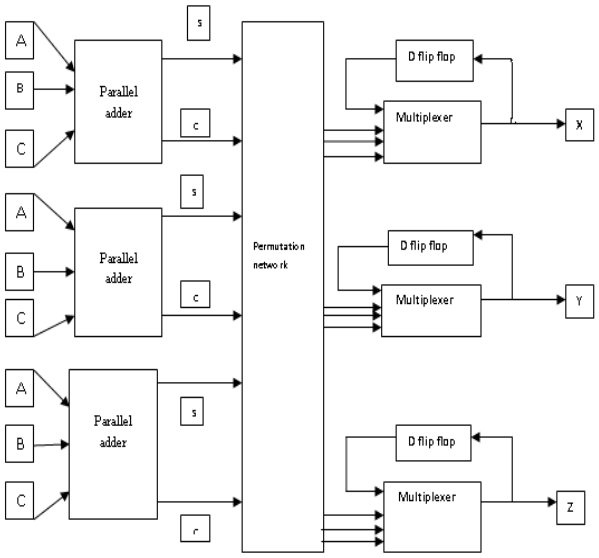

Fig. 2: Block diagram of ADD-PPN Architecture

3.2. Permutation Polynomial Network (PPN)

PPN modeling helps in handling the decoding operation related to addition operation over finite fields in check node operations. It facilitates the layered decoder to be accomplished efficiently. In order to maximize the throughput, the permutation network and the minimum value filter are utilized to devise a trellis based decoding architecture. The inputs given to adder are processed simultaneously. Therefore, a permutation polynomial network is necessary to shuffle the outputs of the adder in order to transfer uniformly in order.

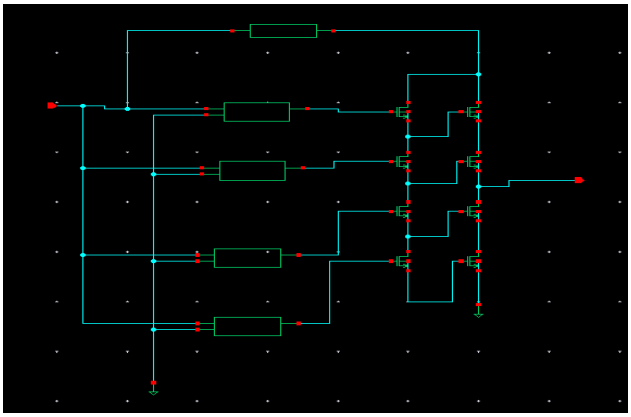

Fig. 3 Permutation Polynomial Network

3.3. Adder

The adders are manipulated in decoding architecture to reduce the power consumption as well as to maintain full voltage swing at reduced supply voltage. It has improved power delay product and better noise immunity. The inputs are forwarded to the adder followed by the permutation network for further processing. The usage of adder results in greater noise immunity and desirable power delay product.

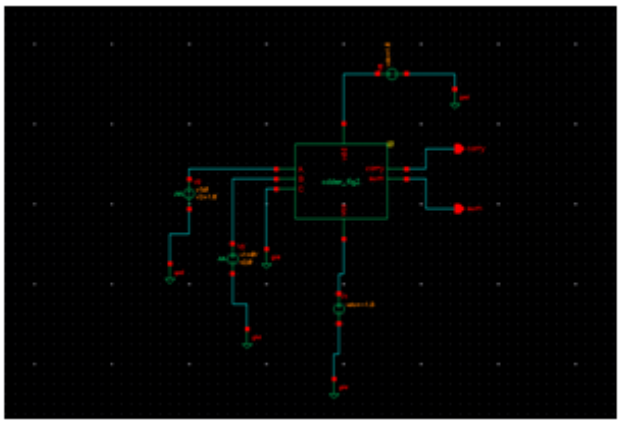

Fig. 4: Adder circuit for the permutation network

3.4. Flip-flop

Flip-flops are often used as a storage device. It stores the output value from the multiplexer and values are restored when it is needed for further processing. The power consumption of the flip-flop is reduced by deactivating the clock independently when it does not have to change its value.

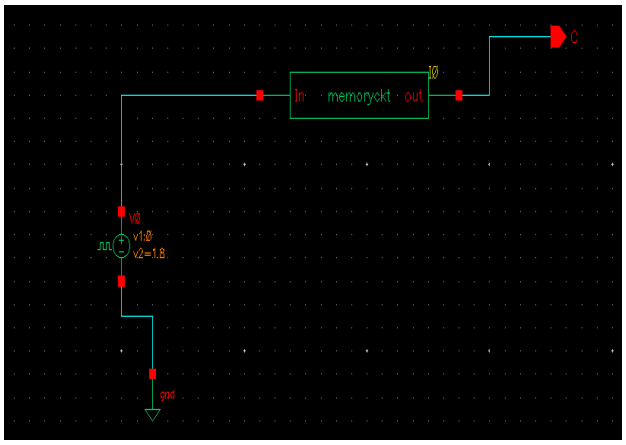

Fig. 5: Flip Flop circuit coupled in permutation network

3.5. Multiplexer

Multiplexing technique is utilized to minimize the number of electrical connections required for each component. This further reduces the complexity and increase the flexibility of the decoder. Here, the driver signals are activated over a group of rows and columns at a time, but finally it switches to a single output.

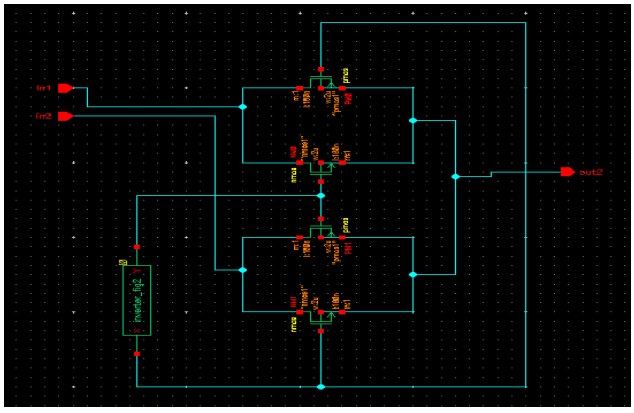

Fig. 6: Multiplexer for the permutation network

3.6. Bidirectional recursion

Bidirectional recursion and layered scheduling are incorporated into the decoding architecture for maximum throughput. The number of iterations is reduced due to the layered scheduling and number of frequency clock cycles is reduced due to integration of bidirectional scheduling which includes forward and backward recursion as a parallel operation. Besides, bidirectional scheduling also decreases the latency compared to unidirectional scheduling.

TRELLIS BASED MAX ADD ALGORITHM [[4]

Step 1 (initialization)
At initial condition € = 0 and t=0, it checks for the starting node to travel further
Step 2 (forward recursion)
The node travel in forward direction when
€ > t and the path metric have the following condition
(d + 1) >= t1
Step 3 (backward recursion)
The node travel in reverse direction when
€ < t and the path metric have the following condition
(d + 1) < t1.
Step 4 (end of the process)
After completing step 3, it comes back to the initial node and check for the next node and the same process is repeated.

3.7. Message Compression and Decompression Unit

The decoding architecture uses two register memory banks to store posteriori messages and check to variable message. The memory register banks are small in size and reside in larger area. Message compression and decompression techniques are introduced to lower the area of the decoder. In addition, this technique also supports the memory bank to store APP and check to variable messages along with their corresponding log – likelihood ratios (LLR).

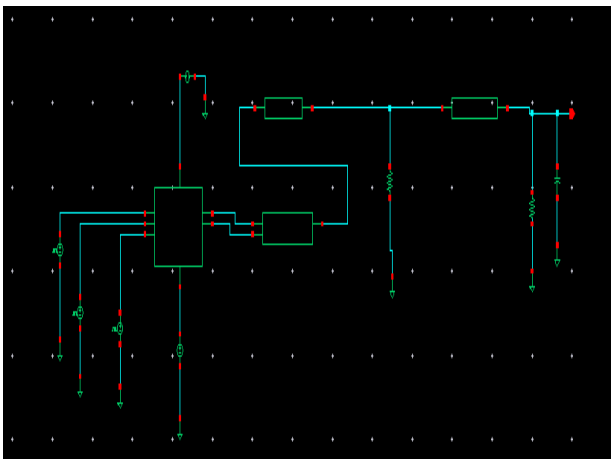

Fig. 7: Message compression and decompression unit

3.8. Trellis Based CNU Unit

The figure 8 shows the trellis based check node unit (CNU). It consists of a forward unit, a backward unit and a pair of LLR units. The two units are named as LLR unit 1 and LLR unit 2.The forward unit consists of multiplexers, filters, ADD-PPN node and forward memory unit. The multiplexer selects the initial input values and gives to the permutation network. The NBC network reorders the received messages and shuffles and forward it back again to the multiplexer. The filter unit consists of arbiter unit and serial unit. The serial unit calculates the maximum threshold voltage and the arbiter unit lists the values that exceed the maximum threshold voltage. The completed forward recursion unit values are stored in forward memory unit. The backward

recursion operation follows the similar procedure as the forward recursion process. The LLR unit 1 consists of filter and NBC unit. The estimated information resulting from the forward memory unit are directed to the LLR unit 1. Similarly, the backward computation information from the backward memory are forwarded to the LLR unit 2 to obtain the check to variable message. Both forward and backward computation information are transferred successively. Hence reduces the number of iterations with reduced frequency clock cycles.

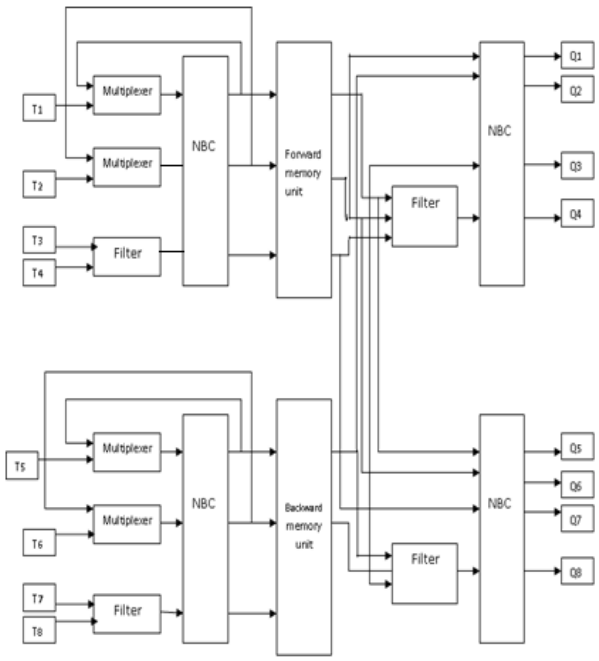

Fig. 8: Trellis check node unit decoding architecture with permutation network

4. Results and Simulation

Here, the implementation result for the trellis decoder is shown in figure 9. This architecture is implemented using cadence virtuoso tool. It consists of permutation network, message compression and decompression unit, forward and backward memory unit and filter circuit

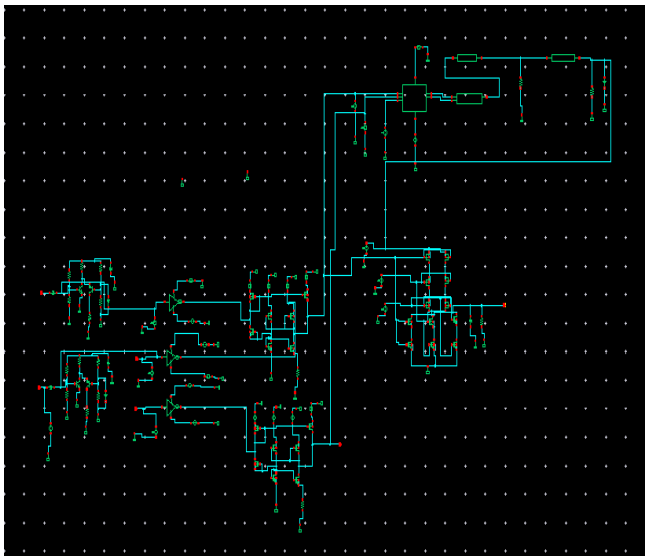

Fig. 9: Trellis based decoding architecture

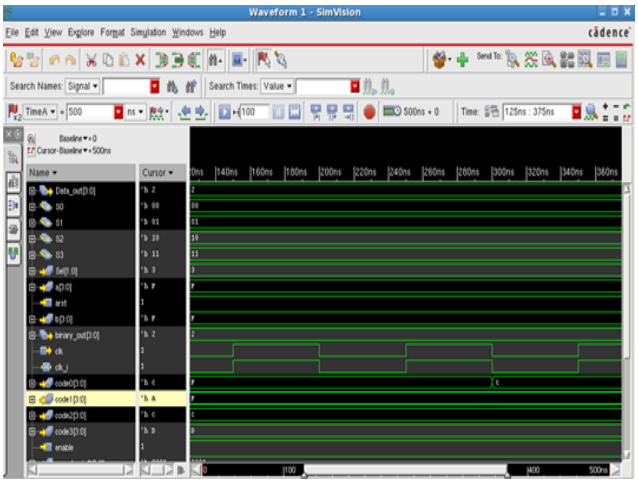

Fig. 10: Simulation Results of LDPC Code Generated

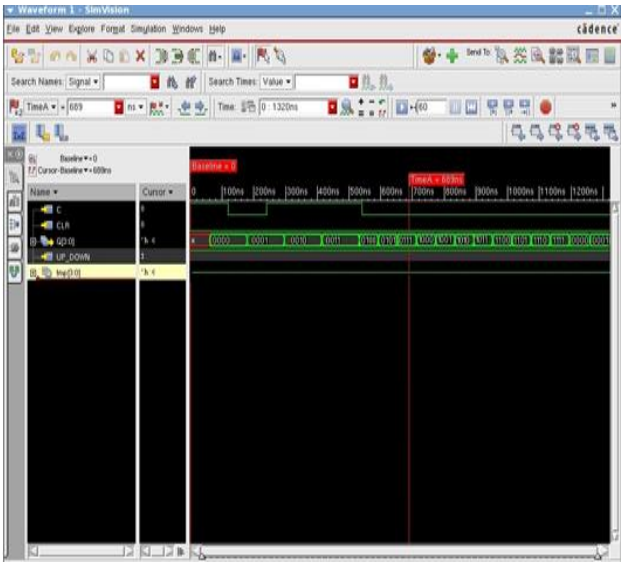

Fig. 11: Simulation Results of Bidirectional recursion

The figure 12 shows the transient response of the decoding architecture. It is analysed to determine the response of system to change from equilibrium.

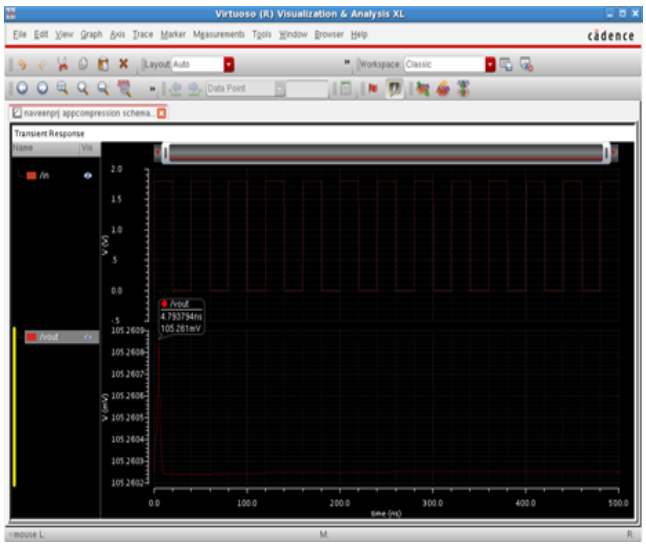

Fig. 12: Transient response of trellis decoding architecture

The Figure 13 clearly depicts the DC response of decoding architecture to determine the operation of the system, Here the input given is 0 to 5 V and obtained output is 2.375 V.

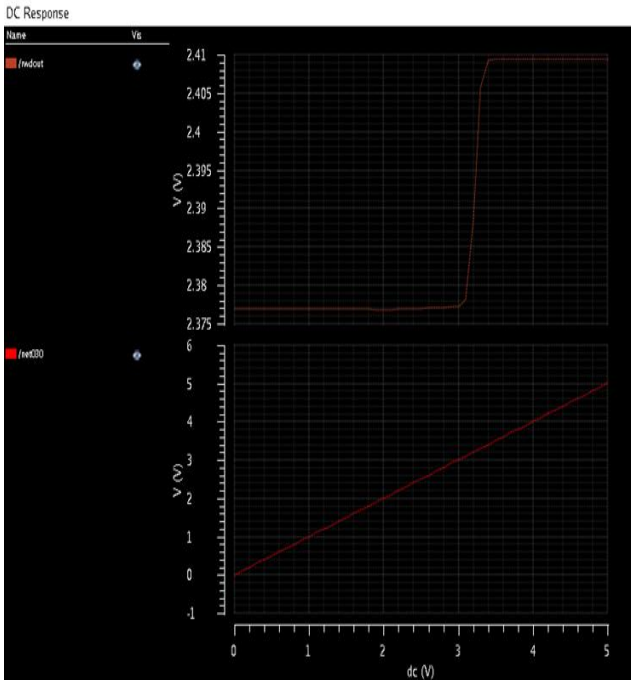

Fig. 13: DC response of trellis decoding architecture

The throughput of decoding architecture can be calculated as follows:

Throughput = $\frac{N \times log_2(q) \times f_{clk}}{N_{it} \times N_c}$

Where N_c is the number of clock, f_{clk} is the clock frequency and N_{it} is the number of iterations. In the designed decoder a throughput of 39.21 Mb/s is achieved.

Table 1: Comparison of different algorithm

Algorithm	Frequency(MHz)	Iterations	Throughput(Mb/s)
Selective input Min-Max	260	15	8.84
Max log QSPA	250	5	27.44
Trellis based Max -add algorithm	190	2	39.21

5. Conclusion

In this work, trellis based decoding architecture with efficient check node processing is Presented. This decoder is incorporated with parallel forward and backward recursion for efficient processing. The layered scheduling and decoding latency are integrated to reduce the number of iterations with reduced number of frequency clock cycles compared to the existing method. Therefore, the throughput can be maximized for improving the efficiency of the system. In addition, a compression and decompression techniques are embedded into the architecture to shrink the area and memory size. The proposed trellis decoding architecture for LDPC codes achieves the highest throughput and better error-rate performance than several existing preceding decoders. In future, decoding architectures with high error controlling techniques are planned to design and implement.

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