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Research paper

A novel 3-D-IC test architecture-a review

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Abstract

Here, this paper completely examines the crosstalk noise of Through-Silicon-Vias (TSVs) in high speed operations by means of a novel 3-Dimensional-IC Test structural design. In order to decline the crosstalk, the fast rise time devices have to be circumvented except they are essential for performance in some certain circuit parts. It must be noted that this system simultaneously examines the TSVs and the memory and does not require spending additional area for a test pattern generator in case of the TSV test. With the intention of reprocessing the test patterns of new-fangled memory BIST, the value of "data" or "address" need to be fixed to some specific values. In accordance with the outcomes of the TSV grouping, here also implemented a high-efficiency, low-area-overhead TSV test structural design. The amount of test cycles essential for the purpose of finding failing TSVs and regulate the fault category effectively than that in related work.

Keywords: *TSV, Cross talk, integrated circuits, BIST.*

1. Introduction

In this paper, Three-dimensional integrated circuits (3-Dimensional-ICs) have been formulated for the purpose of overcoming the current drawbacks of the IC construction procedure through dropping routing range and power intake at the same time increasing communication bandwidth. 3-Dimensional-ICs are effectively built through the process of stacking multiple dies with interconnection known as Through Silicon Via (TSV). 3-Dimensional integration is one of the potential candidates that can be used to alleviate these problems. fig 1.1 depicts a general structure of three-dimensional stacked ICs (3-Dimensional-SICs) where a memory is stacked on logic (CPU). The connection between both dies goes through TSVs [1]. 3-Dimensional-SICs based on TSVs are one of the promising solutions to alleviate the aforementioned problems. Through Silicon Vias (TSVs) are vertical electrical connections between stacked dies that undergo the silicon substrate and are packed with a conducting substance, for instance, copper or tungsten [2]. Following are the few advantages of TSVs,

- Reduced power consumption due to reduced wire length as the wires between components do not have to travel across large chip areas.
- Short global interconnect delay due to short vertical interconnects.
- High communication bandwidth is achievable, as the vertical interconnects between dies are perpendicular to the area surface and not only on the perimeter of the chip.
- Heterogeneous die integration, as each die can be effectively manufactured in a various technologies and improved for explicit prerequisites like area (DRAM) and speed (CPU).

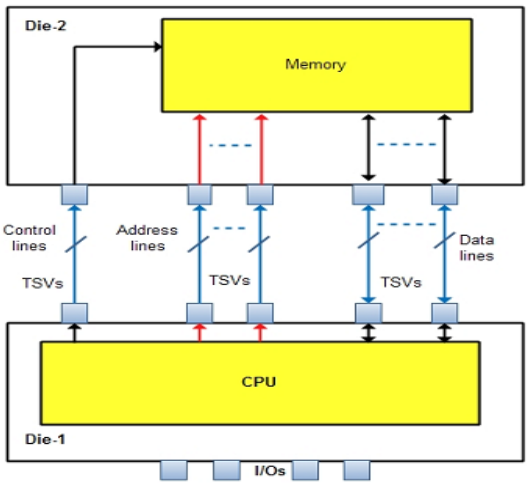

Fig. 1: General structure for 3D stacked IC (Memory-on-Logic)

2. Related works

Very Large Scale Integration (VLSI) circuits are scaled down for the purpose of increasing device practicality and working. 3-D IC strategy has demonstrated the capability to handle the prerequisites for newfangled generation of ICs through assorted amalgamation of multi-disciplinary schemes. In the midst of potential resolutions for joints among 3D slanted IC, TSV tools has materialized as a sustainable, besides well-organized solution owing to its small interconnect extent, elevated density, and small imprint. On the other hand, TSV tools generate different encounters and analyzing TSV interconnects necessitate advancement of novel Design-For-Test (DFT) schemes and test access tools [3-5].

Quite a lot of test schemes have been formulated in the literature for the purpose of addressing the challenges of testing pre-bond

and post-bond TSVs. In case of Pre-bond TSV tests, it senses defective dies before stacking and in case of post-bond tests, it covers flaws because of misalignment and damaged bonding. Hence, a die-level wrapper dependent on IEEE 1500 has been proposed into support TSV testing. Dedicated probe pads on non-bottom dies and intra die interconnects called "test elevators" between stacked dies are introduced in this method.

A sense amplifier is utilized for the purpose of detecting pre-bond TSV flaws as a result of resistive shorts . This method requires an accurate tuning and standardization of on-chip circuitry for the purpose of fault discovery. Extremely sensitive amplifiers have also been utilized for the purpose of blinding TSVs to notice pre-connection capacitive flaws. TSV pinholes and emptiness are sensed with the assistance of a resistance dimension scheme by means of a leakage-current sensor and a capacitive bridge. Hence, a DFT dependent scheme for pre-connection testing is formulated in which a collection of TSVs are traced simultaneously through a probe needle to generate a network of TSVs [6]. This approach necessitates a straight access to TSVs through contact probes. Hence, a socket based solution by means of micro-scale contactor is carried out for the purpose of examining TSVs and micro-bump arrays. Also, the contactor can be formulated with small pitch and based on decent electrical connection among the contact points. As a result, an all-digital pre-bond test solution by means of ring oscillator is formulated for the purpose of detecting resistive exposed and seepage errors in accordance with the dissimilarities of oscillation frequency.

Although, the new generation of MEMS based test probes supports the pitch constraint, however they do not completely exclude the possibility of scrub marks and physical integrity degradation due to probing. Contactless probing resolves many of the constraints of straight TSV probing. It must be noted that, they do not necessitate routine cleaning or preservation as they are not exposed to physical force. They also present better mechanical performance and durability than the conventional probes.

With the intention of increasing the coupling efficiency, a resonant inductive coupling has been formulated and implemented. This scheme as compared against the traditional coupling supports an extended communication range. The authors have formulated three probable wireless communication schemes known as RF, near-field and optical-inductive and capacitive coupling illustrating the near-field schemes [7]. The electrical characterization of TSV prepared through tungsten and hybrid Cu-adhesive wafer bonding is reported in which different techniques are utilized to determine TSV parameters. A delay testing and characterization method for interposer wires. However, this [9] scheme completely based on a fixed clock frequency produced through a ring oscillator, which can produce test seepages or over-testing when different functional frequencies (for different dies on the interposer) are used for response capture. Therefore, its drawback is the inflexibility and potential ineffectiveness in realistic scenarios.

The standard test access port (TAP) and boundary scan (JTAG) are obvious candidates for the testing of interposer interconnects. JTAG can effectively unite the I/O pins of the dies on the interposer, and can be completely regulated by means of a finite state machine. On the other hand, the exploitation of JTAG alone is not sufficient for detecting interposer interconnect defects [10]. With the standard TAP controller, since the Capture DR and Update DR states are separated through over and above one clock cycle, SDDs cannot be detected through at-speed testing. More in recent times, an interposer assess structural design in accordance with the delays to the standard was proposed and evaluated. However, the boundary-scan cells involved are not well-suited with the JTAG structural design. Furthermore, subsequently the TAP controller is not utilized in this test procedure, the entire control signals must come from the tester, which increases the complexity of test.

The TSV test architecture in its embedded into an existing memory Built-In Self-Test (BIST) structural design. The foremost indication is to exploit the patterns produced through memory BIST circuitry for the purpose of testing TSVs. This work simultaneously examines the TSVs and the memory and does not require spending spare zone for a examination pattern generator for the purpose of assessing the TSV.

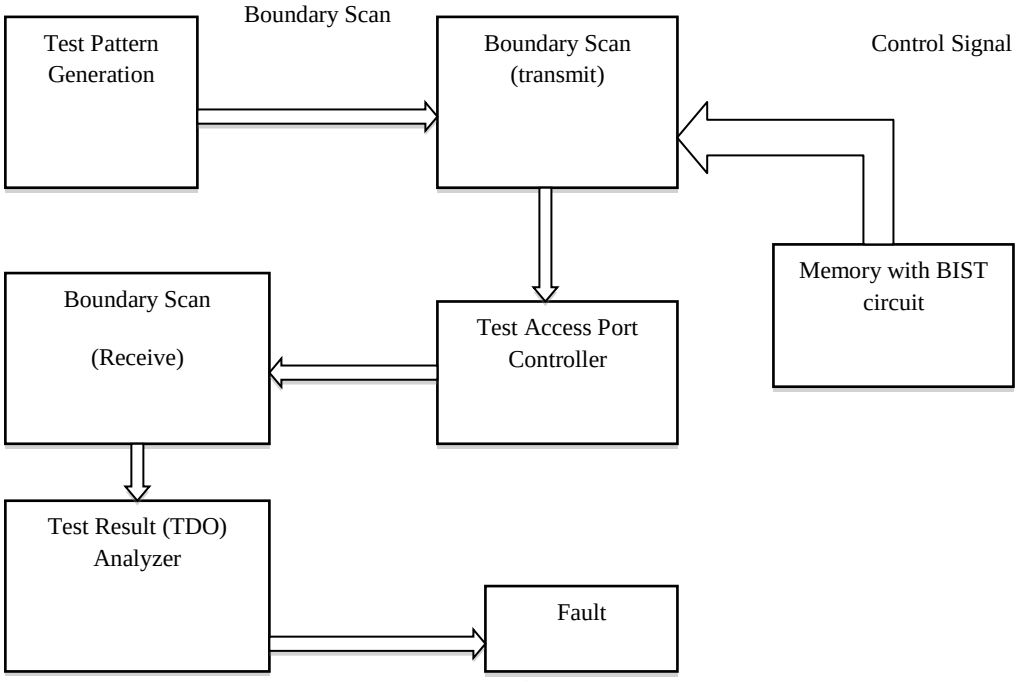

Fig. 2: Block diagram of conventional approach

3. Proposed approach

3.1. Fault Model

The Maximum Aggressor Fault (MAF) model is extensively implemented for the purpose of crosstalk faults. In case of coupling capacitances and inductances among one victim and one neighboring aggressor cable are inattentive from the actual path

into a connection component Z. it must be observed that the crosstalk consequences among two aggressors and a target cable are exposed in fig 1. In this kind of aggressor-victim circumstance, signal changeovers on a solitary cable are disturbed through the crosstalk noise tempted through transitions on neighbor wires. In case of the maximum aggressor fault model, it considers the poorest case of crosstalk, supposing that the entire aggressors change in the same track simultaneously. However doubtful, it safeguards the discovery of crosstalk errors generated through whichever subsection of aggressors.

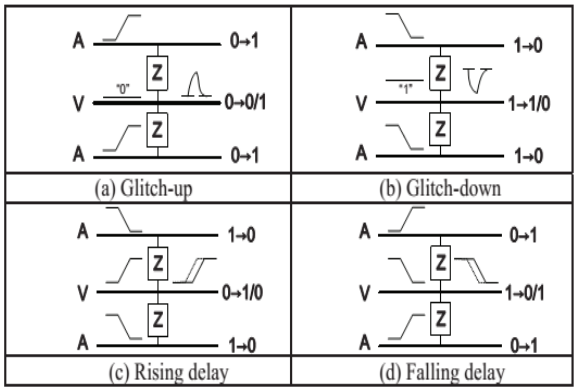

Fig. 3: Maximum aggressor fault model

In the above Fig 3, the resultant (a) glitch-up fault, (b) glitch-down fault, (c) rising delay fault, and (d) falling delay fault are clearly summarized. The examination of every single fault category necessitates two different patterns.

The initial pattern determines the preliminary form of the victim and the aggressors. The subsequent pattern transforms the rate of the aggressors and possibly will transform the rate of the victim. When the transformations on the aggressors disturb the victim, the rate on the victim will be completely dissimilar from the predicted value for the subsequent pattern [8]. Subsequently, the TSV grouping schemes is defined in keeping with the crosstalk fault influence limit.

3.2. TSV grouping

3.2.1. Motivation

In case of TSV crosstalk fault assessment, 4 aggressor TSVs very neighboring to a victim TSV have been taken into account (e.g., [9]), i.e., merely the crosstalk fault consequences made by aggressor TSVs that are approximately 1 unit ahead of the victim TSV are taken into account, in which a unit is described as the extremely smallest distance among 2 TSVs. This scheme completely categorizes all the TSVs into two different groups [Figure 2(a) for a 4 x 4 TSV matrix]. Here a TSV grouping method is formulated for the purpose of partitioning the TSVs in accordance with the different crosstalk fault limits.

3.2.2. TSV modeling for grouping and valid distances

Here it is considered that TSVs are positioned in a systematic arrangement of rows and columns as given in Figure 4.3, in which every single minor square characterizes one particular TSV and its size completely based on the authentic arrangement. Here in this situation, the space in the middle of two TSVs possibly be 1, √2, or alternative length. The likely distances đ can be oversimplified with the term đ=$\sqrt{a^2 + b^2}$, in which "a" and "b" indicates the positive integers or 0. As a result, some distances, like √3, √6, do not be existent.

3.2.3. TSV grouping method

With the intention of truncating the TSV test period, it is essential to make best use of the amount of TSVs that are examined at the same time, i.e., take full advantage of the number of TSVs fractioned into one group [4]. In case of a crosstalk influence limit of k units, it is regarded that the crosstalk effect produced by aggressor TSVs that are over and above k units ahead of the victim TSV v is slight.

As a consequence, the neighboring victim that can be moved to the similar group as (and be examined at the same time) should have a space to v of beyond k units. For that reason, this formulated scheme will place those TSVs that have the least valid distance that is in excess of the prearranged crosstalk impact limit into the same group. This way of process is continuously applied recurrently in order to discover the entire TSVs in the TSV array that can be examined in parallel. At that point, the TSVs of the subsequent group are chosen from the left over TSVs.

The amount of sets that are generated through this scheme is regulated through the side length of the square form, i.e., the smallest effective distance đ in excess of the influence limit. In the meantime, the extent of every single square of size length đ will be the same as the extent of the maximum set of TSVs that are not in the similar group, a square with area đ² encircles đ² dissimilar TSVs. This suggests that đ² exceptional groups will be acquired. Figure 5 demonstrates the TSV combination consequences for dissimilar crosstalk fault limits r of up to √10 units.

Take a fault limit of 1.5 units for instance. 1.5 is in the interim from √2 to 2. Henceforth, the distance stuck between the TSVs in the similar group has to be 2 units. The entire TSVs further down test are fractioned into only 2^2=4 groups. In case if the amount of TSVs under test rises, the amount of groups will not transform.

3.3. Proposed BIST architecture for TSV testing

This TSV test structural design is shown in Figure 4. The structural design can be partitioned into a Receive Unit at the lowermost die and an Apply Unit in the topmost die. Here, reprocessed the prevailing Boundary Scan Cells (BSCs) that are employed for pre-bond die test [9] in order to spread over and obtain the test data and reaction, correspondingly.

The general block diagram of the proposed system is shown in Fig 5. For the reason that, BSCs are effectively reused for the purpose of applying and receiving test data, it is essential to control their operations during testing. Instead of adding individual control signals per BSC, which would incur high routing overhead, we multiplex the control signals generated by the TAPC with committed signals for the effective functioning of the TSV Test Mode [10]. For the best processing of "Shift DR," "Update BSR," "Clock BSR," and "Mode" signals, multiplexers are perfectly added which are regulated through the "TTM en" signal.

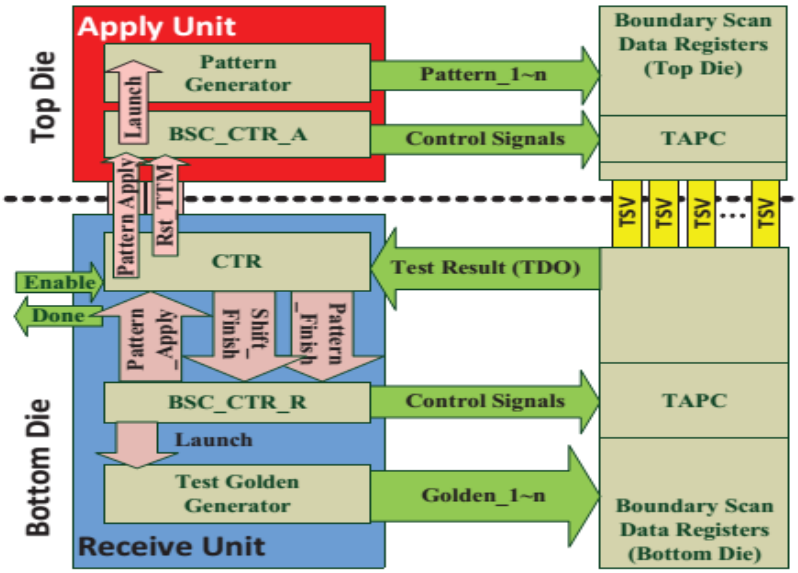

Fig. 4: TSV test architecture

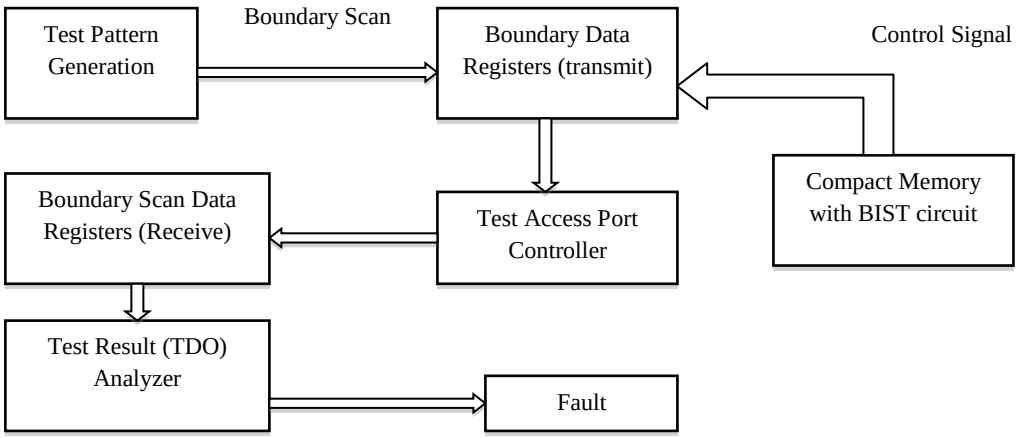

Fig. 5: Block diagram of proposed approach

4. Results and discussion

4.1. Implementation Results

The proposed system was implemented in Xilinx Virtex5-XC5VLX30 device. Detailed implementation results of individual blocks are listed in Table 1.

Table 1: Proposed Implementation Results

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	214	19200	1%
Number of Slice LUTs	2555	19200	13%
Number of fully used LUT-FF pairs	23	2746	0%
Number of bonded IOBs	75	220	34%
Number of BUFG/BUFGCTRLs	1	32	3%

The area of IO bonds of the existing system are taken for comparison, which consumes 64% and then evaluated the speed of conventional method, consumes 53.7 ns. The maximum frequency is obtained as 18.6 MHz. The power consumption of conventional method utilizes 14.4% & 64.1% of logic gates and IO's when it was implemented in Xilinx Virtex5-XC5VLX30 device.

4.2. Performance parameters of proposed system

4.2.1. Area utilization

The area consumption of individual gates, flip flops, buffers, memory are listed and are shown in Fig. 5. The area of IO bonds consumes 34%, which is comparatively less than previous method.

Proposed_work Project Status			
Project File:	VER_3.xise	**Parser Errors:**	No Errors
Module Name:	Proposed_work	**Implementation State:**	Synthesized
Target Device:	xc5vlx30-3ff324	**•Errors:**	No Errors
Product Version:	ISE 12.1	**•Warnings:**	137 Warnings (86 new)
Design Goal:	Balanced	**•Routing Results:**	
Design Strategy:	Xilinx Default (unlocked)	**•Timing Constraints:**	
Environment:	System Settings	**•Final Timing Score:**	

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	214	19200	1%
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Number of fully used LUT-FF pairs	23	2746	0%
Number of bonded IOBs	75	220	34%
Number of BUFG/BUFGCTRLs	1	32	3%

Fig. 6: Area consumption of proposed system

4.2.2. Speed utilization

The evaluated speed of conventional method consumes 54.56 ns. The maximum frequency is obtained as 18.3 MHz as shown in below Fig 7. The speed is considered to be the lower value on comparison. Hence, it is taken as consideration in our future work.

```
Timing Summary:
---------------
Speed Grade: -3

   Minimum period: 54.566ns (Maximum Frequency: 18.327MHz)
   Minimum input arrival time before clock: 2.786ns
   Maximum output required time after clock: 3.790ns
   Maximum combinational path delay: No path found

Timing Detail:
--------------
All values displayed in nanoseconds (ns)
```

Fig. 7: Speed consumption of proposed system

4.2.3. Power utilization

The power consumption of conventional method utilizes 14.2% & 34.1% of logic gates and IOs, when it was implemented in in Xilinx Virtex5-XC5VLX30 device. The utilization of power is reduced and provides better outcome compared to existing method (in below Figure 8).

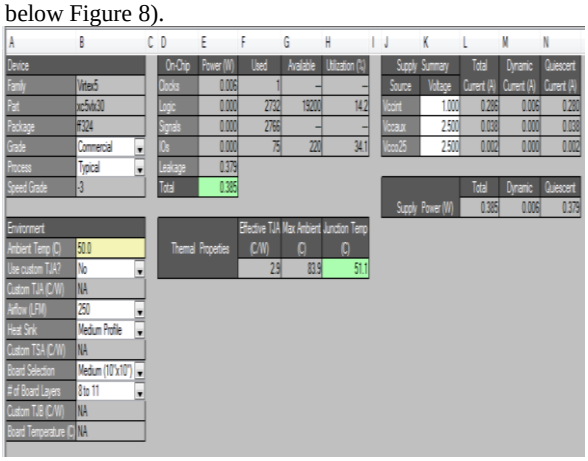

Fig. 8: Power consumption of proposed system

4.3. Performance Comparison

The evaluated implementation results of area, power and speed are listed & compared for both the approaches (tabulated in Table 2).

Table 2: Comparison Results of Base Work and Proposed Work

Parameters	Base work	Proposed Work
Area (IOBs)	64%	34%
power(logic & IOs)	14.4% & 64.1%	14.2% & 34.1%
Speed	53 ns	54 ns

5. Conclusion

Thus, the system completely concentrates on the TSV post-bond assessment for continuous crosstalk faults. Initially, a grouping scheme is formulated for the purpose of TSVs under test, which utilizes various crosstalk fault impact limits into account. The entire TSVs in one set can be effectively tested at the same time. The amount of sets does not completely based on the amount of the TSVs under assessment. Furthermore, a hardware-efficient BIST structural design is provided that effectively reuses the prevailing boundary scan cells and circuitry. With the intention of diminishing the test cost, it is also presented a test-path scheme and scheduling approach that completely diminishes a composite cost function in accordance with the assessment time and the design-for-test overhead in terms of further TSVs and controls the redundant operations using assessment access port. Here, a detailed simulation outcome is presented for the purpose of demonstrating the effectiveness fault detection, and synthesis results for the purpose of evaluating the hardware cost per die. Here, furthermore presented test-path design and test-scheduling results for the purpose of highlighting the success of the compact memory for the optimization technique.

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