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Research paper

Effect of radius on various parameters of cylindrical surrounding double-gate (CSDG) MOSFET

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Abstract

The MOSFET is an integral component of electronics device and scaling the device is continuously in progress. This research work introduces a novel structure of the Cylindrical Surrounding Double-Gate (CSDG) MOSFET to improve scaling and to suppress Short Channel Effect (SCE). In order to achieve this improvement, the drift-diffusion components are used to analyze the drain current of the device through the Pao-Sah integral. Then transconductance is derived to indicate an improved performance of the proposed design. The capacitance characteristics of this MOSFET is also analyzed through the equivalent capacitance model as well as the analysis of the carrier mobility, in which it has been observed that scaling of the device supports increase in mobility of the charge carrier.

Keywords: *CSDG MOSFET; Carrier Mobility; Drift-Diffusion Component; Nanotechnology; Pao-Sah Integral; Transconductance; VLSI.*

1. Introduction

The Metal Oxide Semiconductor Field-Effect Transistor (MOSFET) is a basic semiconductor device in the production of Very Large Scale Integrated (VLSI) circuits. Its characteristics of simple structure, low power consumption and economical fabrication have facilitated its application in the design of portable electronic devices [1, 2]. Also, the high impedance of the MOSFET makes it useful for low-current circuits to operate effectively. Furthermore its structural framework helps in realizing a high switching speed [3], [4].
With the operation of MOSFET, various models have been initiated in order to bridge the designer ideas with the manufacturing processes. The effectiveness of these models are verified to check the sustainability at different conditions. Most of these analysis are explained using the Gradual Channel Approximation (GCA) [5], [6]. Taylor [7] developed a 1-D model based on assumption of some parameter in the short-channel MOSFET. The work intends to connect the activities in the sub-threshold region to the structure and fabrication of the device but with a little disadvantage of imprecise prediction of Short Channel Effect (SCE) and disregard for gate oxide dimension.
Ng et. al. [8] attempt to improve the Moore rule by introducing a generalized approach to scaling the MOSFET using the amount of SCE as an input variable. In this work, the authors derived an empirical formula for MOSFET with channel length of 5 μm or less. However, the derivation was based d on observation than a satisfactory analytical perspective. The Meyer Model considered both the depletion and inversion layer with respect to Gauss law and the assumption that both the semiconductor body and the source are grounded [9]. The charge per unit in this model is the sum of the depletion charge density and the inversion charge density. With the simplicity and almost accurate predictive attribute of this model in simulations, it is still insufficient in predicting correct capacitance in Metal Oxide Semiconductor (MOS) charge pumps, dynamic memory circuits and capacitance circuit [10]. Yu et. al. [11] introduce a 2-D analytical model to minimize the channel length of the MOSFET. This approach develop channel length scaled to 0.1 μm with scaled oxide and other parameters. However, no proper explanation on SCE was considered.
The advantage of scaling in MOSFET include smaller dimension as well as improved performance. Both are essential consideration in the design of VLSI circuits [2]. However, the challenge of SCE necessitate the need in improving the characteristics and operation of MOSFET, which can be improved by Double-Gate (DG) MOSFET. Having two conducting channels of small width which are controllable by the two gates at both the upper and lower part of the substrate to overcome SCE is the main objective of the device.
Taur et. al. [12-14] have proposed a 1-D analytical solution to a lightly doped or undoped symmetric DG MOSFET by introducing a mobile charge to the Poisson equation. The work was able to validate the drain current of the symmetric DG MOSFET at saturation, linear, and sub-threshold region. This analysis, however, did not consider some physical effects like SCE and quantum effect. The mobility model was also ignored. Lu and Taur [15] extended the analysis of Taur et. al. [2], [12-14] by applying the quasi-Fermi potential, while not equating the drain current to zero. It was discovered from the analysis that the Poisson equation is similar to that of symmetric DG MOSFET, except that there are two boundary conditions due to different oxide interfaces. However, a proper and detailed analysis of the SCE and carrier mobility was ignored. The Cylindrical Surrounding-Gate (CSG) MOSFET, which is the fabrication of a hollowed cylindrical-like Silicon substrate with controlling gate around it. This structure has promising package of better current drive, reduced sub-threshold characteristics and reduced thermal effect. Iniguez et. al. [16] developed a unified charge control model for the CSG MOSFET. This model was analyzed using the charge density at the two ends of the channel (source and drain) to generate a charge current flowing in the channel. Yu et. al. [17] proposed the Ward-Datton Charge partition method derived from Poisson's equation without using sheet approximation to get the analytical function of the CSG MOSFET. These models have been based on high dopant channel in order to reduce SCE and increase current drive, but it has degraded the charge mobility [18]. These

challenges give rise to a cylindrical structure but with two gate (CSDG) introduced by Srivastava et. al. [19]. This device is proven to have two scaled channel path that reduced parasitic effect in the device [20]. The structural dimension of the device is also of great significance because it has little contact on the board(s) on which it is mounted. This help reduce heat and with little effort from heat sink, the device promise to provide long-lasting operation [21].
The structural density also makes it useful in VLSI circuits as billions of the structure can be packed for sophisticated functions. The work confirmed that the source to drain capacitance in the CSDG MOSFET is higher than the CSG MOSFET and hence making the drain current operational area larger in CSDG MOSFET. This also makes the stored energy to be almost double the CSG MOSFET and attributes to increased current flow than the SG and DG MOSFET. However, there is need to improve on the structure not only to overcome SCE, but for increase current drive and better carrier mobility. This work is organizes as follows. The dimensional description of the new CSDG MOSFET is in section 2. The parametric analysis of the CSDG MOSFET has been discussed in section 3. The result and discussion of this work is in section 4. Finally, section 5 has conclusion and future aspect.

2. Dimensional description of CSDG MOSFET

The CSDG MOSFET is rotatory extension of Double-gate (DG) MOSFET. Where, the DG structure is equivalent to two Single-Gate (SG) MOSFET arranged back-to-back. To design CSDG MOSFET as shown in Fig. 1, this DG MOSFET has been rotated with respect to one of its gates. This is structured in such a manner that the inner channel is alike in width and thickness as the outer channel. Moreover, both the inner and outer gates, which controls these channels are also similar in dimension. These dimension can be varied according to their specific application. A thick suitable substrate placed between the conducting channels and helps to separate activity from each other. The CSDG MOSFET has two gates, G1 and G2 (indicated in blue color), two drains, D1 and D2, (indicated in green color for p-channel, and red color for n-channel), the Oxides, oxide1 and oxide2, (indicated in yellow color), and the p-type substrate/body (indicated in red color for p-channel and green color for n-channel). The gate, G1 is formed in the inner part of the cylinder, followed by the thin oxide, oxide1 (to immune the effect of short-channel effect) while the protruding part of the cylinder is the drain and source as shown in Fig. (1) [19], [21-24], [30].
In the n-channel enhancement CSDG MOSFET, when suitable positive voltages are applied to the gates G1 and G2, the body, which has the majority carrier as holes and minority carrier as electrons, will have the holes repelling from the insulators oxide1 and oxide2 and electrons attracted toward the insulator.
Hence creating a channel in which electrons at the n-type substrate will be able to move through the source to the drain. Thus, creating n-channel in the p-type body. This structure has an intruding drain and source region, making the conducting channel of the device capable to overcome punch-through effect, velocity saturation and SCE. A hollow at the center of the structure makes it effective in limiting thermal effect in the operation of the device.

3. Parametric analysis of CSDG MOSFET

With the introduction of this new undoped-channel device, there is need to analyze its parameter with respect to drain current, transconductance, and characteristics of the capacitance and carrier mobility. In this analysis, it is important to consider the activities in the two channels when appropriate biased are applied.

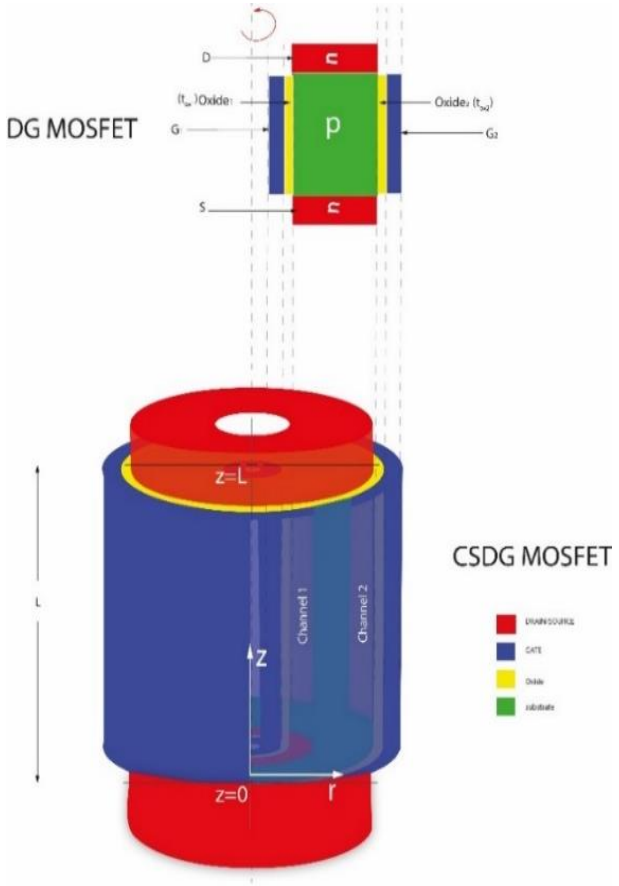

Fig. 1: Schematic Diagram of N-Channel CSDG MOSFET.

3.1. Drain current

Considering the n-channel CSDG MOSFET under the influence of electric field generated from applied voltages V_a and V_b. A 3-D analysis of the CSDG MOSFET in r and z-axis is presented in Fig. 1 with the assumption of the validity of Gradual Channel Approximation (GCA). This explains the electric field (E) generated in the inner and outer channel with assumption of different gate voltage applied to the gates. In this parameter, Pao-Sah integral [22] is utilized with consideration of the components of drift and diffusion current [23] usable at different MOSFET operation region and a constant carrier mobility. Using Pao-Sah integral for both, the inner and outer structure for the applied voltage generating electric field in the conducting channels give [22], [23]:

$$I_{d_{internal}} = \int_0^{V_{DS}} \frac{2\pi a}{L} \mu Q(V_a) \partial V \tag{1}$$

$$I_{d_{external}} = \int_0^{V_{DS}} \frac{2\pi b}{L} \mu Q(V_b) \partial V \tag{2}$$

Where V_a and V_b are the applied voltage of the internal and external gates respectively, a and b are the internal and external radius, respectively, and L and m is length of the channel and constant mobility, respectively. Expressing the charge (Q), as a function of surface potential (ψ_S), gate-source voltage (V_{GS}) and the different work function between the gate metal and the semiconductor (V_{FB}) with consideration of body effect charge (Q_B) expressed as:

$$Q = -C_{ox}(V_{GS} - V_{FB} - \psi_s) - Q_B \tag{3}$$

Considering a single conducting channel, the drain current is expressed as:

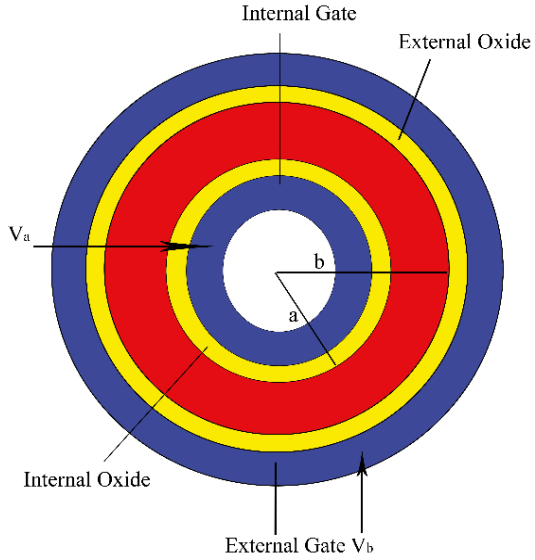

Fig. 2: Cross Sectional Area of CSDG MOSFET.

$$I_{d_{internal}} = \frac{2\pi a}{L}\mu C_{ox}\int_{\psi_{s0}}^{\psi_{sL}}(V_{GS}-V_{FB}-\phi_s)\partial\phi_s + \frac{2\pi a}{L}\int_{\psi_{s0}}^{\psi_{sL}}Q_B\partial\psi_s \quad (4)$$

But the total drain current in the CSDG MOSFET, which is the sum of the internal and external drain current is:

$$I_{d_{CSDG}} = I_{d_{internal}} + I_{d_{outer}} \quad (5)$$

Applying the drift-diffusion component with consideration of the independent applied voltages at both conducting channels of the device is expressed in Eq. (4) due to its asymmetric condition of different work function. Analyzing this in the inversion model with body effect put into account makes the drain current:

$$I_{d_{CSDG}} = \frac{2\pi(a+b)}{L}\mu\psi_s * \left[\begin{array}{l}2C_{ox}(V_{GS}-V_{FB})-C_{ox}(\psi_{sL}+\psi_{s0}) \\ +(2\Phi_t C_{ox}-Q_B)+2Q_B\end{array}\right] \quad (6)$$

The ψ_s and C_{ox} are surface potential difference and capacitance of the oxide respectively, V_{FB} and Φ_t are flat-band voltage and thermal voltage respectively, and Q_B is the body charge. The application of the drift-diffusion component helps to work with the scaling of the channel length. This makes the drain current in CSDG MOSFET more than triple as compared to the Cylindrical Surrounding-Gate (CSG) MOSFET.

3.2. Transconductance

The differential change in the drain current with the change in gate source voltage influenced by the area of the gates portray transconductance [24]. The efficiency of this device can be measured as the ratio of the output signal to the input signal. The transconductance (g_m) of this device is obtained by differentiating Eq. (6) with respect to V_{GS}, while keeping V_{DS} as a constant. Thus,

$$g_m = \frac{\partial I_d}{\partial V_{GS}} = \frac{\partial I_d}{\partial \psi_s}.\frac{\partial \psi_s}{\partial V_{GS}} \quad (7)$$

$$g_m = \frac{2\pi(a+b)}{L}\mu * \left[\begin{array}{l}2C_{ox}(V_{GS}-V_{FB})-C_{ox}(\psi_{sL}+\psi_{s0}) \\ +(2\Phi_t C_{ox}-Q_B)+2Q_B\end{array}\right]\frac{\partial\psi_s}{\partial V_{GS}} \quad (8)$$

This parameter is important because of its dependence on the input signal and explains the fact that the CSDG MOSFET gives output than that of the CSG MOSFET. It has been observed that there is an increase in transconductance with respect to increase in V_{DS}. This is made possible by the dual gate with scaled channels dimension which aid higher electron transportation near the source, this attribute enhance the driving current and gate control. Also, the higher transconductance in the double surrounding gate helps with electrostatic control in the operation [25].

3.3. Capacitance characteristics

The capacitance model of the CSDG MOSFET is derived through the equivalent circuit of the device as shown in Fig. 3. It comprise of six intrinsic capacitances, namely source-gate capacitance of the inner structure (C_{SG1}), source-gate capacitance of the outer structure (C_{SG2}), drain-gate capacitance of the inner structure (C_{DG1}), drain-gate capacitance of the outer structure (C_{DG2}), source-drain capacitance (C_{DS1}) and drain-source capacitance (C_{DS2}) of the CSDG MOSFET [26]. However, in this device the gate-oxide capacitances, (Cox_1) and (Cox_2) have been considered in the capacitance calculation. The element I_d represent the drain current of the MOSFET from the applied voltages at both gates. The gate-oxide capacitances can be expressed mathematically as:

$$C_{ox1} = \frac{E_{ox1}}{\left[aIn\left(1+\frac{t_{ox1}}{a}\right)\right]} \quad (9)$$

$$C_{ox2} = \frac{E_{ox2}}{\left[bIn\left(1+\frac{t_{ox2}}{b}\right)\right]} \quad (10)$$

Where E_{ox1} and E_{ox2} are the generated electric field at inner and gates respectively, and tox_1 and tox_2 are the oxide thickness of both inner and outer structures, respectively. These have different values due to different applied voltages that might be applied at the gates.

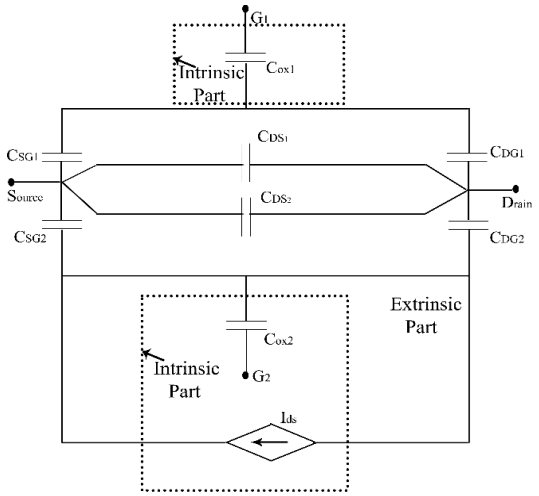

Fig. 3: The Equivalent Capacitive Model of CSDG MOSFET.

The total capacitance from the equivalent circuit comprises the capacitance in series and parallel as the drain-source current from through them. The capacitance for CSDG MOSFET is calculated as:

$$C_{CSDG} = \frac{2\pi\varepsilon L}{In\frac{b}{a}} \quad (11)$$

Considering the capacitance as sum of the capacitance in series and parallel expressed as:

$$C_{CSDG} = C_{ox1} + C_{SD} + C_{DS} + C_{ox2} + \frac{C_{SG1}C_{DG1}}{C_{SG1}+C_{DG1}} + \frac{C_{SG2}C_{DG2}}{C_{SG2}+C_{DG2}} \quad (12)$$

In the new structure, permittivity (ε) and the gate-oxide has been considered due to the effect of the body on the capacitance and this produces higher stored energy in the devices that almost doubled that of CSG MOSFET. Therefore, making the device preferable in application.

3.4. Carrier mobility

The carrier mobility has always been kept constant, but this is an integral parameter that is determined by different collision as a result of the generated electric field in the conducting channels. The movement of the charges along the channel is due to the generated field at the gates. For a heavily doped MOSFET, the mobility reduces [27] with loss of energy as a result of wider dimension of the conducting channel and different collision that takes place. Due to this collision, different scattering occur along the channel. Matthiessen rules [28] explain the relationship between the charge mobility, μand the different scattering as:

$$\frac{1}{\mu} = \frac{1}{\mu_1} + \frac{1}{\mu_2} + \frac{1}{\mu_3} + ... \quad (13)$$

Where μ_1 is the coulomb scattering, μ_2 is the phonon scattering and μ_3 is the surface roughness scattering among other scattering. But for the device in view, it is either lightly doped or undoped, so some of the scattering are not present which gives the advantage of greater mobility. Also, the dimension of the channel is smaller and the rate of collision is reduced. From Gauss' law, the electric field generated at the CSGD MOSFET is expressed as:

$$E_{CSDG} = \frac{q(a+b)}{2\pi ab\varepsilon} \quad (14)$$

Where q is the charge per length. In addition, the drift velocity, V_d is directly proportional to the electric field with the charge mobility as the proportionality constant, it could be expressed as:

$$\mu\alpha \frac{(ab)}{a+b} v_d \quad (15)$$

Implying that the carrier mobility is proportional to the drift velocity [29-31]. However the flexibility in radii of this device gives it an advantage over the bulk DG MOSFET. According to Eq. (13), if the inner radius is increased and the outer radius is fixed, the device agrees with the scalability property while still maintaining an increased in the carrier mobility in the device. It has been observed that because the CSDG MOSFET is able to control the Si-channel by reducing the channel width to be small. With the voltages applied to both sides of the gates help to suppress the SCEs and increases the carrier mobility. This can only be achieved by increasing the inner radius of the CSDG MOSFET while making the outer radius fixed.

4. Result and discussion

The performance of the CSDG MOSFET is investigated by experiments and parameters obtained are analyzed in the following. The drain current of the CSDG MOSFET is presented as a function of the drain-source voltage as in Eq. (6). This is compared to that of the CSG MOSFET.

As observed in Fig. 4, the drain current in CSDG MOSFET shows a better drive with a low threshold voltage. In fact, the current drive of the CSDG MOSFET is about three times that of the CSG MOSFET. This indicates that the CSDG MOSFET would be suitable for designing devices with low power input and high current drive.

The transconductance of the CSDG MOSFET is deduced from the drain current analysis and compared with that of CSG MOSFET.

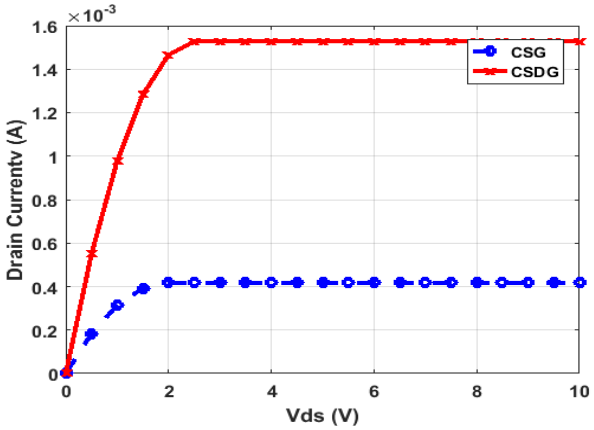

Fig. 4: Drain Current to Drain-Source Voltage of the CSG and CSDG MOSFET with Fixed V_{GS}.

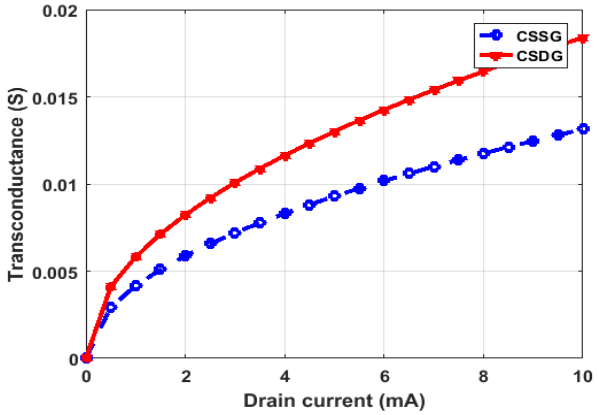

Fig. 5: Variation of Trans Conductance to Drain Current for the CSG and CSDG MOSFET.

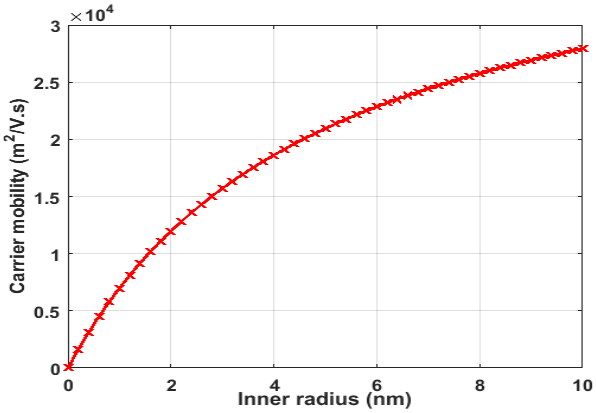

Fig. 6: Variation of the Carrier Mobility to Internal Radius of the CSDG MOSFET.

The transconductance is presented as a function of the drain-source current ranging between 0-10 mA in Fig. 5. It can be seen that as the drain current increases, the transconductance of the CSDG MOSFET exceed that of the CSG MOSFET. This makes the CSDG MOSFET suitable for high speed switching application. The carrier mobility is also presented with respect to the inner radius (a) as shown in Fig. 6. The result shows that the mobility of the charges increases and the size of the CSDG MOSFET is retained as the external radius is fixed with varying inner gate radius.

Thus, the CSDG MOSFET is able to control the Si-channel whose dimension is relatively small. Further-more, the voltages applied to both sides of the gate to suppress the SCEs and increases the carrier mobility. This can only be achieved by increasing the inner radius of the CSDG MOSFET while keeping the outer radius fixed.

5. Conclusions and future works

In this work, a new CSDG MOSFET structure have been introduced and its analysis done on the basis of drain current, transconductance, capacitance characteristics and carrier mobility. The analysis of the drain current involved the use of drift-diffusion application to each of the conducting channel in the device while also applying the Pao-Sah Integral as the basis of consideration. The transconductance of the devices was thus analyzed from the drain current analysis. Capacitance characteristics in the CSDG MOSFET was calculated and a higher storage attribute was produced.

The work further considered the carrier mobility in isolation unlike previous work where it is considered as a constant. With Gauss' law, an expression of the mobility was presented, which is in agreement with scalability. In all, it has been discovered that the CSDG MOSFET is better in performance than the bulk DG MOSFET and CSG MOSFET. It also allows for scaling with the help of its radii and will be a better device for application due to its low power consumption and higher drain current. Beyond the parametric analysis, there is the need to examine the application of the device as an amplifier. This will be analyzed in future work to investigate how its parameters affects application as an amplifier. Also, potential challenges such as heat and noise that could be associated with its performance will also investigated.

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